A 10-bit SAR ADC With Two Redundant Decisions and Splitted-MSB-Cap DAC Array

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Abstract—**A novel switching method is proposed and implemented in a 10-bit fully differential SAR ADC. When compared with the charge recycling or the set-and-down approach, the proposed scheme uses a single-ended switching procedure to reduce the total switching energy by 80% or 20%, respectively. Besides, two redundant decisions are inserted in the SAR ADC with a 4b/4b/4b configuration, which is capable of more than 30% speed enhancement. The 10-bit SAR ADC's performance is verified through Matlab simulation and it achieves 10-b resolution. After a Monte-Carlo analysis (100-times), the mean value of the SNDR is 61.8dB, and the maximum INL and DNL are 0.05LSB and 0.1LSB, respectively.**

I. INTRODUCTION

Conventional SAR ADCs use a binary-weighted capacitive array to implement the DAC and the sample-and-hold function [1]. Recently, when compared with the flash and pipeline converters, SAR ADCs have been widely used for low-power applications.

The power consumption of SAR ADCs depend on three dominant circuit components: the digital logic, the comparator and the DAC array. In recent years, work has been focused on coming up with smart switching techniques to decrease the switching power, such as charge-recycling [2] and set-and-down method [3]. The traditional topology wastes a lot of energy on changing the voltage on the top plate of capacitors and switching the next capacitor from ground to V_{ref}. Though the charge-recycling method uses the same amount of capacitance to improve slightly this aspect, it still has the disadvantage of doubling the number of switches. On the other hand, the set-and-down scheme reduces half capacitance and costs much less switching energy, but, it still requires a large sum of energy to convert middle output codes.

Moreover, the speed of the SAR ADC is limited by the settling time of the DAC, SA logic and decision time of the comparator. For a n-bit SAR ADC, it takes *n* decisions for every conversion, and every decision must be as accurate as the full ADC resolution. The requirement of settling error for every decision can be expressed as:

$$settling\ error = V_0 \times e^{\left(\frac{-t}{\tau}\right)} < V_{ref} / 2^{n+1} \qquad (1)$$

With settling time,

$$t > \tau \times \ln\left(\frac{1}{2^{n+1}} \times \frac{V_{ref}}{V_0}\right) \qquad (2)$$
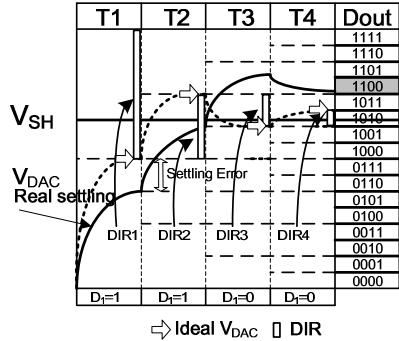

Fig. 1 Example of settling error causing wrong decisions.

where V_0 is the desired settling amplitude in each step.

When the DAC settling time is incomplete the ADC can't export accurate decision codes. As shown in Fig.1, V_{SH} is the sample input and the ideal conversion settling is the dotted line where the white bars are the ideal determined input range (DIR). Since there are some settling errors the output codes don't exhibit n bit accuracy.

Therefore, a new switching scheme is proposed which uses a single-ended switching procedure, not only decreasing the dimension of the capacitor array, but also reducing the energy consumption necessary for converting the middle-scale output codes. Besides, for relaxing the requirement of settling time, redundant decisions are inserted in the SAR ADC. Plus, the addition of digital error correction [4] is also implemented to achieve the desired resolution.

The paper will be organized as follows: Section II introduces the proposed switching scheme and energy saving; Section III reviews the algorithm of redundancy and presents its implementation in the proposed switching technique; Section IV presents the simulation results and the conclusions are drawn in Section V.

II. PROPOSED SWITCHING METHOD

As shown in Fig.2, the DAC array exhibits a new topology that uses 4 unit capacitors to achieve a 3-bit SAR ADC. The proposed switching algorithm applied in this SAR ADC is a single-ended switching procedure, which only switches one capacitor on one side of the capacitive array after the first transition.

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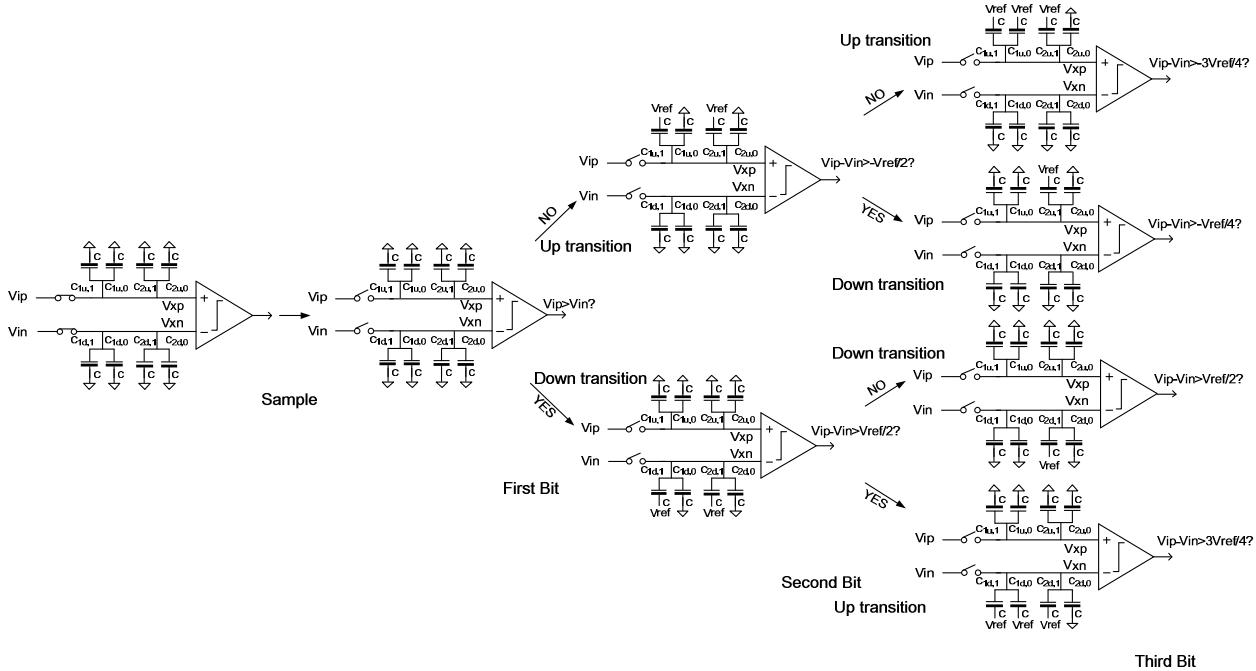
Fig. 2 The single-ended switching procedure of a 3-bit SAR ADC.
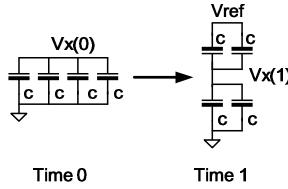
Fig. 3 The first transition T1 in the proposed switching.
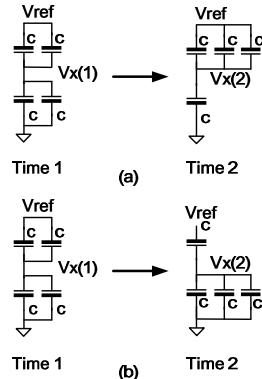
Fig. 4 The second transition T2 in the proposed switching:

(a) "up" transition; (b) "down" transition.

Fig.5 Switching energy versus output code for different switching methods.

Initially, during sampling, the positive and negative voltages, V_{XP} and V_{XN} in the capacitor array store V_{IP} and V_{IN}, respectively. Then, at the instant of time 0, these sampling switches are opened, and then the first bit B_1 can be decided by the value of V_{XP} minus V_{XN}. If the value is positive, B_1 is 1, otherwise, B_1 is 0.

Every bit code controls the next switch transition. As shown in Fig. 2, for the first transition T1, up transition is defined while V_{XP} increases. Oppositely, it is called down transition. For the following transitions, if V_{XP} or V_{XN} increases, the tran-

sition is an up transition. Otherwise, it is a down transition. For instance, if 011 is the output code, the SAR ADC goes through one up transition and one down transition, successively.

As is analyzed in [2][5], the switching energy for each transition can be worked out. Initially, since all capacitors do not need to be switched before obtaining the first bit, the DAC doesn't consume switching energy.

As depicted in Fig.3, in the first transition, if the capacitor array settles during $t1$, the total energy drawn from V_{ref} is

$$
\begin{aligned}
E_{0 \to 1} &= U \times i(t)t = V_{\text{ref}} \int_{t0}^{t1} i(t)dt = V_{ref} \int_{t0}^{t1} \left(-2C \times \frac{du(t)}{dt} \right) dt \\
&= -V_{ref} \times 2C \times (u(t1) - u(t0)) \\
&= -V_{ref} \times 2C \times \left(\left(V_{X(1)} - V_{ref} \right) - \left(V_{X(0)} - 0 \right) \right)
\end{aligned}
\tag{3}
$$

The voltage difference of V_{XP} or V_{XN} (up transition or down transition) is $V_{ref}/2$ and energy consumption is CV^2_{ref} that is the same as in [3] at T1. During the second-bit cycle, the up or down transition shown in Fig.4. Based on Eq.(3), the

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switching energy is $1/4CV^2_{ref}$ for the transition. However, for a 3-b SAR ADC, [3] uses 3 times more energy to lower the voltage of the comparator input at the second down transition because it needs to discharge a capacitor 2 times larger to ground, when compared with the proposed technique.

However, the input common-mode (CM) of comparator varies according to the input signal because the proposed switching procedure keeps the larger input side stable and then alters the other to approximate it. The variation would cause dynamic offset and result in degradation of ADC performance. Therefore, the SAR ADC should design a comparator insensitive to input CM range [6] and further insert redundant decisions to improve its performance.

In short, the total capacitance of the proposed method is 2^{n-1} unit capacitors, identical to the set-and-down, yet it consumes about 20% less energy. Compared with the charge-recycling method, this will reduce half capacitance and consumes about 80% less switching energy. Especially, in the middle of the digital output codes, the advantage will be more significant, as shown in Fig.5.

III. REDUNDANCY REVIEW AND IMPLEMENTATION OF THE PROPOSED SWITCHING METHOD

A. Review of the redundancy method

The redundancy method relaxes effectively and efficiently the tight requirement of settling. Furthermore, binary redundancy with respect to non-binary method can lower the demand of capacitance mismatch without burdening the digital circuits. The redundancy decisions presented on [5] enables the correction of the settling error, with the SAR ADC segmented into coarse and fine conversion. Considering the critical requirement of capacitance mismatch and the effect of parasitic capacitance, there is a need to apply this method together with other switching schemes.

Fig.6 presents an example of a 2-b-coarse and 3-b-fine with 1-b redundancy SAR ADC to correct the settling error. The main algorithm inserts redundant decisions and uses addition-only digital error correction (ADEC) to get the accurate output codes. This digital correction method shifts up all of the decision thresholds of the coarse ADC by $1/8\ V_{ref}$. And, as long as the settling error is less than 0.5 LSB of the coarse resolution, fine SAR conversion enables the correction.

Also, from Fig.6 it is possible to verify that the ADC is segmented into two sub-DACs, DAC_H and DAC_L, considering the position of the inserted redundant decision. By switching the second largest capacitor to V_{ref}, the ADC shifts the coarse decision to $5/8V_{ref}$, getting the threshold $5/8\ V_{ref}$ instead of $1/2V_{ref}$. Following the switching procedure the additional conversion step T3 is realized by switching 2C to V_{CM}, which makes V_{DAC} located at the center of DIR2. While all 5 digital codes were determined, ADEC imposes MSBs and LSBs with 1-b overlap to achieve the final desired digital codes.

B. The implementation of the redundancy method in the proposed switching scheme

The redundancy implementation is segmented into three conversions: first, coarse and fine conversion. Fig.7 shows a 5-bit SAR ADC with 1-bit redundancy.
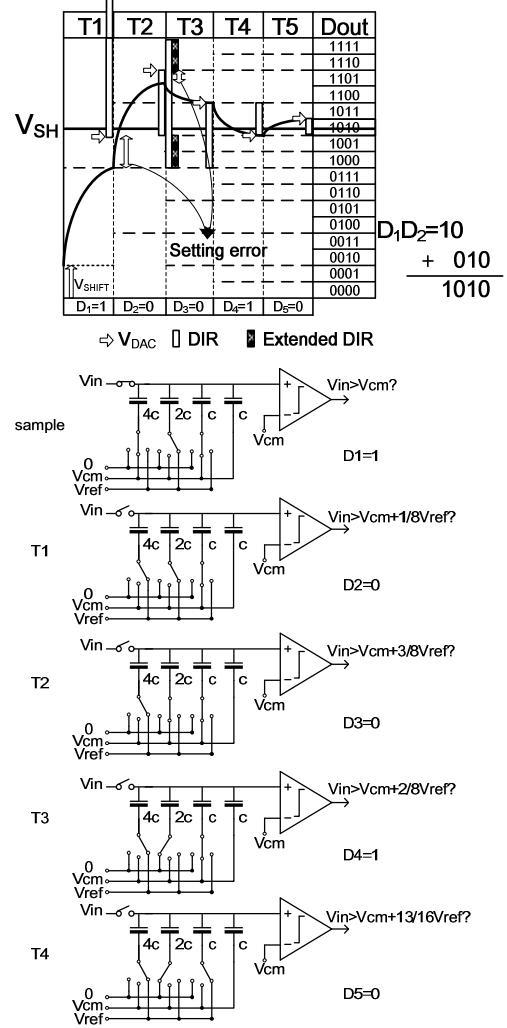
Fig. 6 A 2-b-coarse and 3-b-fine with 1-b redundancy ADEC SAR ADC to correct the settling error.

Due to the proposed switching scheme, to get the first code does not imply the switching of any capacitors connected to the ground. After B1 is confirmed, the threshold will be shifted to $5/8V_{ref}$ or $3/8V_{ref}$ by connecting C_{2D} both to V_{ref} or C_{2U} both to ground. When deciding the redundant decision, $1/8V_{ref}$ needs to be subtracted or added correspondingly.

Since coarse decisions were converted the following operation of switching has to be analyzed in detail. There are three different ways according to two different shifted thresholds $5/8V_{ref}$ and $3/8V_{ref}$: i) The first corresponds to the original switching process while B3, the bit before the redundant decision, is 0. It only has half of the C_{2U} to be connected to ground or V_{ref} accordingly for returning the V_{DAC} back to the center of last DIR; ii) The second is called a reset mode because of the DAC settling overflow. This happens when B2B3 equals to 11 and at this time B3 has to be reset to zero. iii) The final one arises when the last bit of the coarse conversion (B3 is the example in Fig.7), before the redundant decision, is 1. Taking B2B3=01 into consideration, if B1=0, the up third capacitor needs to be returned to V_{ref}. Inversely, the fourth down capacitor is switched to ground.
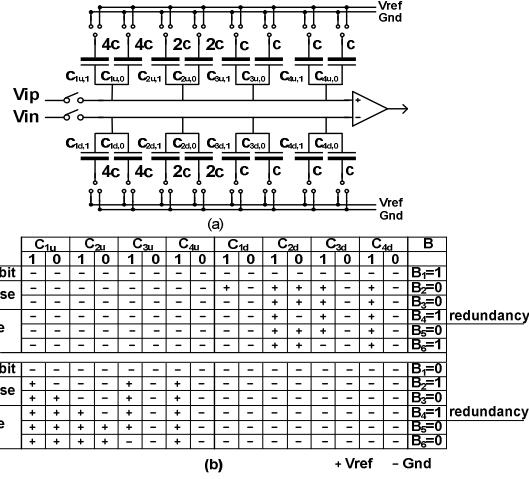
Fig. 7 (a) A 5-bit proposed SAR ADC; (b) corresponding switching table.

Fig.9. 100-time Monte-Carlo simulation of the proposed SAR ADC.

Fig.10. INL and DNL vs. digital output codes.

However, the operation for this case actually shifts V_{DAC} to the bottom or top of the DIR (B1=1 or B1=0) rather than to its center. So, it is necessary to switch the up or down second capacitor to ground or V_{ref}, separately, in such a way that V_{DAC} will be moved to the desired level of DIR.

IV. SIMULATION RESULTS OF THE PROPOSED SAR ADC

The 10-b SAR ADC with a 4-b/4-b/4-b configuration has 512 unit capacitors on each side array, which consists of two binary weighted capacitor arrays with total 256 capacitances. It reduces the capacitance to half with respect to the conventional SAR and also implements a common-centroid topology efficiently in the layout of the DAC array.

$$
\begin{array}{llll}
B1\ B2\ B3\ B4 & & & \\
& B5\ B6\ B7\ B8 & & \\
+ & & B9\ B10\ B11\ B12 \\
\hline
D1\ D2\ D3\ D4\ D5\ D6\ D7\ D8\ D9\ D10
\end{array}
$$

Fig.8. Output codes of the proposed SAR ADC

In the topology, two bit redundancies are inserted: B5 and B9. The first brings in $1/16\ V_{ref}$ offset before the first decision and the second is $1/128\ V_{ref}$ before the fifth decision. As shown in Fig.8, the digital correction is also applied in the SAR ADC.

Due to the single-ended switching scheme and assuming the same time constant at each step, the first 4b requires 3-b accurate DAC settling: $\tau * \ln(\frac{1}{2^{4+1}} * \frac{V_{ref}}{V_{ref}/2})$. Then, the second and final 4b both require 4-b accurate DAC settling. Therefore, the settling time of 4b/4b/4b case for each step is 4 accurate DAC settling. When compared with the set-and-down ADC with 10 accurate DAC settling, the whole DAC settling time is enhanced by more than 30% .

In the Matlab model of the proposed SAR ADC a Gaussian random variable with standard deviation of 1% is added to the value of the unit capacitor. Considering that all conditions are identical, under the condition of the 100-times Monte-Carlo capacitor mismatch simulation, the mean value is 61.8dB SNDR, shown in Fig.9. Finally, Fig.10 depicts the maximum DNL and INL that are 0.1LSB and 0.05LSB, respectively.
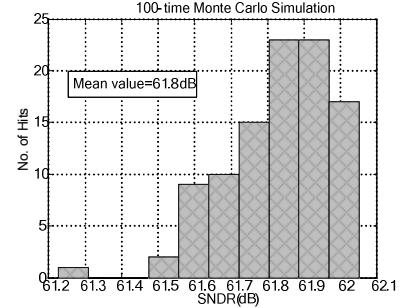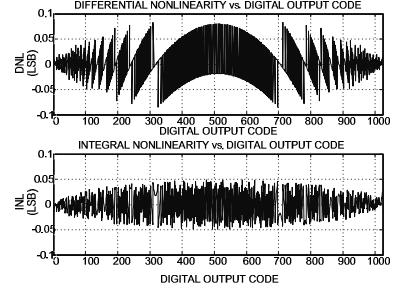
V. CONCLUSIONS

This paper presents a 10-bit SAR ADC with a single-ended switching procedure and 2-bit redundancy. This switching technique reduces 50 percent of the area of the DAC array and imposes better switching energy efficiency in the converter. Furthermore, the redundancy method enhances the settling speed of the DAC and relaxes the comparator's accuracy.

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