On-Chip Unsteady Reference Voltage Compensation Techniques for Very-High-Speed Pipelined ADC

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Abstract – The operating principle of pipelined analog-to-digital converter (ADC) is to subtract, sequentially along the cascaded stages, different reference voltages from the analog sample. This operation, nevertheless, creates internally an input-dependent fluctuation on the reference voltage. Such kind of signal-dependent error cannot be eliminated by trimming and/or calibration. The effect is especially significant at very-high conversion rate, since conventional method for stabilizing the reference voltage with large off-chip capacitor is no longer appropriate, as such a capacitor will resonate with the package inductance. However, on-chip generates a stable and high-speed reference not only consumes large power and area, but also makes the reference voltage highly sensitive to internal noises. This paper, first, presents an in-depth investigation on the causes and effects of unsteady reference voltage. Then, an effective model scheme is carried out and verified by circuit simulations. Finally, two on-chip reference voltage compensation techniques, which can effectively eliminate the error without the aforementioned drawbacks and feature compact in size, are proposed.

I. Introduction

High-speed pipelined analog-to-digital converter (ADC) is generally assisted by background or post-fabrication calibration to compensate the errors induced by diverse circuit non-idealities and process variations. Numerous calibration techniques [1-3] have been proposed for the correction of op-amp finite DC gain and gain-bandwidth product (GBW), offset in comparators and clock-jitter noise, etc. In additional to them, unsteady reference voltage has been proved recently to be another dominant noise source that hardly can be calibrated out by traditional approaches, since its induced error is highly input dependent [4]. For instance, a buffered reference voltage of an 8-bit 400-MHz pipelined ADC (1.5-bit/stage followed by a 2-bit flash) will exhibit a signal-dependent variation as large as 3 times of its numerical difference, while the allowed settling time is less than 1.25 ns (half of the sampling period). Thus, power-hungry driving buffer and large capacitive decoupling are traditionally needed for stabilizing the reference voltage.

This paper concentrates on such a matter presenting thorough analysis and effective model scheme, followed by the proposal of two novel on-chip reference voltage compensating techniques, as well as the comparison of their simulated performances against the traditional techniques. Although the analysis is carried in general single-channel 1.5-bit resolution per stage pipelined ADC, the modeling techniques and presented results are still applicable to other enhanced architectures such as time-interleaved or double-sampling, since all channels typically share only one reference voltage generator.

II. Dynamic Error: Sample-Variant Fluctuation on Reference Voltage

A. Source of Dynamic Error

The source of unsteady reference voltage is described in Fig. 1, based on a 1.5-bit/stage pipelined ADC. In normal operation, during phase 1 (phase 2), the sampling capacitor C_s in the even (odd) stages requires different reference voltages (i.e., $\pm V_{ref}$ or 0) to accomplish coarse digitization as well as signal passing. Recalling that the saved charge in C_s is came from the stage analog input, therefore, direct coupling the reference voltage buffer will drive the instantaneous reference voltage, $V_{ref}(nT_s/2)$, loses its original precision with different extent [range from V_{ref_ideal} to $V_{drop}(nT_s/2)$ as depicted in Fig. 1].

Other that such coupling effect, the amount of imprecision also depends on the total number of capacitor C_s loaded to the buffer at every instant, since the connection of $-V_{ref}$, 0 or $+V_{ref}$ to the stage is determined by the digital output codes m {-1, 0, +1} of their sub-ADCs (the functionality of the sub-ADCs is to perform coarse digitization of the stage analog input range, i.e., $< -V_{ref}/4$, $[-V_{ref}/4, V_{ref}/4)$, or $\geq V_{ref}/4$). If the C_s in all stages are equal in size, the maximum voltage drop of an N-bit ADC can be found,

$$V_{drop,max} = \frac{V_{ref}}{4} + \frac{3}{4} V_{ref} \left(\frac{1}{1 + \frac{C_s}{C_p} \cdot \left\lceil \frac{N - N_f}{2} \right\rceil} \right) \qquad (1)$$

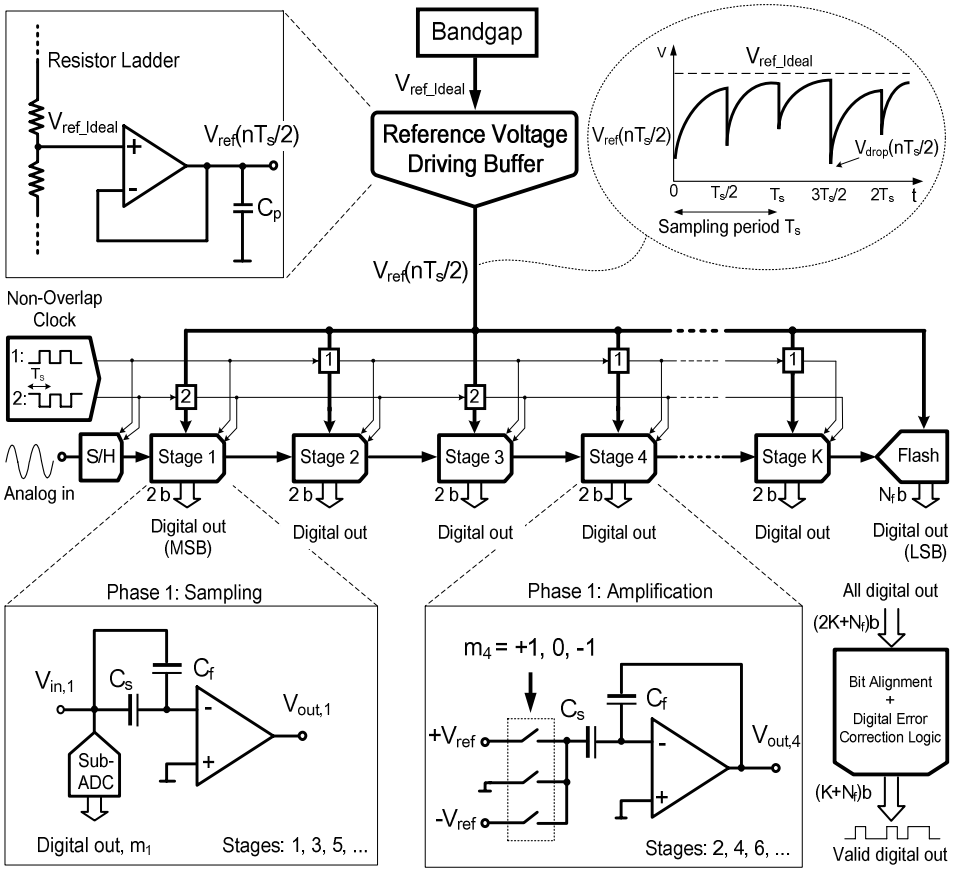


Fig. 1 A generic switched-capacitor 1.5-bit/stage pipelined ADC. The number of pipelined stage, *K*, is assumed to be even

where N and N_f are the resolution of the entire ADC and the last stage sub-ADC, respectively. C_p models all the parasitic capacitances at the buffer's output. These two operating mechanisms create the channel that links the signal dynamicity (i.e., the signal swing and frequency) to the reference voltage fluctuation. Conventional capacitive decoupling is helpful to reduce such fluctuation. However, it is not well suited for high-speed operation because, as described next, doing decoupling off-chip suffers from package-inductance induced oscillation; while on-chip approach occupies huge chip area.

B. Model of Dynamic Error

The modeling approach can be described as follows: Denote $m_k(nT_s/2)$ as outputs from sub-ADC at stage k in each half sampling period which equals either -1, 0 or +1. The equivalent capacitive loading in each half sampling period is given by,

$$C_{eq}(nT_s/2)=\begin{cases}\sum_{k=1}^{\lceil (N-N_f)/2 \rceil}\left(C_{s,2k-1}\cdot\left|m_{2k-1}(nT_s/2)\right|\right) & \text{for } n=1,3,5...\\ \sum_{k=1}^{\lfloor (N-N_f)/2 \rfloor}\left(C_{s,2k}\cdot\left|m_{2k}(nT_s/2)\right|\right) & \text{for } n=2,4,6...\end{cases} \tag{2}$$

where, $C_{s,k}$ is the sampling capacitor at stage k. N and N_f are the resolution of the entire ADC and the last stage sub-ADC, respectively.

Due to the finite recovery speed of the driving buffer, the initial voltage drop limits the precision of V_{ref} reached at every half-clock period. Moreover, the reference voltage is also affected by input-dependent variations caused by sample-variant capacitive loading. Assuming the buffer's op-amp is a non-linear single-pole system, the non-ideal reference voltage, $V_{ref}(nT_s/2)$, reached at the end of each amplification phase can be expressed as,

If slew-rate (SR)> $SR_{min}=\dfrac{|V_{drop}|}{\tau}$, linear settling yields,

$$\begin{aligned}V_{ref}(nT_s/2)=&\left[V_{ref}\left(\frac{n-1}{2}T_s\right)-V_{drop}\left(\frac{n-1}{2}T_s\right)\right]\\&+V_{drop}\left(\frac{n-1}{2}T_s\right)\cdot\left(1-e^{-T_S/2\tau}\right)\end{aligned} \tag{3a}$$

Otherwise, non-linear settling results

$$\begin{aligned}V_{ref}(nT_s/2)=&V_{ref}\left(\frac{n-1}{2}T_s\right)-e^{\frac{-(T_S-2t_0)}{2\tau}}\times\\&\left[V_{drop}\left(\frac{n-1}{2}T_s\right)-SR_{min}\cdot t_0\cdot sign\left[V_{drop}\left(\frac{n-1}{2}T_s\right)\right]\right]\end{aligned} \tag{3b}$$

where $t_0=\dfrac{|V_{drop}|}{SR_{min}}-\tau$, $\tau=\dfrac{1}{2\pi\cdot\beta\cdot GBW}$ (4)

τ is the settling time constant and β is the feedback factor of the buffers' op-amp. Founded by (2)-(4), the effective number of bits (ENOB) of the entire converter, in terms of the precision of driving buffer and the entire ADC resolution, is plotted in Fig. 2. It shows that the appropriate precision of the reference voltage buffer is around 1 bit less than the required resolution of the ADC, precision higher than that is generally exhausted.

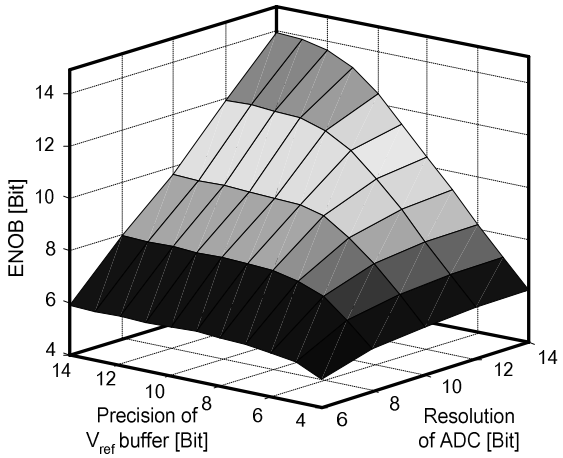


Fig. 2 Reference voltage buffer precisions versus ENOBs for different ADC resolutions.

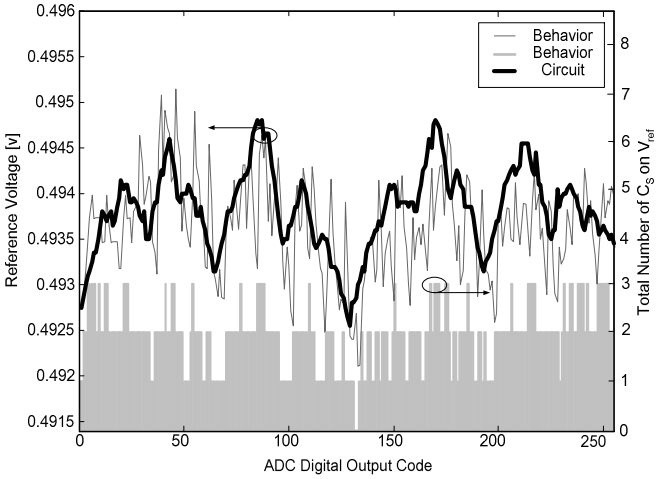


Fig. 3 Behavior and circuit simulation results of V_{ref}.

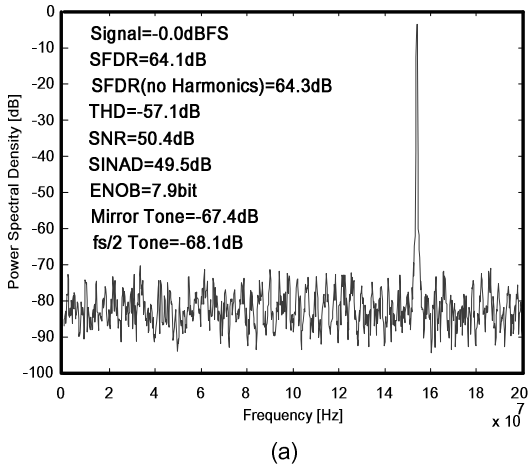
Such model is verified by comparing the behavioral simulations obtained in Matlab™ with the one obtained through circuit simulation in Cadence™. The assumptions include 200-MHz sampling rate, 10-bit resolution, 1.5-bit/stage and 1-V_{pp} input range (0.5-V reference voltage). With a ramp signal as the analog input, the reference voltage reached at $nT_s/2$ is plotted in Fig. 3. Such results follow our expectation by assuming that it is a single-pole system with small-signal settling (i.e. the slewing of the op-amp is ignored). As it can be observed that even the accuracy of the model is not high, the tendency is well predicted. Such tendency helps to characterize the magnitude of the distortion components, which is very imperative since it is input-dependent and dynamic in nature. The modeled results can also be translated to measurable ADC performances index such as spurious-free dynamic range (SFDR). For instance, comparing the spectrum purity of an 8-bit ADC with 6-bit V_{ref} precision to the one that possesses infinite V_{ref} precision, an increase in harmonic distortion is clearly observed, as shown in Fig. 4(a) and (b).

III. Conventional On/Off-Chip Reference Voltage Stabilizations

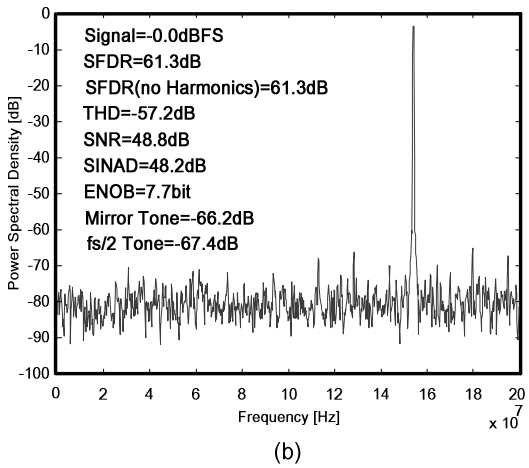
Adding a large decoupling capacitor to increase the ratio of non-switching capacitance to the switching ones is highly effective for stabilization the reference voltage. Another advantage is such a capacitor also performs compensation for multistage op-amp-based buffer [5]. The output impedance of the buffer would be extremely low at all frequencies and consumes little power.

The effectiveness of this method in very high-speed operation is studied by the equivalent-circuit model depicted in Fig. 5. The capacitive load of the driving buffer is modeled as two sets of interleave-switching capacitor pairs from odd and even stages. All the capacitors are pre-charged with distinct voltage levels to emulate the unknown stored charge from the previous phase. For the buffer, the op-amp is assumed as a single-pole linear system with very low close-loop output impedance (close to the open-loop output impedance, R_{out}, divided by the DC gain A_o). The two-phase operation is driven by two non-overlap clock phases, namely 1 and 2.

Firstly, consider the model without the package and external decoupling capacitor components. At phase 1, the odd stage capacitors are charged with 0.4 V and 0.46 V while the even stages ones are connected to V_{ref}. Similar operation runs at phase 2 with different pre-charged voltages. The sampling frequency is set to be 400 MHz. The resulted V_{ref} is plotted in Fig. 6(a), which is set to be 0.5 V originally. The observable static negative offset from 0.5 V to 0.48 V is due to periodic charge and discharge of switching capacitors, which is



(a)



(b)

Fig. 4 Power spectrum density (non-ideal model simulation). (a) With infinite V_{ref} precision. (b) With 6-bit V_{ref} precision

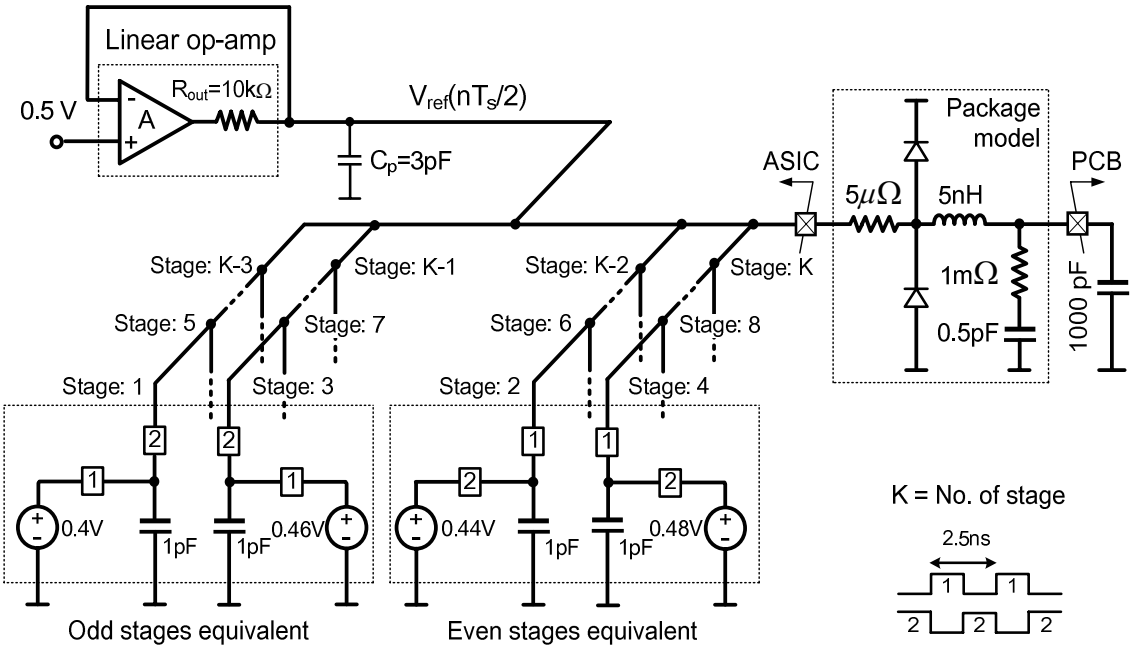


Fig. 5 A two-phase equivalent-circuit model of V_{ref} generation in pipelined ADC.

thermo-dynamically equivalent to a real resistor loaded on the buffer at such a high sampling rate (the resulting impact of constant negative offset mainly reflected in the spurious free dynamic range [2]). When the clock is activating at either phase 1 or 2, the pre-charge voltages in the odd or even stage equivalents will be averaged. Recovering the originally value calls for instantaneous action, i.e., large transient current. The recovering speed is therefore highly related to the slew rate, output impedance and GBW (i.e., power) of the buffer, and also the *RC* time constant formed by the switches and the sampling capacitors.

For instance, by using a linear single-pole op-amp (60-dB DC gain and 1-Grad/s GBW) together with a 1000-pF on-chip decoupling capacitor, a highly stabilized V_{ref} is obtained in Fig. 6(b). Such a capacitor regrettably occupies huge chip area. Rather, in off-chip approach, the inductance of the package bondwires will resonate with the capacitor as illustrated in Fig. 6(c), and the resonant frequency is easy to be inside Nyquist. One solution for that is to reduce the bondwire inductance by parallel use of bondwires. This way, however, raises the package cost and may not be always possible. Another solution is by adding a resistor R (e.g., 100 Ω) in series with the decoupling capacitor and bondwire to increase the damping speed, but the resistor cannot be too large as it will also cause a periodic voltage drop when the sharp current of the switching circuits is injected into the resistor [Fig. 6(d)].

IV. Proposed On-Chip Reference Voltage Compensations

To get rid of the input-dependent fluctuation without the use of large decoupling capacitor and/or power-hungry driving buffer, two on-chip V_{ref} compensations are proposed. They are conducted by adding a compensational branch to the 1.5-bit multiplying digital-to-analog converter (MDAC).

A. Weighted-summer V_{ref} Compensation

The first method is shown in Fig. 7(a). This circuit has been known for years in low-voltage pipelined ADC but has not been applied to eliminate the input-dependence error on the reference voltage. Injecting the reference voltage at the virtual ground through an additional capacitor C_c allows linear and separately weighted summation. With the same working conditions as above cases, its performance is shown in Fig. 6(e). The instantaneous voltage drop keeps constant after C_c resets at every half of sample period. The size of C_c should be identical to that of C_s and C_f. Therefore, the main overhead of this technique is the feedback factor, which is now degraded from 1/2 to 1/3.

B. Correlated Double-Sampled V_{ref} Compensation

Another method is showed in Fig. 7(b) single-endedly. To eliminate the signal dependence, at the sampling phase (phase 1), the input signal is not only sampled by capacitors C_s and C_f, and also sampled by C_c such that it can be used for compensation at the amplifying phase (phase 2). Considering there are three cases for different values of m: when m=+1 (-1), C_c is charged with the potential difference of V_{ref} ($-V_{ref}$) and $+2V_{ref}$ ($-2V_{ref}$), thus results in no transient voltage drop, i.e., $V_{ref}(nT_s/2)$= $+V_{ref}$ ($-V_{ref}$). For m=0, C_c is self-reset so as to perform only signal amplification. The DC voltages $\pm 2V_{ref}$ can be generated by resistor ladder similar to that of $\pm V_{ref}$. The simulated performance of this method is shown in Fig. 6(f). It is noteworthy that the voltage drop in this case is due to the transient current sunk to the resistor ladder. The recovery speed, however, is extremely fast since such a resistor ladder can be designed to be very small through parallelism. For the MDAC, this method will not degrade the feedback factor (i.e., faster in speed than method 1), but the capacitive load is increased from 2C to 3C at the sampling phase.

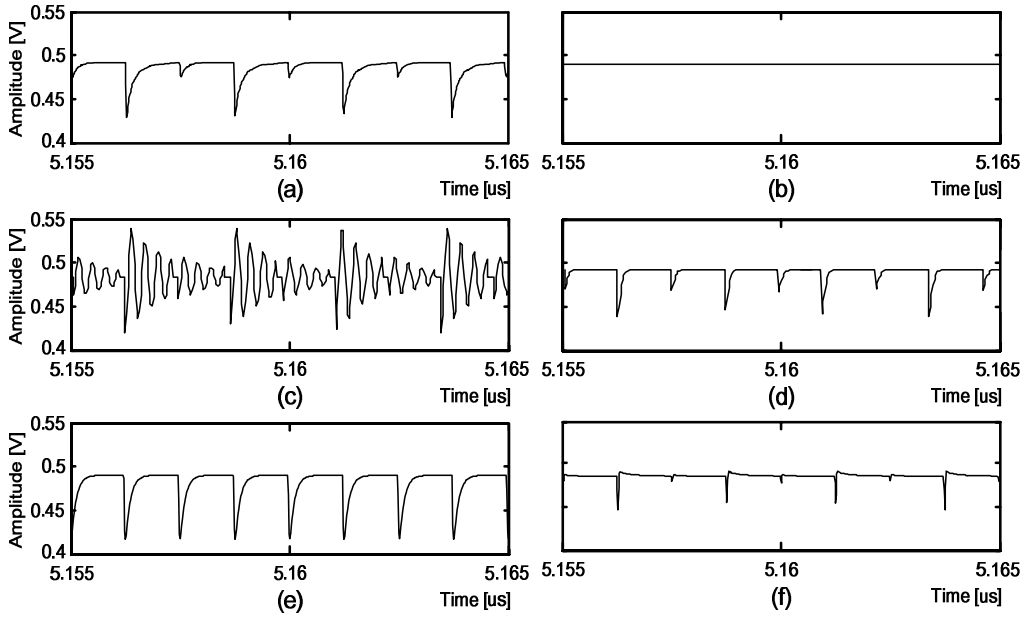


Fig. 6 Simulated reference voltages. (a) No stabilization. (b) With 1000-pF stabilization capacitor on-chip. (c) With 1000-pF stabilization capacitor off-chip. (d) Case (c) with another 100-Ω resistor added in series. (e) Proposed on-chip V_{ref} compensation method 1. (f) Proposed on-chip V_{ref} compensation method 2.

V. Conclusion

An exhaustive analysis on the causes and effects of unsteady reference voltage to the performance degradation of very-high-speed pipelined ADC was presented. The sample-variant loading effect is a dynamic error, which is input-dependent and therefore induces harmonic distortion. Featuring such characteristic, calibration to this error is ineffective. For off-chip stabilized approach, it will cause package-inductance-induced oscillation. Hence, stabilizing the reference voltage in very-high-speed operation requires purely on-chip solutions. Two proposals were given to eliminate the problem by using pure circuit techniques, which featured simple in implementation and compact in size.

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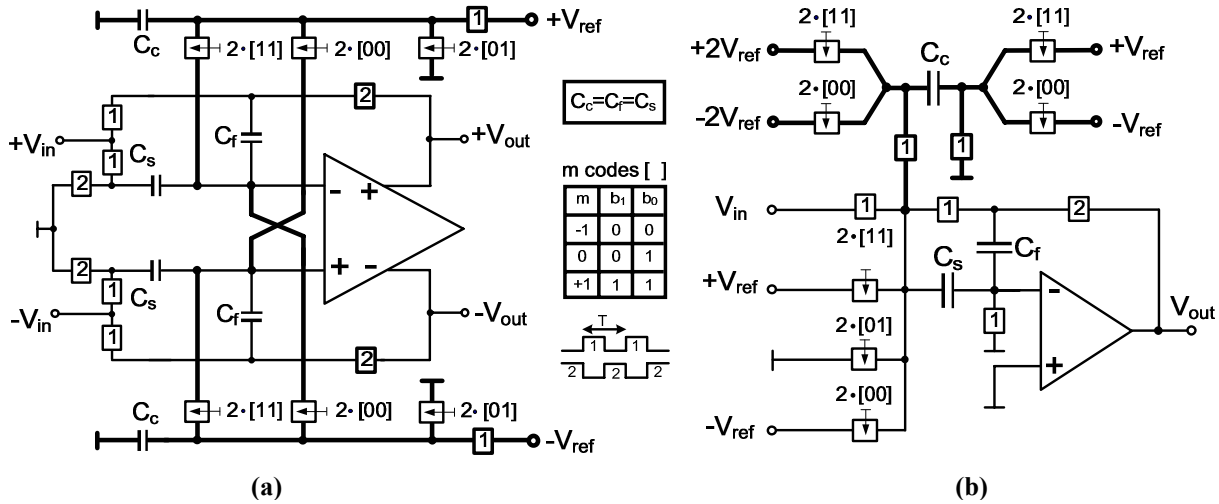

Fig. 7 (a) Weighted-summer V_{ref} compensation. (b) Correlated double-sampled V_{ref} compensation.