A 28-µW EEG Readout Front-End Utilizing a Current-Mode Instrumentation Amplifier and a Source-Follower-Based LPF

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***Abstract*—A novel low-power EEG readout front-end featuring a current-mode instrumentation amplifier (CMIA) followed by a 4th-order gain-compensated source-follower-based lowpass filter (LPF) is proposed. The CMIA is of current-conveyor topology and is chopper-stabilized to improve the common-mode noise rejection and suppress the dc-offset and 1/*f* noise. The typical gain-loss problem of source-follower-based LPF is alleviated by adopting a gain-compensation technique. Optimized in 0.35-µm CMOS, the achieved CMRR is >100 dB from 0.01 to 16 Hz, and >90 dB up to 40 Hz. With the chopper stabilization, the noise voltage density is 248 nV√Hz at 0.01 Hz and 197 nV√Hz at 100 Hz. The power consumption is 28 µW at 3 V.**

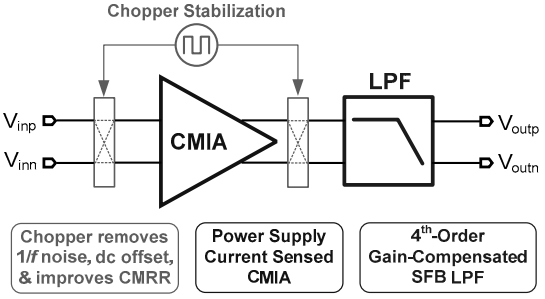

Fig. 1. Proposed EEG readout front-end.

I. Introduction

Electroencephalogram (EEG) reflects the electrical activity of the brain as a diagnosis reference of Epilepsy and other neuropathies. In clinical applications, the most relevant signals spread over 0.3 to 40 Hz with amplitude ranging from 2 µV to several hundreds of µV. The ultra-low-frequency EEG signal (below 0.1 Hz) is mainly informative for diagnosis of cerebral death whose threshold amplitude is 2 µV. Most present clinical technologies require the patients, who are under a long-time continuous monitoring, to be connected by a bulky instrument, which keeps them of their normal routines while causing discomforts. This discomfort may change the pathological characteristics of the measured EEG signal and induce possible diagnosis faults [1]. Thus, ultra-low-power (ULP) and miniaturized EEG acquisition system is on great demand for ambulatory clinical practice. The aim is to provide both comfort and accurate diagnosis for patients, while extending the applications to health care, entertainment and sport [2].

The most critical and power consuming building block of portable EEG measuring system is the readout front-end which has to dissipate ULP. The front-end instrumentation amplifier (IA) defining the signal quality has to feature a high common-mode rejection ratio (CMRR) such that the strong interference from the mains can be rejected, and to feature a high signal-to-noise (SNR) ratio to extract the weak biopotential signals. This paper proposes a novel EEG readout front-end. It is structured by a current-mode IA (CMIA) followed by an ULP LPF. The block schematic is depicted in Fig. 1. The CMIA is based on a power-supply current-sensed current conveyor. Its central principle was reported in [3] and was recently gained more attention in biomedical applications [4]. The proposed CMIA features chopper stabilization for dc-offset and 1/*f* noise removals while improving CMRR. The LPF is based on a 4th-order source-follower-based (SFB) structure. Different from the existing SFB LPF that employs saturation-biased transistors and is targeted for high-frequency applications [5], this work explores subthreshold-biased SFB LPF for ultra-low-frequency biomedical applications. The typical gain-loss problem of SFB LPF is alleviated in this work by adopting a new gain-compensation technique.

II. Current Mode IA (CMIA)

A. CMIA Circuit Topology

Figure 2(a) shows the block schematic of the proposed CMIA. It consists of two Op Amps A_1 and A_2, and a resistor R_1 to sense the differential outputs. A_1 and A_2 are connected as unity-gain buffers to convey the differential input voltages on resistor R_1. Since the common-mode voltage cross R_1 is expected to be equal to each other, only differential current $i_x = (V_{inp} - V_{inn}) / R_1$ will flow through R_1. In order to apply the power-supply current-sensed technique, two current mirrors CM_1 (CM_1') and CM_2 (CM_2') are inserted to both positive and negative power-supply rails of A_1 (A_2), thus, i_x can be copied precisely to the output stage, which consists of A_3 (A_4) and R_2 (R_2'). A_3 (A_4) is connected as a trans-resistor to create a virtual ground at the outputs of $CM_{1,2}$ ($CM_{1,2}$') and convert i_x into voltage via R_2 (R_2'), generating the desired output voltage $V_{outp} = i_x R_2$ ($V_{outn} = i_x R_2$'). The overall differential voltage gain is given by $G_d = R_2 / R_1$ or R_2' / R_1.

In practice, process variation and mismatches will lead to non-zero common mode gain, yielding a finite CMRR that can be approximated by,

$$CMRR_{IA} \cong \frac{A_{d1}A_{d2}}{A_{d1} - A_{d1}A_{c2} + A_{c1}A_{d2} - A_{d2}}, \qquad (1)$$

where, A_{d1}, A_{d2} and A_{c1}, A_{c2} are differential mode and common mode gains of A_1 and A_2, respectively. With $CMRR_1 = A_{d1} / A_{c1}$ and $CMRR_2 = A_{d2} / A_{c2}$, (1) can be re-expressed as,

$$\frac{1}{CMRR_{IA}} \cong \frac{1}{A_{d2}} - \frac{1}{A_{d1}} + \frac{1}{CMRR_1} - \frac{1}{CMRR_2}. \qquad (2)$$

It indicates that $CMRR_{IA}$ not only depends on the CMRR of each active core, but also the *matching* of gain and CMRR [6].

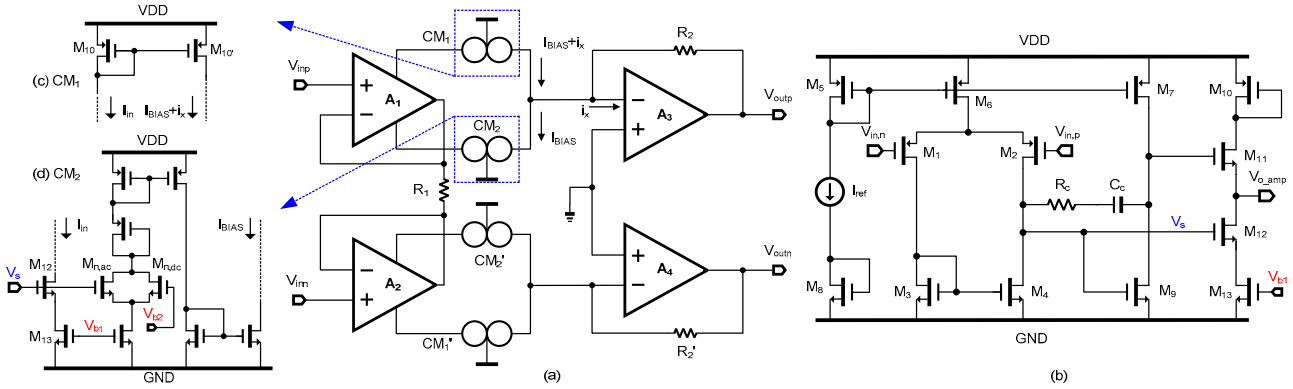

Fig. 2. (a) Current-conveyor-based CMIA. (b) Schematic of the OpAmp. (c) The Current mirror CM_1. (d) The Current mirror CM_2.

B. *Chopper Stabilization*

The CMRR of the CMIA can be degraded by the non-zero common-mode gain, which is either systematic (topology related) or random (matching related). Chopper stabilization in Fig. 3 has been an effective technique for suppressing the 1/*f* noise and dc-offset of differential circuits. Here, it is particularly relevant to improve the CMRR. The input chopper is transparent to the input common-mode signal. Thus, the common-mode signal will be converted to differential by the non-zero common-mode gain of the CMIA. The output chopper frequency-translates such a non-ideal differential-mode output signal to the chopping frequency such that it can be suppressed by the following LPF. This mechanism rejects the CMIA's 1/*f* noise and dc-offset as well.

C. *Circuit Implementation*

Figure 2(b) shows the schematic of the CMIA's OpAmps, which is of a two-stage topology with Miller compensation. The current mirrors are built on the output stages of A_1 and A_2. The input PMOS differential pair is of large *W/L* aspect ratio to minimize the 1/*f* noise. Table I summarizes the typical performance metrics of the employed OpAmp. A dc gain of 44 dB and a gain-bandwidth-product of 126 kHz fulfill the targeted specifications. Special attention has been paid to bias the OpAmp such that the impedance of its output is less sensitive to mismatch and process variations. Mismatch of this parameter can degrade the CMRR of the CMIA [7] and it is sensitive to R_1. The current mirrors also play a significant role in determining the CMRR. Figure 2 (c)-(d) shows their schematics. CM_1 is of the basic standard PMOS current mirror structure to copy the current through M_{10}, whereas CM_2 is capable of copying small ac current by a current-division technique; a transistor is split into two, i.e. $M_{n,ac}$ and $M_{n,dc}$. $M_{n,ac}$ is sized to have a very small trans-conductance g_m, such that a tiny ac current can be conducted. The bias current is conducted by $M_{n,dc}$. V_{b1} is the bias voltage of M_{13} and V_{b2} is the same dc voltage of V_s to bias $M_{n,dc}$. The copied current is further adjusted through M_{c1} and M_{c2} to improve the accuracy.

TABLE I.
SIMULATED OPAMP PERFORMANCE.

DC Gain	44 dB
3-dB Cutoff Frequency	850 Hz
Gain-Bandwidth Product	126 kHz
Phase Margin	70°
CMRR up to 3 kHz	100 dB
Power consumption at 3 V	4.2 μW

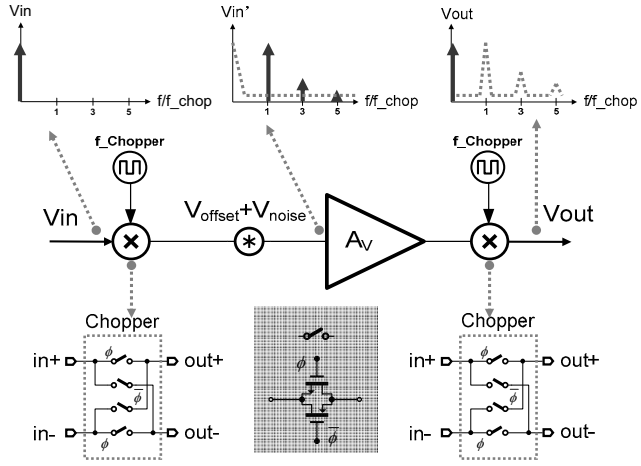

Fig. 3. Chopper stabilization for 1/f noise, dc-offset reduction and CMRR improvement.

III. GAIN-COMPENSATED SOURCE-FOLLOWER-BASED LPF

For a conventional MOS source follower, due to the transistors' bulk transconductance, the gain is less than unity, corresponding to a gain loss when it is employed to realize a LPF. Typically, the dc-gain loss is in the order of 3.5 dB for a subthreshold-biased NMOS source follower (NSF) biquad. In this work, a gain-compensation technique is proposed as depicted in Fig. 4. The 1st NMOS source follower (NSF) biquad is gain-compensated by adding a cross-connected differential pair, which provides an additional *gain* path to compensate the gain loss. Obviously, this gain path can degrade the good linearity of source-follower-based LPF. In order to balance the linearity and gain loss, the cross-connected differential pair is only applied to the NSF and is source-degenerated by R_{deg}. The 2nd biquad is a generic PMOS source follower (PSF), ensuring a good linearity.

The characteristic of the gain-compensated NSF biquad is analyzed by considering its small-signal half equivalent circuit as shown in Fig. 5, where g_{mn1}, g_{mn2}, g_{mp} are the trans-conductances

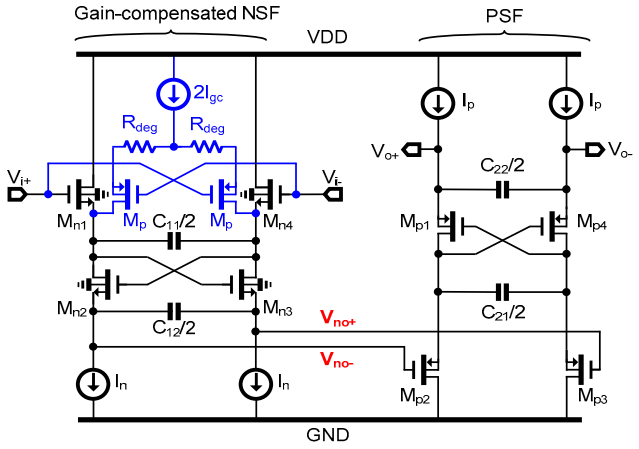

Fig. 4. Proposed 4th-order SFB LPF with gain-compensated NSF.

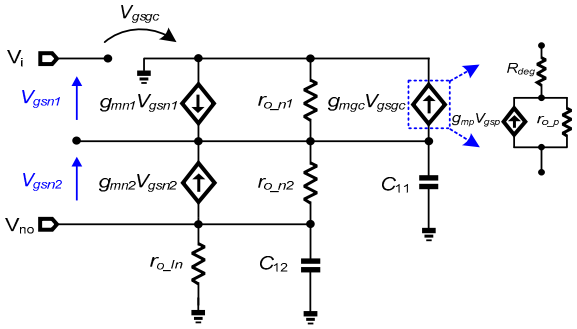

Fig. 5. Small-signal half-equivalent circuit of gain-compensated NSF.

of M_{n1}, M_{n2}, M_p, and r_{o_n1}, r_{o_n2}, r_{o_p}, r_{o_In}, are the output resistances of M_{n1}, M_{n3}, M_{gc}, I_n, respectively. Assuming the transistor's output resistance is much bigger than the reciprocal of its transconductance under the subthreshold bias condition, the transfer function of the NSF biquad is given by,

$$H(s) = -\frac{1+\frac{g_{mgc}}{g_{mn1}}}{s^2 \cdot \frac{C_{11}\cdot C_{12}}{g_{mn1}\cdot g_{mn2}} + s \cdot \frac{C_{12}\cdot g_{mn1} + (C_{11}-C_{12})\cdot g_{mn2}}{g_{mn1}\cdot g_{mn2}} + 1} \quad . \quad (3)$$

Where $g_{mgc} = \frac{g_{mp}}{1+g_{mp}\cdot R_{\deg}}$ due to the source degeneration of M_p.

Eq. (3) clearly shows that g_{mgc} can boost the dc gain of the biquad. The capability of gain compensation is mandated by the tradeoff between linearity, noise and power consumption. The angular pole frequency ω_0 is given by,

$$\omega_0 = 2\pi f_0 = \frac{\sqrt{g_{mn1}\cdot g_{mn2}}}{\sqrt{C_{11}\cdot C_{12}}}, \quad (4)$$

The cutoff frequency is proportional to the term $\sqrt{g_{mn1}\cdot g_{mn2}}$. To realize a low cutoff frequency, a low transconductance is desired to minimize the required capacitor size which can occupy a huge amount of silicon area for this ultra-low-frequency design. All transistors are in sub-threshold-biased region to minimize the transconductance g_m, which is given by,

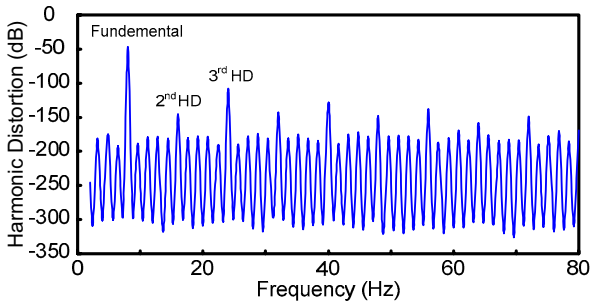

Fig. 6. Harmonic distortion with 5-$mV_{p\text{-}p}$ input @ 8Hz. The gain is set to 10 V/V; corresponding to a 50-$mV_{p\text{-}p}$ input at the LPF.

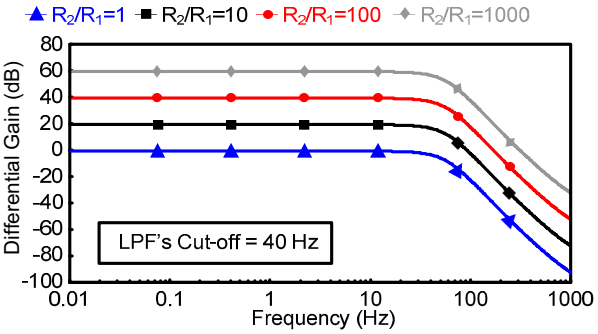

Fig. 7. Frequency response of the CMIA with 40-Hz LPF's cutoff.

$$g_m = \frac{I_D}{nU_T}, \quad (5)$$

where n is the subthreshold slope factor and is of a value close to 1.5; U_T is the thermal voltage and is around 26 mV at room temperature; I_D is the drain current. C_{11}, C_{12}, C_{21} and C_{22} are all differentially terminated to maximize the capacitance per unit area. In this work, the optimized I_D is 200 pA, resulting in ULP dissipation. The sum of all physical capacitances is minimized to an impressive value of 37 pF.

IV. Simulation Results

The readout front-end is designed and fully characterized in 0.35-µm CMOS with *Spectre* as the simulator. Figure 6 shows the harmonic distortion under a single tone test with an 8-Hz frequency and a 5-mV_{pp} amplitude. The linearity is limited by the 3rd harmonic which is 60 dB down from the fundamental. The variable-gain characteristic is demonstrated in Fig. 7, where the gain is set by the ratio of R_2 (R_2') and R_1. With the proposed gain-compensation technique, the gain loss of the LPF is reduced from 3.6 to 0.6 dB. Figure 8 shows the CMRR performance of the entire readout front-end. The CMRR is better than 100 dB up to 16 Hz, and better than 90 dB up to the cutoff frequency of 40 Hz. The noise performances of the CMIA at 0 and 20-dB gain levels are illustrated in Fig. 9(a). Due to the use of chopper stabilization, the input-referred noise voltage density is effectively suppressed to 248 (175) nV/√Hz at 0.01 Hz at 0 (20) dB gain. The chopper also reduces the 1/*f* noise corner frequency from 84 to 1 Hz. At 20-dB gain, the noise performance of the readout front-end with and without chopper is depicted in Fig.

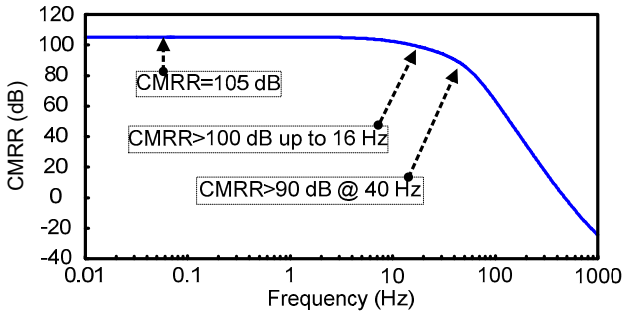

Fig. 8. CMRR of the entire readout front-end.

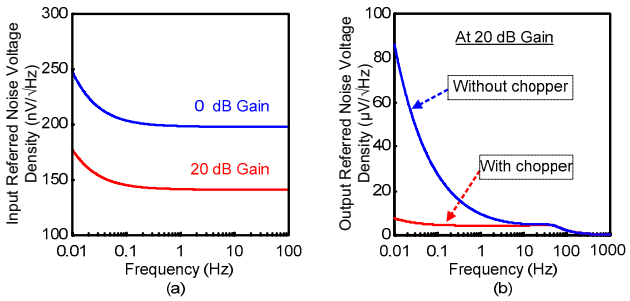

Fig.9. (a) CMIA's input-referred noise voltage density at 0-dB and 20-dB gain. (b) Readout front-end's output-referred noise voltage density with and without chopper at 20-dB gain.

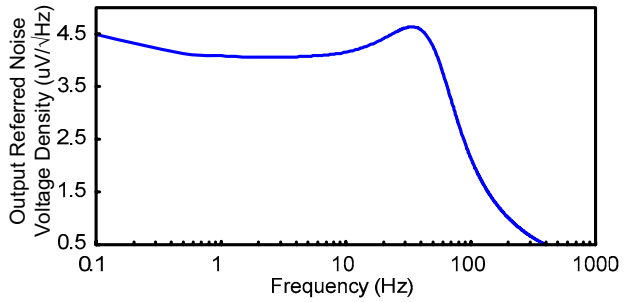

Fig. 10. LPF's output-referred noise voltage density.

9(b). The in-band output-referred noise voltage density is around 8μV/√Hz. The noise performance of the standalone LPF is shown in Fig. 10. Due to its simple hardware structure, the in-band output-referred noise voltage density is just 4.5 μV/√Hz. A performance summary of the entire readout front-end is given in Table II.

V. Conclusions

This paper has described a novel low-power EEG readout front-end. It is structured by a current-conveyor-based CMIA followed by a 4th-order SFB LPF with gain compensation. Chopper stabilization is applied to effectively suppress the 1/*f* noise and dc-offset while boosting the CMRR. The SFB LPF is biased in the subthreshold region. It achieves a huge time constant with small power and capacitor area. The LPF is constructed by two ULP SFB biquads in cascade. Since

TABLE II.
PERFORMANCE SUMMARY.

Supply Voltage	3 V
Technology	0.35 μm CMOS
Variable Gain (Via R_2 and R_2')	1, 10, 100, 1000 V/V
Gain-Bandwidth-Product (CMIA)	280 kHz
Input-Referred Noise Voltage Density (CMIA with Chopper)	248 nV/√Hz @ 0.01 Hz 197 nV/√Hz @ 100 Hz
CMRR	> 100 dB (0.01 to 16 Hz) > 90 dB (up to 40 Hz)
Lowpass Cutoff Frequency	40 Hz
Stopband Attenuation	70 dB / Decade
LPF HD_3 down from fundamental (with 50m V_{P-P} input @ 8 Hz)	61.6 dB
THD (with 8 Hz 5m V_{P-P} input, 10 V/V gain)	0.075%
Power Consumption	27.6 μW (CMIA) 4.3 nW (LPF)

nonlinearity is dominated by the 2nd biquad, gain-compensation is applied only at the 1st biquad, minimizing the gain loss to a sub-dB range (0.6 dB) while keeping a high dynamic range. The CMRR is 100 dB from 0.01 Hz to 16 Hz, and is 90 dB up to 40 Hz. The power consumption is minimized to 28 μW at 3 V.

ACKNOWLEDGEMENT

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