23.1 A 2.5V 57MHz 15-Tap SC Bandpass Interpolating Filter with 320MHz Output Sampling Rate in 0.35µm CMOS

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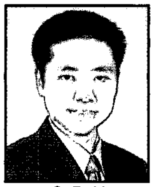

S-P. U

A 57MHz SC bandpass interpolating filter with 320MSample/s output is realized in 0.35µm CMOS for DDFS system. 15-tap FIR response is achieved with sampling rate increase and frequency upconversion by translating 22MHz 80MSample/s input to 56MHz 320MSample/s output. Dynamic range is 69dB (1%THD) and 61dB (1%IM3). The filter dissipates 120mW analog and 16mW digital at 2.5V supply.

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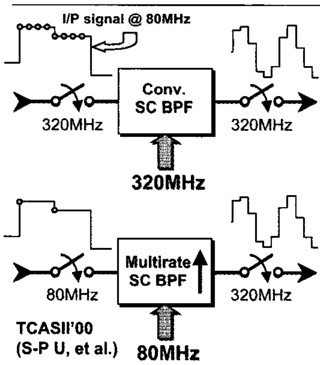
Outline

- Overview
- System Topology
- Design Challenges
- Circuit Implementation
- Measurements
- Summary

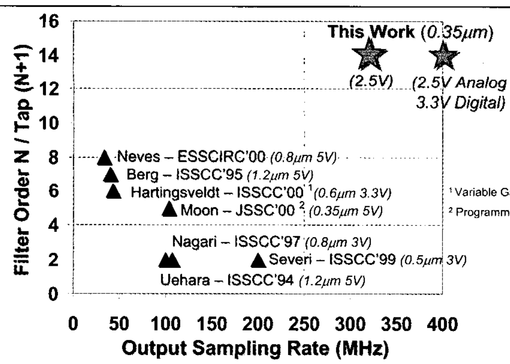
Conventional vs. Multirate Approaches



- High-speed operation (High power & large area)
- Limited circuit design headroom
- Low-I/P Sinx/x effect

- Low-speed filter core + A simple high-speed output commutator
- Enlarged circuit design headroom
- No Low-I/P Sinx/x effect

State-of-the-Art HF CMOS SC Filters

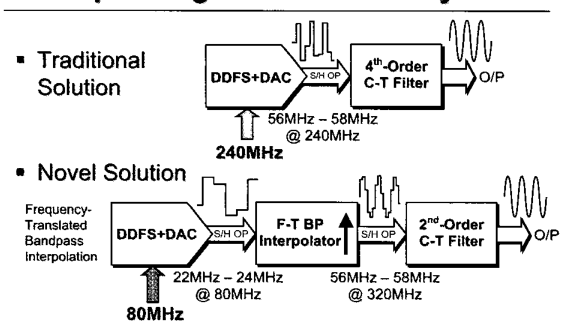


Design Challenges

- High-Speed Output
- High Filter Order
- Capacitor/Path Matching
- Fixed Pattern Noise
- Phase Skew
- Digital Coupling Noise

Interpolating BPF for DDFS system

- Traditional Solution
- Novel Solution

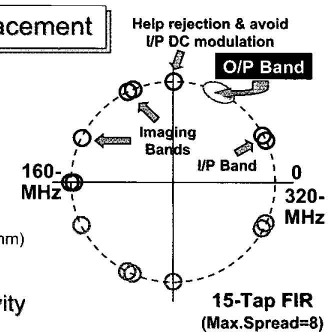


Lower speed of DDFS & DAC + Simplify C-T Post-Filtering

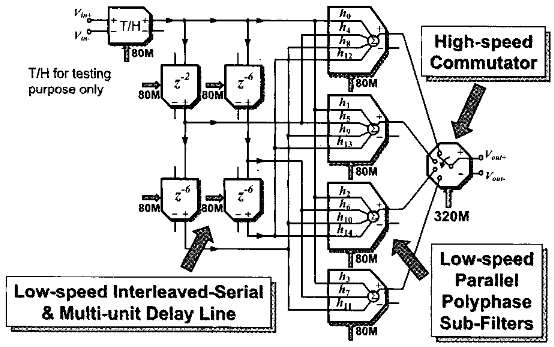
Multi-notch FIR Transfer Function

Optimum Zero-Placement

- Avoid High-Q IIR Function (Q>20, no f_s control for f_o)
- Avoid High-Order Traditional FIR Design (N>30 & 40 for Optimal & Window algorithm)
- Optimize Spread, Order and Sensitivity



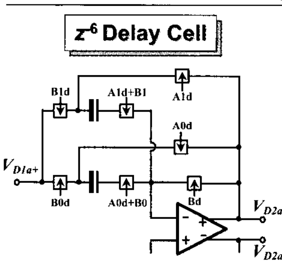
Improved Multirate Polyphase Structure

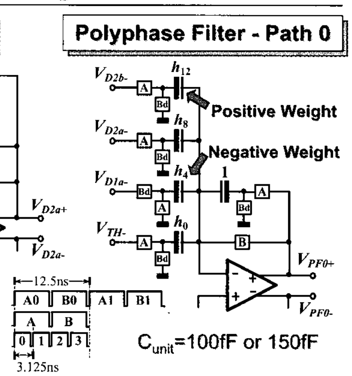


Switches & I/O Circuitry

- NMOS switches only
  - VCM=0.95V
  - $(W/L)_{max}$ =53/0.3, $(W/L)_{min}$ =5/0.3
- Testing-purpose I/O
  - I/P T/H stage @ 80MHz
  - O/P Level-shifter
  - O/P Wideband PAD & 50Ω driver

Autozeroing Filter Core





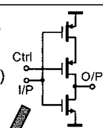
- Rotating-switching
- Mismatch-insensitive
- Offset-compensated

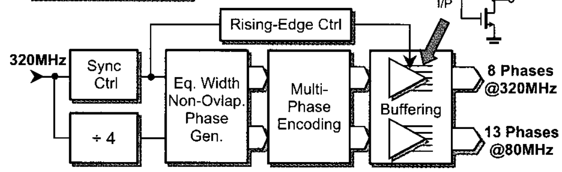
C_{unit}=100fF or 150fF

Low-Skew Phase Generator

SFDR>60dBc ⟹ σ<5ps

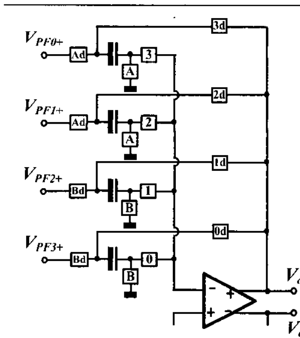
- Random process mismatch Ctrl
(Edge-triggering buffers)



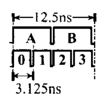


- Design systematic mismatch Ctrl
(Logic design for equal propagation-gate-delay)
- dI/dt supply-noise mismatch Ctrl
(Individual-on-chip-VDD supply for 320MHz & 80MHz)

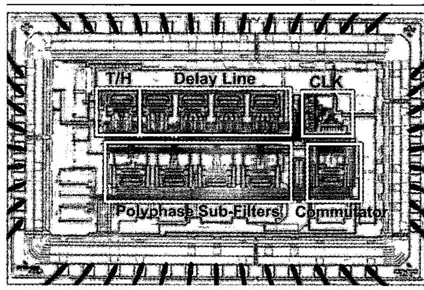
Output 4-path Commutator



- Full-output period for settling (≈ 2.4ns)
- Large Feedback factor (>0.5)
- Mismatch-insensitive
- Output-glitches-reduced
- Double-sampling SC CMFB



Die Micrograph

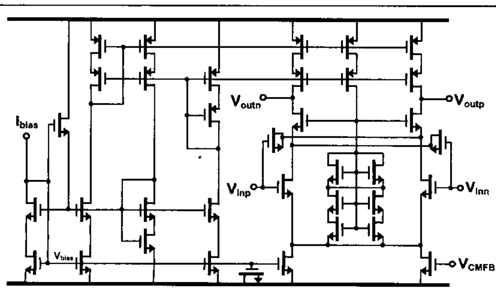


0.35μm
2P3M
CMOS

$2mm^2$
Active Area

- Separate VDDs with Common GND & on-chip Decoupling
- Common-centroid, Dummy-periphery, Symmetric layout, Guard ring, Ample contacts, Multi-D shielding

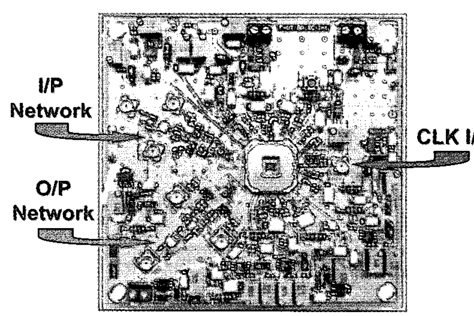
OP AMP Structure



Single-stage Telescopic with wide-swing biasing

(OP AMP_{fast}: Gain=66.5dB, GBW=1GHz@2.5pF, t_{settl}=1.6ns@1V step, SR=1.7V/ns, 12mW@2.5V)

Measurements – Testing Board



4-Layer PCB Board (Top View)

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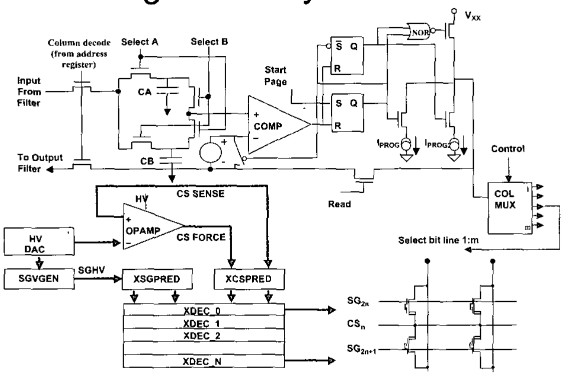
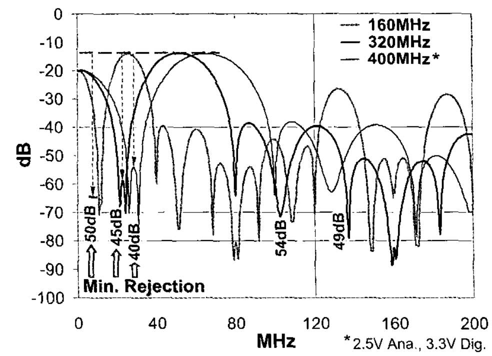
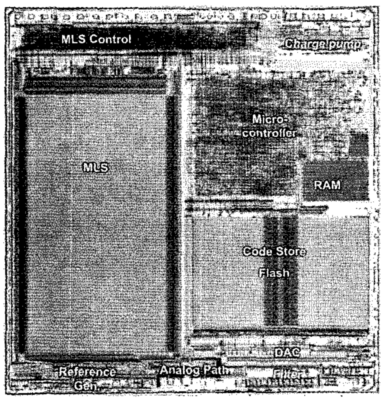
Program Verify Circuit

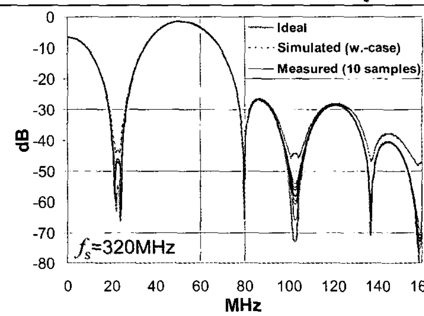


Measurements – Gain Response I





Measurements – Gain Response II



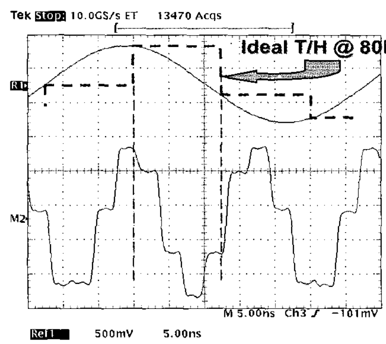
- Passband Ripple < 0.6dB, 3σ = 0.02dB
- Stopband Rejection > 45dB, 3σ = 0.45dB @ 22-24MHz band

WTS701 Device Summary

- Single Chip text-to-speech solution.
- Available languages: English and Mandarin
- PWM digital audio interface
- Speaker Driver
- SPI serial control interface
- Area: 8.7 x 9.2 mm
- 0.5μm triple poly double metal Flash CMOS
- MLS Memory 6M cells
- Digital Flash 300k Bytes
- RAM 2k
- Vcc 2.7– 3.3V.
- Isb < 10μA

For more information see http://www.winbond-usa.com/

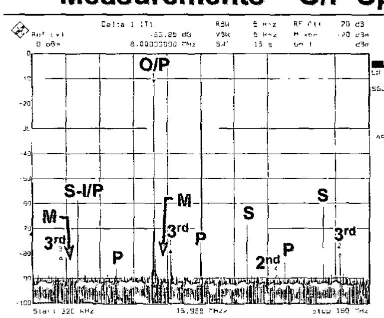
Measurements – I/O Waveform



Input: 22MHz, $1V_{p\text{-}p}$

Output: 58MHz sampled at 320MHz

Measurements – O/P Spectrum



$HD2_{max}$=-78dBc
$HD3_{max}$=-67dBc
THD=-62.4dB

P_{max}=-70dBc
P_{total}=120μV_{rms}

M_{max}=-73dBc

- Input: 22MHz, $1V_{p\text{-}p}$
- Output: 58MHz sampled at 320MHz

S: Signal or its sampling images
P: Pattern Noise Tone
M: Modulation sideband by phase skew and parallel mismatches

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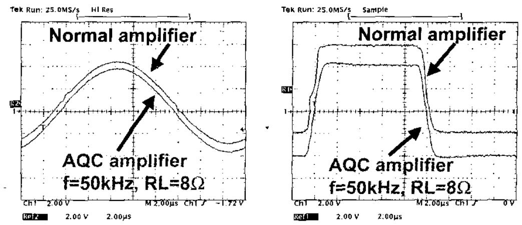
Measurements Summary II

Technology	0.35μm CMOS		
Filter order	15-tap FIR BPF		
Output Sampling Rate	400MHz	320MHz	160MHz
Input Sampling Rate	100MHz	80MHz	40MHz
Center Frequency (f_{center})	71.25MHz	57MHz	28.5MHz
OIP3	22.5dBm	23dBm	26.4dBm
CMRR (f_{in}=f_{center})	53dB	54.5dB	56dB
Supply (Analog, digital)	2.5V, 3.3V	2.5V, 2.5V	2.5V, 2.5V
Analog Power	120mW	120mW	59mW
Analog Power / Tap	8mW	8mW	4mW
Digital Power	37mW	15.8mW	7.8mW
Active Core Area	2mm² (T/H + BPF + CLK)		

Conclusions

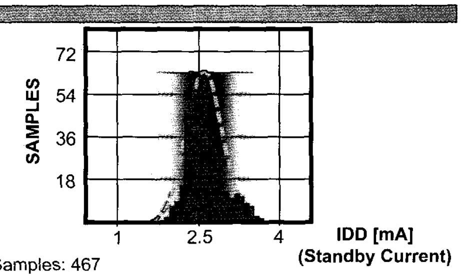
- **A 2.5V HF SC interpolating BPF in 0.35μm CMOS**
  - High center frequency: 57MHz (71.25MHz)
  - High output sampling rate: 320MHz (400MHz)
  - High filter order: 15-tap FIR
  - High dynamic range: 69dB (1%THD), 61dB(1%IM3)
  - Low pattern noise: <-70dBc, (120 $\mu V_{rms})_{Total}$
  - Low mismatch-modulated effect: <-72dBc (by phase skew and parallel-path mismatches)
- **A novel scheme for DDFS systems**
  - Sampling rate increase + Frequency-translated filtering
  - Suitable for other high-speed Analog Front-End

Experimental Results(1)



⇨IDD=2.6mA @VDD=5V
⇨THD=0.1% @ Po=1W, RL=8Ω, f=1kHz, VDD=5V
⇨THD=0.3% @ Po=1W, RL=8Ω, f=20kHz, VDD=5V

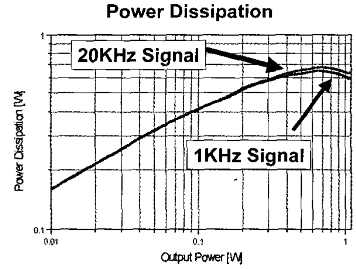
Experimental Results(2)



⇨ Samples: 467
⇨ Average: 2.6mA (Spec.: 2.5mA)
⇨ Standard deviation: 0.34mA
⇨ Buffers offset & AQC effect on IDD → ignorable

Experimental Results(3)

Power Dissipation



⇨ Power increases at 20kHz since AQC is turned on.

Summary

Supply voltage:	**2.6 ~ 5.5V**
IDD:	**2.6mA @ VDD=5.0V**
Offset:	**5.1mV @RL=8Ω**
THD+N:	**0.1% @ Po=1W, f=1kHz**
	0.3% @ Po=1W, f=20kHz
PSRR+:	**71dB @ 1kHz**
Maximum Efficiency:	**65.1%**
Process:	**0.8μm BiCMOS (1 poly, 2 metals)**
Chip Size:	**1810 x 1580 μm²**