Split-Based Time-interleaved ADC with Digital Background Timing-skew Calibration

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***Abstract*— This paper presents a split-based time-interleaved (TI) ADC with digital background timing calibration for wideband applications. Each interleaved channel uses a split ADC, which adds a dimension for timing-skew error detection and correction. Thus, the complexity of digital post-processing is greatly relaxed without the use of any dummy channel. The behavioral simulations show a 28 dB and 35 dB improvements in signal-to-noise plus distortion (SNDR) and spurious-free dynamic range (SFDR) respectively, after adopting the proposed timing skew correction for a 10-bit 4GS/s ADC example.**

Keywords—ADC, converters, digital background calibration, time-interleaving, split-ADC, timing.

I. Introduction

As modern wired, wireless and optical communication systems evolve toward more advanced modulation schemes, there exists a pressing need for a power efficient ADC operating at multi-to-tens-GS/s with 8-12 bits resolutions [1][2]. Time-interleaving (TI) provides an effective means for these applications when the performance of single-channel ADC becomes limited by physical technology limit [3]. However, analog parallelism suffers from channel mismatches, including dc offset, gain, and timing mismatches, which introduces additional errors and degrading the accuracy of analog-to-digital conversion [4]. Compared with offset and gain mismatches which can be readily removed by long-term averaging and correction in the digital domain, timing skew would generate a signal-dependent error in terms of both amplitude and frequency which increase the complexity of calibration.

Some correction methods of timing skew errors, including in the analog [1][3][5][6] or in the digital domain [2][7], have been proposed to overcome this limitation. However, analog correction suffers from the poor feedback-induced stability hazard; furthermore, the controlled delay line introduces additional jitter which will degrade the SNR at higher frequency. Digital-domain correction takes advantage of technology scaling, but complex slope-extraction digital filter [2][7] limits the signal bandwidth, and the costs of other dummy extra converters [5] in power consumption and area could be high.

A split-based time-interleaved ADC with digital background timing mismatch calibration is presented in this paper. The proposed correction does not require digital filters and, therefore, allows a low-power, low complexity implementation; furthermore, thanks to the proposed architecture, no dummy converters are required.

II. Proposed Split-based Architecture With Timing Skew Calibration

A. Split-based Time-Interleaved ADC Architecture

Fig. 1(a) shows the block diagram of the proposed time-interleaved ADC. The effective conversion rate of this ADC (f_s) can be expressed as $f_s = f_c \times M$, where f_c and M are the conversion rate of each-channel and the number of the interleaved channels, respectively. Each channel is split into two sections: A and B, converting the same input but producing their output codes y_A and y_B [8]. Φ_i is the sampling clock of the i th sub-ADC, where $i = 1, \ldots, M$, and each channel has two identical clocks Φ_{iA} and Φ_{iB}, which samples at a rate of f_s/M.

Fig. 1(b) illustrates the timing diagram of the proposed TI ADC. The sampling period of time-interleaved ADC and the M sub-ADCs are T and $M \cdot T$, respectively. ΔT_i, is the small sampling-time difference between each split part, which is introduced (can be intentionally) by timing mismatches between the sampling switches and clock buffers.

B. Proposed Timing-skew Correction Algorithm

We first describe the method for two interleaved channels. Supposing for example, as shown in Fig. 2, channel-1 is split into channel-*1A* and -*1B*, sampling the input signal $x(t)$ at t_{1A} and t_{1B}. Similarly, channel-2 samples at t_{2A} and t_{2B}, where ΔT_{1A}, ΔT_{1B}, ΔT_{2A} and ΔT_{2B} are the offsets from their ideal values t_1 and t_2.

Then we choose the average value of y_{1A} and y_{1B} as the calibrated output of channel 1:

$$y_{1,cal}[k] = \frac{y_{1A}[k] + y_{1B}[k]}{2}. \quad (1)$$

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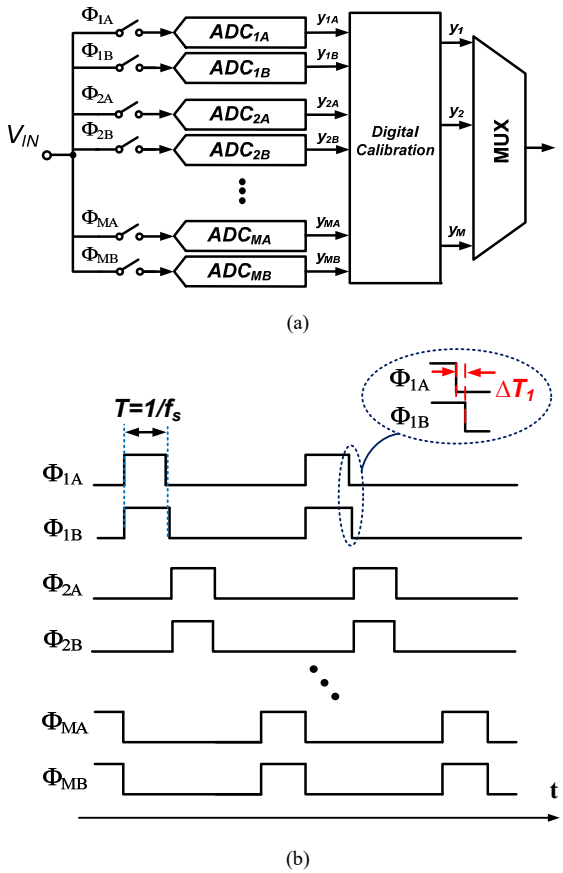


(a)

(b)

Fig. 1. (a) Block diagram of the proposed time-interleaved Split ADC, and (b) simplified timing diagram.

Assuming ΔT_1 is a short timing delay and $\Delta T_{1A} = \Delta T_{1B} = \Delta T_1/2$, as shown in Fig. 2, then we have $y_1[k] \approx y_{1,cal}[k]$, respectively.

For channel-2, similarly, using $y_{2A}[k]$ and $y_{2B}[k]$, we can obtain the approximation of an ideal sample. Although the timing skew between each channel is unknown, we can use the same equation to obtain the approximate value no matter extrapolation or interpolation, as shown in Fig. 3:

$$y_{2,cal}[k] = y_{2A} - \frac{y_{2A}[k]-y_{2B}[k]}{t_{2A}-t_{2B}} \cdot t_{2A}. \qquad (2)$$

Here, we choose t_2 as the reference origin of t-axis, and t_{2A}, t_{2B} can be a positive or a negative value.

However, the value of the timing skews $t_{1A,B}$ and $t_{2A,B}$ need to be determined. Fortunately, it only requires the relative value of t_{2A} and t_{2B} from the equation (2). By using the timing skew detection method [6] to process the outputs of ADCs, it can be shown that it depends on the difference between expected values of $\left(y_1[k] - y_{2A,B}[k]\right)^2$ and $\left(y_1[k+1] - y_{2A,B}[k]\right)^2$ as follows:

$$-4 \cdot t_{2A,B} \cdot \frac{dR}{d\tau} \approx E\left[\left(y_{1,cal}[k] - y_{2A,B}[k]\right)^2\right] - E\left[\left(y_{1,cal}[k+1] - y_{2A,B}[k]\right)^2\right] \qquad (3)$$

where $R(\tau)$ is the autocorrelation of $y(t)$. To simplify the digital algorithm, we can just calculate the absolute value of each difference instead [6].

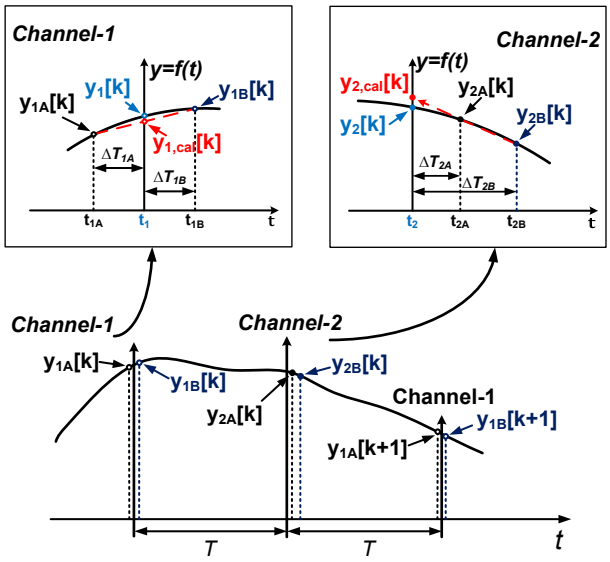
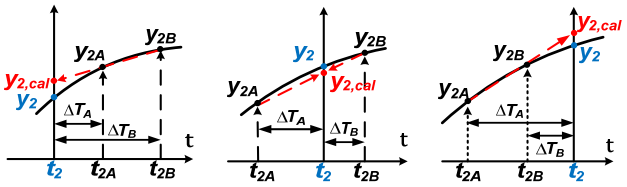


Fig.2. Two-channel ADC: waveform illustrating the effect of timing mismatch.

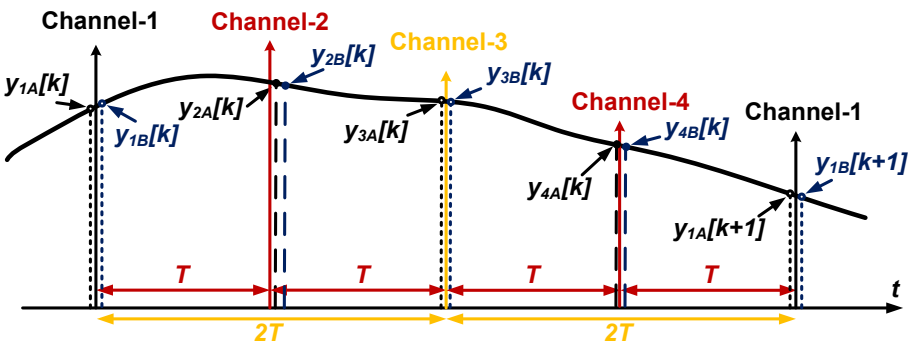


(a) Extrapolation (b) Interpolation (c) Extrapolation

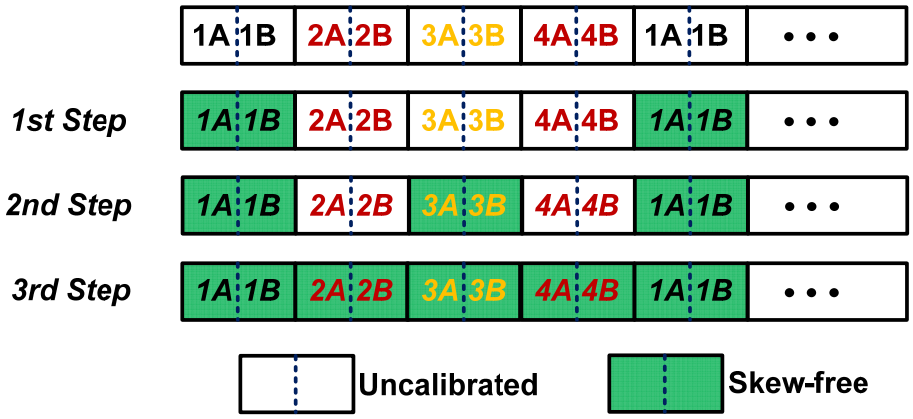
Fig. 3. Channel 2: three-types of the relationship between the ideal sample and practical sample.

C. *Extension to multiple interleaved channels*

One can further extend the above analysis to multiple channels ADC accordingly. To this end, as Fig. 4(a) shows the waveforms for 4-channel interleaved case; the first channel's sampling time is considered as the reference which is calculated by the equation (1). Then the timing skew of channels 2, 3, and 4 can be evaluated based on channel 1. This calculation consists of three steps: 1) average the individual spilt-channel values as the calibrated output of channel 1; 2) detect the mismatches between channel 3A, 3B and channel 1 then calculate the output of channel 3 by equation (2); 3) detect and correct the other two channels timing errors based on the calibrated channel 1 and channel 3.



(a)



(b)

Fig. 4. Four channel ADC: (a) waveform showing the effect of timing error and (b) calibration sequence.

III. Practical Issue in Calibration

A. Design Considerations of Adding a short Time Delay

This timing skew correction is based on different split channel samples at different time points. To avoid $y_A[k] = y_B[k]$, a short constant time delay ΔT_j needs to be inserted between Φ_{jA} and $\Phi_{jB}, j = 2, \dots, M$. And it is crucial to choose a proper value because it impacts the skew range and approximation error. Too small constant time delay will decrease the detectable skew range, but too large will degrade the accuracy of calibration. According to Talyor expansion, and keeping only first order and second order terms, we can calculate the approximation error

$$\varepsilon = y_j[k] - y_{j,cal}[k] \approx -\frac{1}{2} y_j''[k] \cdot \Delta t_{jA} \cdot \Delta t_{jB} \qquad (4)$$

where $y_j''[k]$ is the second order derivative of the input signal, and Δt_{jA}, Δt_{jB} are the time delay between the ideal samples.

B. Impact of Quantization Error and Thermal Noise

The analysis in section II is based on the ideal ADC raw output and it is necessary to discuss the impact of quantization error and thermal noise. For the first channel, it is similar to the traditional split ADC [8], the overall noise is the same as the traditional structure by averaging the two parts of digital codes, even the noise of each part is multiplied by $\sqrt{2}$. This is different for the other interleaved channels due to the digital process that corrects the timing error. Here we consider the digital code of the channel -j output $y_{jA,B}$ as

$$y_{jA,B} = x_{jA,B} + e(N) \qquad (5)$$

where $x_{jA,B}$ are the samples of the input signal at $t_{jA,B}$, and $e(N)$ includs the quantization error and thermal noise. Combining with (2) and (5), and assuming those errors and noises are uncorrelated with the signal, we can write

$$y_j[k] = \alpha_A \cdot x_{jA}[k] + \alpha_B \cdot x_{jB}[k] + \beta \cdot e(N) \qquad (6)$$

where $\alpha_A = \frac{t_{jB}}{t_{jB} - t_{jA}}$, $\alpha_B = \frac{-t_{jA}}{t_{jB} - t_{jA}}$, and $\beta = \sqrt{\frac{\left(t_{jB}^2 + t_{jA}^2\right)}{\left(t_{jB} - t_{jA}\right)^2}}$.

The effect of the noise can be reduced if the coefficients of $e(N)$ are set properly. One can try to reduce the value of β, which is determined by the relative value of $t_{jA,B}$. As shown in Fig. 3, the case of interpolation can keep $\beta < 1$.

IV. Simulation Results

The behavioral simulation of a 4-GS/s, 10-bit 4-channel split-based TI ADC has been performed in MATLAB with a

behavioral model based on a 65nm CMOS process with $1.2V$ supply, and an ADC input full scale set to $1.2V_{pp}$. To verify the method analyzed in Section IV, a kT/C thermal noise (equivalent to a *180fF* sampling capacitor) has been added to the input signal, for each split-side of one sub-ADC (it means the total sampling cap of each channel is *360fF*), degrading the SNR from the ideal value of 62 dB by 1 dB due to the thermal noise. The timing skew error range is approximately $\pm 5\,ps$ from the published works [1] and [3] in the same process. Without loss of generality, we set the timing skew t_s of 2nd, 3rd, and 4th channel to -3ps, 3ps and 4ps, respectively.

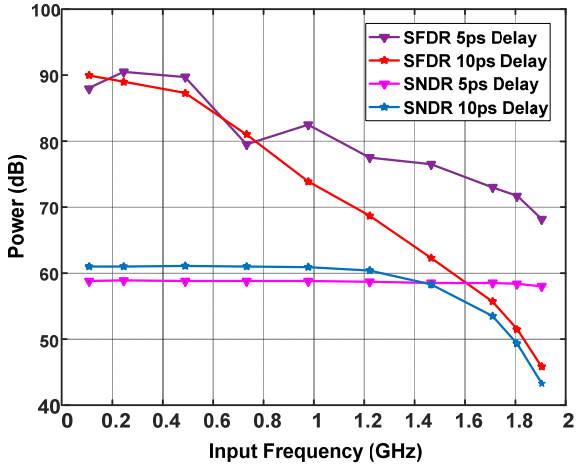


Fig. 5. The overall dynamic performance of the ADC array split parts of sub-converter with delay 5ps time and 10ps.

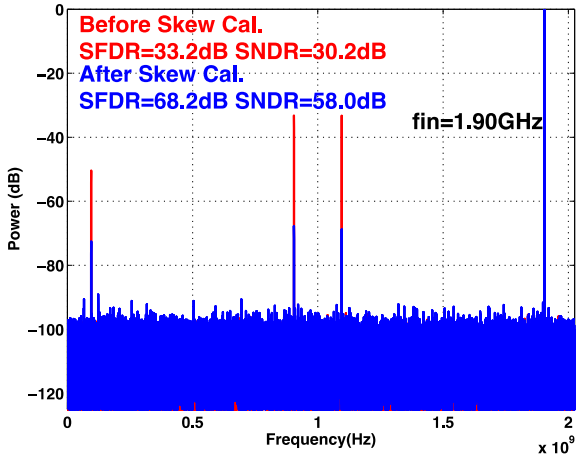


Fig. 6. Output spectra of ADC, before timing calibration vs. after timing calibration.

As analyzed in Section III, the value of added time delay ΔT_j impacts the SNDR of the overall ADC by the accuracy of calibration, the quantization error, and thermal noise. Fig.5 shows the overall dynamic performance of the ADC array with different time delays ΔT_j. A larger time delay like 10ps has an improved noise performance at a low input frequency, and it keeps the SNDR about 61dB when the input frequency is lower than 1.2GHz. However, the accuracy of timing calibration will decrease the dynamic performance at a higher frequency dramatically.

On the other hand, a smaller 5ps time delay achieves an excellent performance at a higher frequency, though it will degrade the SNDR from ideal 61dB by 2dB due to the drop of SNR. Considering of the wideband performance of converters; we set the constant timing delay to 5ps. Fig. 6 shows the ADC output spectrum with and without timing compensation techniques while the frequency of a sinusoidal input is 1.90 GHz. Fig. 6 shows the enhancement of the SNDR and SFDR by 27.8 dB and 35 dB.

V. Conclusion

This paper proposes a new TI ADC architecture and an efficient digital background timing-skew calibration algorithm, which avoids extra dummy ADCs and complex digital filters when compared with previous works. The calibration enhanced the SNDR by 27.8 dB at Nyquist for a 10-bit 4GS/s ADC example. Moreover, the concept of split-based TI ADCs could be extended to multiple interleaved channels.

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