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An Integrated DC-DC Converter with Segmented Frequency Modulation and Multiphase Co-Work Control for Fast Transient Recovery

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***Abstract*— This paper presents a fully integrated VCO-based switched-capacitor (SC) DC-DC converter in 65 nm CMOS. We propose two transient-enhancement techniques: segmented frequency modulation (SFM) and multiphase co-work control (MCW) to reduce the latency of the VCO-based control loop and shorten the SC DC-DC converter response time. We design a 15-phase interleaved converter to support an output voltage of 1 V from a 2.4 V input supply, delivering up to 138 mA of load current, which takes only 25/29 ns for output voltage recovering to the steady state from heavy-to-light/light-to-heavy load transients, respectively. It obtains a peak efficiency of 82.8 % and keeps the efficiency above 80 % from 31 mA to the maximum load current. The SC DC-DC converter chip occupies 0.61 mm^2, and its output power density is 240 mW/mm^2.**

Keywords*— *SC DC-DC converter, fully integrated, switched-capacitor, voltage-controlled oscillator (VCO).

I. INTRODUCTION

Fully integrated switched-capacitor (SC) DC-DC converters have increasingly proven their advantages while achieving high-conversion efficiency and generating different supply voltage domains on-chip with few shared voltage supply pins [1]-[5]. Multiphase interleaving of SC DC-DC converters can adjust the number of switching phases along with a wide range of load currents. Besides, multiple phases allow the control-loop to respond at every phase that is a fraction of the switching period [3], thus having a strong ability to achieve a fast load transient response. However, the response of the control loop is not able to provide the fast recovery requested to the converter output during load transition. As shown in [2], the VCO, whose frequency is proportional to the charge pump integrator voltage, determines the clock frequency of the multiphase generator. To accomplish both the rapid detection and fast recovery, [2] uses an additional bypassing control path to handle the load transition specifically. The frequency of the VCO-based clock generator was set to the maximum immediately after detecting an undershoot. However, for limited light-to-heavy load transition, such brute-force action caused the excessive switching of the SC array that exceeds the frequency required by the corresponding steady-state load current. Consequently, after the undershoot is recovered, a new overshoot is generated due to the overcharged voltage of the charge pump integrator which prolongs the total load transient recovery time [2].

The circuit described in this paper uses a segmented frequency modulation technique (SFM) and a multiphase co-work scheme (MCW) for the multi-phase SC DC-DC converter to improve the transient recovery speed during light-to-heavy and heavy-to-light load transients, thus achieving smooth and fast control at the same time. The details will be described next.

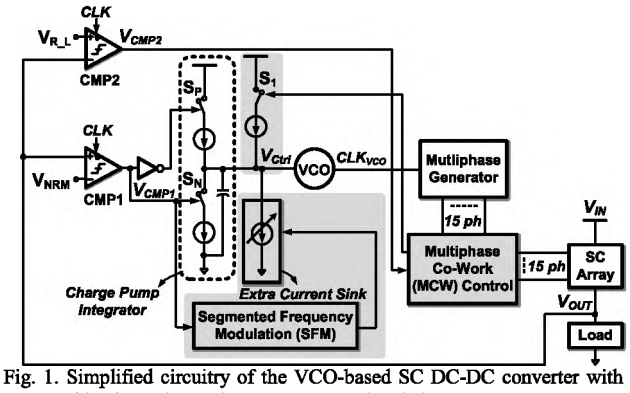

Fig. 1. Simplified circuitry of the VCO-based SC DC-DC converter with proposed load transient enhancement control techniques.

II. PROPOSED LOAD TRANSIENT RECOVERY SCHEMES

Fig. 1 depicts the simplified block diagram of the proposed VCO-based SC DC-DC converter. It is based on the implementation in [4], with the CMP1, the charge-pump integrator and the VCO forming the primary control path to drive the multi-phase clock generator, and the CMP2 providing the brute-force path for undershoot detection. This paper introduced two extra blocks for the load transient enhancement control, i.e., a segmented frequency modulation (SFM) control with extra current sink control and a multiphase co-work (MCW) control circuit. These two additional techniques relaxe the limitation outlined in [2].

A. Segmented Frequency Modulation (SFM)

Fig. 2 shows the circuitry of the proposed SFM modulator. It consists of a pulse counter, a 2-bit decoder, three switches S_{X0}, S_{X1}, S_{OV} and three binary weighted extra sink current branches. The pulse counter accumulates the output states of the CMP1 in each comparison cycle. If the load current changes from heavy-to-light, it generates an overshoot at the output that switches the CMP1 to 1 (V_{NRM} is the detection threshold). When the sum of pulse counts is larger than a given number, an overshoot detection signal V_{SIG} changes from low to high and turns on the switch S_{OV} which increases the sink current of the charge pump integrator. Depending on the degree

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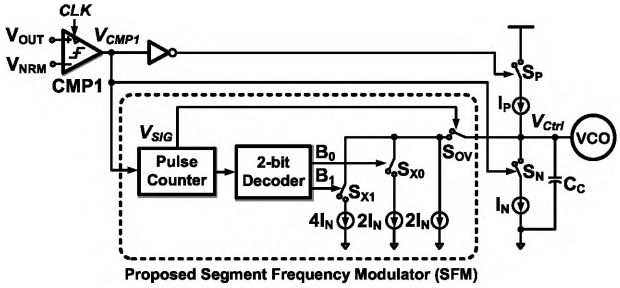

Fig. 2. Circuitry of the proposed segment frequency modulator (SFM).

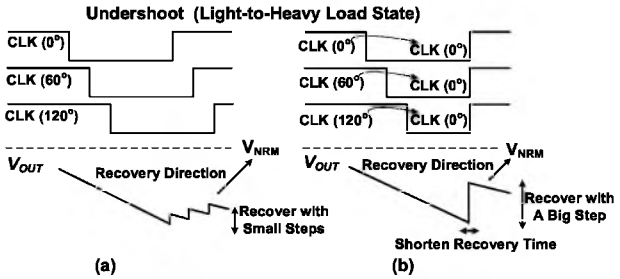

Fig. 3. Output of a 3-phase SC DC-DC converter in light-to-heavy load transient with (a) normal phase interleaving, and (b) MCW schemes.

of overshooting, up to an 8x additional sink current can be supported. This additional sink current can discharge the VCO control voltage V_{CTRL} quickly. Actually, the switching frequency of a VCO-based SC DC-DC converter scales with the load current. Therefore, a fast recovery time denotes speed in turning down the switching frequency for load step-down.

B. Multi-phase Co-Work (MCW) Technique

The multi-phase interleaving technique can reduce the output ripples of the DC-DC converter while avoiding a dedicated output decoupling capacitor [3]. Fig. 3(a) gives an example of the output voltage of a 3-phase interleaved SC DC-DC converter. The ripples of V_{OUT} decrease by a factor of 3 because of 3 channels interleaving, which also imposes a slow transient recover due to the reduced voltage steps. This work uses the MCW technique depicted in Fig. 3(b), which allows simultaneously ripple reduction and fast transient recovery in light-to-heavy load transition. The solution aims to synchronize the selected interleaving multiple-phase SC channels to provide an immediate larger energy step to the load. Indeed, by increasing the energy supply of the multi-phase SC network over time, the load transient recovery speed can be enhanced within a short period.

III. Measurement Results

The proposed DC-DC converter is implemented in a 65 nm CMOS process, with an active area of 0.61 mm^2 (Fig. 4(a)). An on-chip load current generator implemented with a programmable PMOS array can adjust the equivalent width of the PMOS devices to obtain correct I-V measurements during the load transient.

In the measurement, we set the nominal voltage V_{NRM} =1 V, and the undershoot-detection threshold V_{R_L} =0.9 V. The loop response time is within 5 ns, with the VCO switching

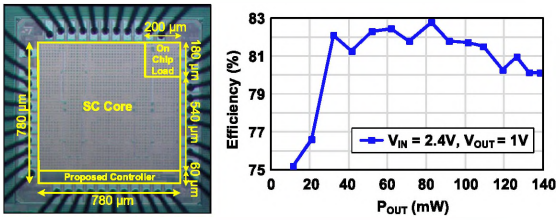

Fig. 4. (a) Chip photo, (b) Measured efficiency vs. output power.

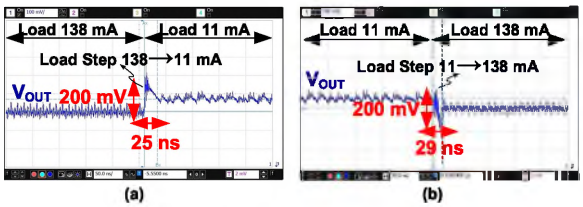

Fig. 5. Measured output voltage waveforms during (a) heavy-to-light load transition and (b) light-to-heavy load transition.

TABLE I: Performance Summary

Technology	65 nm	Max. out Power	138 mW
Topology	1/2 SC	Active Area	0.61 mm^2
Interleave Phase	15	Power Density	240 mW/mm^2
Capacitor Type	MOS	Peak Efficiency	82.8%
C_{fly} / C_{out}	2.56 nF / 0	Load Transient Step	11<->138 mA
SC Frequency	1 - 250 MHz	Light-to-Heavy Recovery	25ns, 5.1mA/ns
V_{IN} / V_{OUT}	2.4 V / 1 V	Heavy-to-Light Recovery	29ns, 4.38mA/ns
Ripple	55 mV	Controller Area Overhead	7.7%

frequency ranging from 1 MHz to 250 MHz for the entire load range, while the clock frequency of the comparators is 1.5 GHz. Fig. 4(b) shows the measured efficiency of the converter when V_{IN} = 2.4 V and V_{OUT} = 1 V. The load current sweeps from 11 mA to 138 mA. The power efficiency is higher than 75 % at light load. From 31 mA to 138 mA the efficiency exceeds 80 % with a peak of 82.8 % at 80 mA.

Fig. 5(a) shows the output voltage waveforms during heavy-to-light load (138 to 11 mA) transient. The SFM technique helps to improve the recovery speed as low as to 25 ns. Fig. 5(b) shows the waveforms during light-to-heavy load with a transient from 11 mA to 138 mA. The MCW helps to improve the recovery speed to 29 ns. These results confirm the effectiveness of the proposed SFM and MCW control techniques. Table I shows the performance summary. Without the use of deep-trench capacitors, the circuit attains a fast recovery and the output power density of 240mW/mm^2.

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