CCM Operation Analysis and Parameters Design of Negative Output Elementary Luo Converter for Ripple Suppression

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***Abstract*— This paper presents the DC analysis of the Negative Output Elementary Luo Converter (NOELC), which includes the continuous-conduction mode (CCM) voltage gain and the boundary condition between the CCM and the discontinuous-conduction mode (DCM). The main features of the NOELC are the high gain with small ripple and the reverse output. Additionally, we address the parameters design of the NOELC and propose an output voltage ripple estimation method. Through MATLAB Simulink simulation, we further demonstrate that the parameters design and the output voltage estimation method can achieve more accurate results when compared with those from the conventional one.**

Keywords—Continuous-conduction mode (CCM); Luo converter; parameter design; voltage ripple

I. INTRODUCTION

PWM dc-dc power converts are widely used in different applications such as renewable energy, computer systems, power supply for portable devices and smart wearables, etc. [1, 2]. Among them, applications in integrated circuit such as audio amplifier, signal generator, double-ended sensors, LCD biasing and light-emitting diode power saving require negative output dc-dc converters [3-8]. A buck-boost converter, for example, can provide inverse output and reach a large gain by varying the duty cycle. However, its output voltage ripple is large and depends on the load current [6]. The larger the load current, the larger the output voltage ripple. The negative output elementary Luo converter (NOELC) can solve the aforementioned problem by adding an output LC filter to the buck-boost converter [9]. Existing papers [9-12] aim to present the control method, its principle and integrations of the Luo converters. Nevertheless, although the output voltage ripple approximation method is presented in [9], it is not accurate and satisfactory as we'll explain here. Hence, we'll propose the parameters design of the NOELC, with a more accurate output voltage ripple estimation method. In Section II, we'll introduce the DC analysis including the continuous-conduction mode (CCM) voltage gain and the boundary between CCM and the discontinuous-conduction mode (DCM). After that, the parameters design of the NOELC will be presented, followed by an output voltage ripple estimation method in Section III. Consequently, the output voltage ripple can be suppressed by an appropriate design of the parameters. To verify such design and output voltage estimation method, we'll compare the simulation results with the conventional method using MATLAB Simulink in Section IV. Finally, we'll draw the conclusions in Section V.

II. DC ANALYSIS OF NEGATIVE OUTPUT ELEMENTARY LUO CONVERTER (NOELC)

Fig. 1 shows the circuit configuration of a negative output elementary Luo converter (NOELC), which includes a switch, a diode, two inductors (L_1 and L_2) and two capacitors (C_1 and C_2), with the load represented by a resistor R.

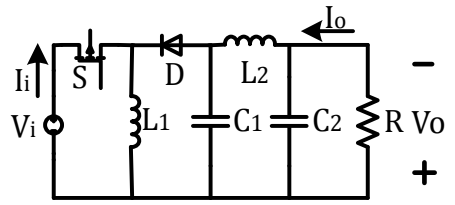

Fig. 1 Negative output elementary Luo converter (NOELC)

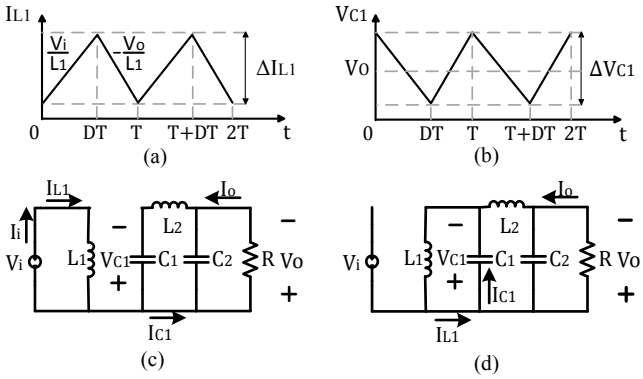

Fig. 2 The operation waveforms and principle of NOELC: (a) inductor current I_{L1}, (b) capacitor voltage V_{C1}, (c) equivalent circuit for $0<t<DT$, (d) equivalent circuit for $DT<t<T$

A. Continuous-Conduction Mode (CCM) Voltage Gain of Negative Output Elementary Luo Converter

Fig. 2 shows the operation waveforms and principle of the NOELC. In Fig. 2 (a) and (b), when 0<t<DT, the charge from the source energizes the inductor L1. When DT<t<T, the inductor L1 releases its energy to charge the capacitor C1, hence we get equations (1) and (2) where f is the switch frequency and *D* is the duty cycle of the switch. The inductor current i_{L1} waveform can be deduced by following (1) and (2) as shown in Fig. 2 (a). In addition, as the energy provided to the load is mainly offered by the capacitor C1 during 0<t<DT and offered by inductor L1 during DT<t<T. During 0<t<DT, if the current passes through C2 is small enough, then since Io≈IC1, the capacitor C1 is driving the load R. During DT<t<T, the energy released by the inductor L_1 is stored in the capacitor C_1, thus, charging it. Hence, the change of capacitor voltage ΔV_{C1} can be deduced as in (3) where Q_{C1} is the charge and the capacitor voltage waveform V_{C1} is as shown in Fig. 2 (b). From (1) and (2), the transfer function can be obtained as in (4), being the same as the buck-boost converter. In the following, I_{L1} represents the dc signal, while i_{L1} represents the ac signal.

$$\Delta i_{L1} = \frac{1}{L_1}\int_0^{DT} V_i dt = \frac{DTV_i}{L_1} = \frac{DV_i}{L_1 f} \tag{1}$$

$$\Delta i_{L1} = \frac{1}{L_1}\int_{DT}^{T} V_o dt = \frac{(1-D)V_o}{L_1 f} \tag{2}$$

$$\Delta V_{C1} = \frac{\Delta Q_{C1}}{C_1} = \frac{I_o DT}{C_1} = \frac{V_o DT}{RC_1} \tag{3}$$

$$M_V = \frac{V_o}{V_i} = \frac{I_i}{I_O} = \frac{D}{1-D} \tag{4}$$

B. Boundary between CCM and DCM of the Negative Output Elementary Luo Converter

From Fig. 2(a), if the average inductor current I_{L1} is smaller than half of its peak-to-peak value, then the converter would enter the DCM. Subsequently, the average of the boundary inductor current I_{LB} between CCM and DCM can be determined from (5). Then, with (5) and (6), the average of the output boundary load current I_{OB}, the minimum duty cycle D_{min} and the boundary load resistance R_B can be defined as in (7), (8) and (9). Where equations (5) – (9) are the same as in the buck-boost converter. Fig. 3 shows the normalized load current and the resistance boundary between CCM and DCM as a function of *D*.

$$I_{L1B} = 0.5\Delta I_{L1} = \frac{DV_i}{2L_1 f} = \frac{(1-D)V_o}{2L_1 f} \tag{5}$$

$$I_{L1} = \frac{I_i}{D} = \frac{I_O}{1-D} \tag{6}$$

$$I_{OB} = \frac{V_O(1-D_{min})^2}{2fL_1} \tag{7}$$

$$R_B = \frac{V_O}{I_{OB}} = \frac{2fL_1}{(1-D_{min})^2} \tag{8}$$

$$L_{1,min} = \frac{R_{max}(1-D_{min})^2}{2f} \tag{9}$$

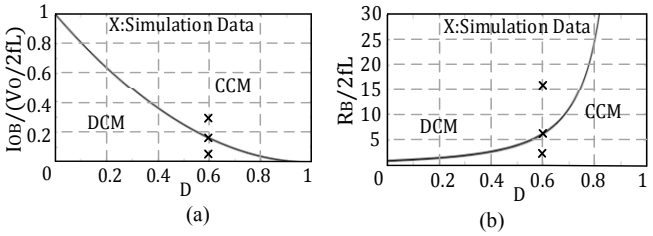

Fig. 3 The normalized (a) load current boundary $I_{OB}/(V_O/2f_SL_1)$ as a function of *D*, (b) load resistance $R_B/(2f_SL_1)$ as a function of *D* at the CCM/DCM boundary for the NOELC

III. Parameters Design of Negative Output Elementary Luo Converter

Here, we'll present the parameters design (L_1, L_2, C_1 and C_2) of the NOELC. The inductor L_1 can be designed according to the target CCM or DCM operation region (9) as discussed before. The inductor L_2 and capacitor C_2 act as a LC filter, which would be designed to eliminate the high frequency switching signal, for the converter to provide an output voltage with small ripple. The capacitor C_1 aims to hold the charge and keep the capacitor voltage V_{C1} equal to V_o.

A. Design of the Inductor L_2 and Capacitor C_2

The inductor L_2 and capacitor C_2 act as an LC low pass filter in this converter. The transfer function of the LC filter can be expressed by (10). The cut-off frequency of the LC filter is determined by the ω_0 in (11) and its gain given by (12),

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{\omega_0^2}{s^2+\omega_0^2} = \frac{\frac{1}{L_2C_2}}{s^2+\frac{1}{L_2C_2}} \tag{10}$$

$$\omega_0 = \sqrt{\frac{1}{L_2C_2}}\left(\frac{rad}{s}\right) = \frac{1}{2\pi}\sqrt{\frac{1}{L_2C_2}}(Hz) \tag{11}$$

$$|H(s)| = \left|\frac{1}{1-L_2C_2(2\pi f)^2}\right| \tag{12}$$

B. Design of the Capacitor C_1

Once we have the cut-off frequency of the LC filter, the output voltage ripple will be only determined by the capacitor C_1. Since the high frequency signal at the output has been filtered out, only the first order harmonic of the switching frequency at the output terminal V_o exists. To suppress the output voltage ripple, such first order harmonic at the capacitor C_1 should be as small as possible.

The capacitor C_1 voltage ripple function in the time domain can be defined as in (13) with the help of Fig. 2(b). By using a Fourier complex series, we can obtain its harmonic coefficient A_k in (14) where $\omega_0 = 2\pi/T$. By simplifying (14) we can get (15) and determine the first order harmonic coefficient A_1 of the capacitor voltage V_{C1}. By using the Euler's Equation as in (16), (15) can be expanded as presented in (17). Then the magnitude of A_1 can be expressed as in (18).

$$V_{C1,ripple} = \begin{cases} \frac{V_o D}{RC_1(1-D)}t + \frac{V_o DT}{2RC_1}, DT - T < t < 0 \\ -\frac{V_o}{RC_1}t + \frac{V_o DT}{2RC_1}, 0 < t < DT \end{cases} \tag{13}$$

$$A_k = \frac{1}{T}\int_{DT-T}^{0}\left(\frac{V_o D}{RC_1(1-D)}t + \frac{V_o DT}{2RC_1}\right)e^{jk\omega_0 t}dt + \frac{1}{T}\int_{DT-T}^{0}\left(-\frac{V_o}{RC_1}t + \frac{V_o DT}{2RC_1}\right)e^{jk\omega_0 t}dt \quad (14)$$

$$A_k = \frac{j}{2k\Pi}\left[e^{jk\omega_0 DT}\left(\frac{V_o DT}{2RC_1} - e^{jk\omega_0 T}\left(\frac{V_o(DT-T)}{RC_1(1-D)} + \frac{V_o DT}{2RC_1}\right)\right] + \frac{1}{(2k\Pi)^2}\left[e^{jk\omega_0 DT}\left(-\frac{V_o T}{RC_1} + \frac{V_o DT}{RC_1(1-D)}e^{jk\omega_0 T}\right) - \frac{V_o(1-2D)T}{RC_1}\right] \quad (15)$$

$$e^{j\theta} = \cos(\theta) - j\sin(\theta) \quad (16)$$

$$A_1 = \sin(2\pi D)\left(\frac{1}{2\Pi}\frac{V_o DT}{RC_1(1-D)} - \frac{1}{\Pi}\frac{V_o D^2 T}{RC_1(1-D)}\right) - \cos(2\pi D)\frac{1}{4\Pi^2}\frac{V_o T}{RC_1(1-D)} - \frac{1}{4\Pi^2}\frac{V_o(1-2D)T}{RC_1(1-D)} + j\left[\frac{1}{\Pi}\frac{V_o D^2 T}{RC_1(1-D)} - \frac{1}{4\Pi^2}\frac{V_o T}{RC_1(1-D)}\sin(2\pi D) - \frac{1}{2\Pi}\frac{V_o DT}{RC_1(1-D)}\cos(2\pi D)\right] \quad (17)$$

$$|A_1| = \sqrt{(Re\{A_1\})^2 + (Im\{A_1\})^2} \quad (18)$$

The output voltage ripple can be determined by multiplying the gain of the LC filter (12) and the magnitude of the first order harmonic coefficient of the capacitor V_{C1} (18), leading to (19).

$$V_{o,ripple} = |A_1||H(s)| \quad (19)$$

IV. Simulation Results

In this section, MATLAB Simulink simulations are carried out to verify the parameters design study of the NOELC. The simulation study can be separated into two parts: 1) verification of the CCM/DCM boundary study; and 2) output voltage ripple analysis. In the simulation, the switch and diode loss are neglected for simplicity.

TABLE I.
THE TEST SIMULATION CONDITIONS OF NOELC FOR CCM/DCM BOUNDARY VERIFICATION

	Case I	Case II	Case III
f	1MHz	1MHz	1MHz
L_1	1μH	1μH	1μH
D	0.6	0.6	0.6
R	33.3Ω	12.5Ω	7.7Ω
Normalized load current	0.06	0.16	0.26
Normalized load resistance	16.67	6.25	3.85

TABLE I shows the simulation condition of the NOELC for the CCM/DCM boundary verification. TABLE II and III show the simulation conditions and the designed parameters for the output voltage ripple analysis of the CCM.

TABLE II.
THE TEST SIMULATION CONDITIONS FOR OUTPUT VOLTAGE RIPPLE VERIFICATION

	Case IV	Case V
f	1MHz	1MHz
V_i	1.2V	1.2V
Vo	3.3V	3.3V
I_O	100mA	150mA
ΔV_O	1~2%	1~2%

TABLE III.
THE DESIGNED PARAMETERS OF THE NOELC FOR OUTPUT VOLTAGE RIPPLE VERIFICATION

	Case IV & V
L_1	1.4μH
L_2	0.5μH
C_1	0.25μF
C_2	0.5μF

A. Verification of CCM and DCM Boundary – Cases I, II, III

According to the parameters of the NOELC from TABLE I, Fig. 4 shows the simulated inductor current I_{L1} for the Cases I, II and III, which verifies the normalized CCM/DCM boundary curve (Fig. 3). In Case I, the normalized load resistance is larger than its boundary value. Then, it enters the DCM region as Fig. 4 shows. In Case II, the normalized load resistance is equal to its boundary value. As a result, it touches the boundary as also shown in Fig. 4; In Case III, the normalized load resistance is smaller than its boundary value. It then enters the CCM region as also illustrated in Fig. 4.

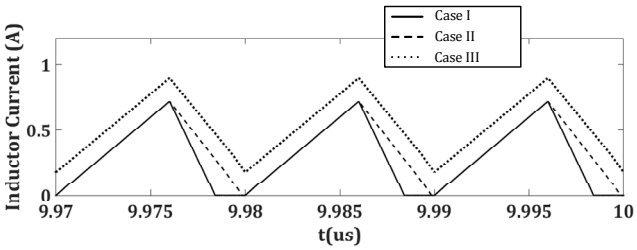

Fig. 4 Inductor Current I_{L1} of the verification of CCM/DCM boundary study

B. Verification of Output Voltage Ripple - Case IV

From TABLE II, the voltage gain is 2.75 and the load resistance is 33Ω. Hence D is 0.734 from (4) and the boundary inductor $L_{1,\,min}$ is 1.17μH from (9). By setting the cut-off frequency ω_0=320kHz, we can obtain C_2=0.5μF and L_2=0.5μH from (11). Therefore, the LC filter gain $|H(s)|$ is 0.113 based on (12). Finally, we substitute the above data into (18) and (19), and the capacitor C_1 can be determined by (20). To achieve 1~2% output voltage ripple, the corresponding capacitor C_1 should be 0.14μF~0.28μF. Therefore, C_1=0.25μF and L_1=1.4μH have been chosen to fulfill such conditions.

$$V_{o,ripple} = \frac{9.39*10^{-9}}{C_1} \quad (20)$$

C. Verification of Output Voltage Ripple - Case V

From TABLE II, the voltage gain is 2.75 and the load resistance is 22Ω. Hence, D is 0.734 from (4) and the boundary inductor $L_{1,\,min}$ is 0.78μH from (9). Then we set the cut-off frequency ω_0=320kHz, thus obtaining C_2=0.5μF and L_2=0.5μH from (11). Therefore, the LC filter gain $|H(s)|$ is 0.113 from (12). Finally, we substitute the above data into (18) and (19), and the capacitor C_1 can be determined by (21). To achieve 1~2% output ripple, the capacitor C_1 should be 0.21μF~0.42nF. Therefore, C_1=0.25μF and L_1=1.4μH have been chosen to fulfill such conditions.

$$V_{o,ripple} = \frac{1.40*10^{-9}}{C_1} \quad (21)$$

According to the designed parameters of NOELC as shown in TABLE III, Fig. 5 shows the output voltages for Cases IV and V and TABLE IV summarizes the comparison between this method and the conventional, in which the output voltage ripple (%) is calculated from (22). From TABLE IV, the conventional voltage ripple approximation method [9] is very inaccurate when compared with the proposed estimation method. Simulation results verify the proposed output voltage ripple estimation method, which can help to design the system parameters in order to suppress the voltage ripple. Finally, a summary of the proposed parameters design of the NOELC is shown in TABLE V.

If the total inductance and capacitance for the conventional buck-boost converter are kept the same as the NOELC, that are the total inductance $L_{buck\text{-}boost}=L_1+L_2$=0.18μH and the total capacitor $C_{buck\text{-}boost}=C_1+C_2$=0.75μF, the buck-boost converter obtains 3.00% output voltage ripple in Case IV and 4.42% output voltage ripple in Case V, which are about 3 times more than the NOELC. This result also verifies the important value of the NOELC study in this paper.

$$V_{o,ripple}(\%) = \frac{V_{o,ripple}}{V_o} \times 100\% \quad (22)$$

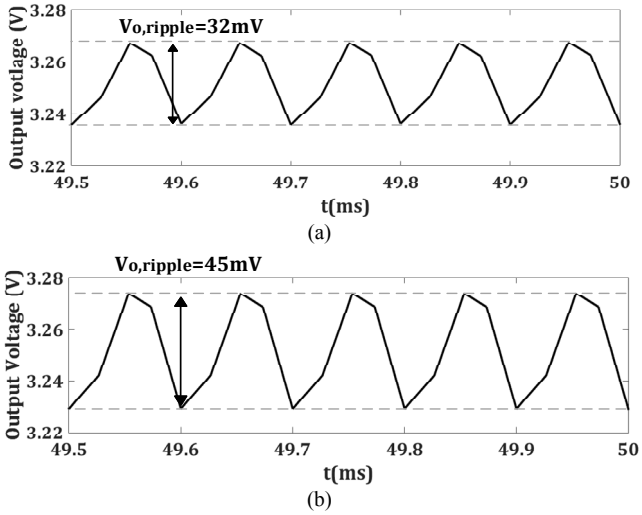

Fig. 5 Output voltage V_o of (a) Case IV and (b) Case V

TABLE IV.
COMPARISON OF OUTPUT VOLTAGE RIPPLES BETWEEN THE CONVENTIONAL [9] AND THE PROPOSED METHOD

	Conventional approximation method [9]	Proposed Estimation Method	Actual value
Equation	$\frac{D}{128f^3L_2C_1C_2R}$	$\|A_1\|\|H(s)\|$	/
Voltage Ripple in Case IV (%)	0.084	1.14	0.97
Voltage Ripple in Case V (%)	0.126	1.70	1.35

TABLE V.
SUMMARY OF PARAMETERS DESIGN OF THE NOELC

Parameter	Equation
L_1	$L_{1,min} = \frac{R_{max}(1-D_{min})^2}{2f}$
L_2	$\|H(s)\| = \|\frac{1}{1-L_2C_2(2\pi f)^2}$
C_1	$V_{o,ripple} = \|A_1\|\|H(s)\|$
C_2	$\|H(s)\| = \|\frac{1}{1-L_2C_2(2\pi f)^2}$

V. CONCLUSIONS

This paper presented the CCM operation analysis of a negative output elementary Luo converter (NOELC), which included the CCM voltage gain and the CCM/DCM operation boundary. The parameters design criteria for the NOELC was also determined, as well as the output voltage ripple estimation method which can help to design the system's parameters in order to suppress the voltage ripple. Simulation results were provided to verify the parameters design and the output voltage estimation method in comparison with the conventional method.

VI. ACKNOWLEDGMENT

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VII. REFERENCES

[1] K. R. Kumar, S. Jeevananthan, "Modelling and implementation of fixed switching frequency sliding mode controller for negative output elementary super lift Luo-converter", *IET Power Electron.*, vol. 5, no. 8, pp. 1593-1604, Sep. 2012.

[2] K. R. Kumar and S. Jeevananthan, "Design and implementation of reduced-order sliding mode controller plus proportional double integral controller for negative output elementary super-lift Luo-converter", *IET Power Electron.*, vol. 6, no. 5, pp. 974-989, May 2013.

[3] R. Kumar, B. Singh, "Solar Photovoltaic Array Fed Luo Converter Based BLDC Motor Driven Water Pumping System", *ICIIS 2014*, Gwalior, India, pp. 1-5, Dec. 2014.

[4] A. Cocor, A. Baescu, and A. Florescu, "Elementary and self-lift negative output Luo dc-dc converters used in hybrid cars," *U.P.B. Sci. Bull., Series C,* vol. 77, no. 4, pp. 179-190, 2015.

[5] S. M. Ding, F.Q. Wang, “A New Negative Output Buck-Boost Converter with Wide Conversion Ratio”, *IEEE Trans. Ind. Electron.*, vol. pp, no. 99, pp. 1-1, Jun. 2017.
[6] M. K. Kazimierczuk, “Buck-boost PWM DC-DC Converter” in *Pulse-width Modulated DC-DC Power Converters,* Dayton, Ohio, USA, Wiley, ch. 4, pp. 139-168, 2008.
[7] J. M. Alonso, A. J. Calleja, D. Gacio, J. Cardesin, E. Lopez, “A long-life high-power-factor HPS-lamp LED retrofit converter based on the integrated buck-boost buck topology”, *IEEE Proc., IECON 11*, Melbourne, VIC, Austria, pp. 2860-2865, Jan. 2012.
[8] M. R. Cosetin, E. A. Bitencourt, T. E. Bolzan, M. F. da Silva, J. M. Alonso and R. N. do Prado, “Comparison of integrated SEPIC-Buck and SEPIC-Ćuk converters as off-line dimmable LED drivers with reduced storage capacitor” *EPE 14-ECCE Europe*, Lappeenranta, Finland, pp. 1-10, Sep. 2014.
[9] F. L. Luo, “Negative Output Luo Converters: Voltage Lift Technique”, *IEEE Proc., Elect, Power Appl.*, vol. 146, no. 2, pp. 208-223, Mar. 1999.
[10] R. Kayalvizhi, S. P. Natarajan, P. Suresh Pandiarajan and R. Vijayarajeswaran, “Control of Paralleled Negative Output Elementary Luo Converters”, *IEEE Proc., PEDS 05*, Malaysia, pp. 1234-1238, Dec. 2005.
[11] Y. Jian, F.L. Luo, M. Zhu “Voltage-lift-type switched-inductor cells for enhancing DC-DC boost ability: Principles and integrations in Luo converter”, *IET Power Electron.*, vol. 4, no. 1, pp. 131-142, Feb. 2011.
[12] B. Achiammal, R. Kayalvizhi, “Genetic Algorithm Based PI Controller for Negative Output Elementary LUO Converter”, *IEEE Proc., ICACCCT 14*, Ramanathapuram, India, pp. 1099-1103, May. 2014.