ISSCC 2005 DIGEST CD

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2005 IEEE Fellows

Laurence W. Nagel
Omega Enterprises, Randolph, NJ
"For contributions to the field of integrated circuit simulation"

Terri S. Fiez
Oregon State University, Corvallis, OR
"For contributions to analog and mixed-signal integrated circuits"

Koichiro Ishibashi
Semiconductor Technology Academic Research Center (STARC) Yokohama, Japan
"For technical contributions to developments of low-power SRAMs and MCUs"

Kazuo Yano
Hitachi, Tokyo, Japan
"For contributions to nanostructured-silicon devices and circuits and advanced CMOS logic"

2003-04 DAC/ISSCC Student-Design-Contest Winners

OPERATIONAL CATEGORY

1st Place and Best Overall
"A Single Chip Ultra-Wideband Transceiver"
Fred S. Lee, Anantha P. Chandrakasan, Raul Blazquez,
Massachusetts Institute of Technology, Cambridge, MA,
Puneet P. Newaskar,
Silicon Labs, Austin, TX

2nd Place
"81 MS/s JPEG 2000 Single-Chip Encoder with Rate-Distortion Optimization"
Hung-Chi Fang, Yu-Wei Chang, Tung-Chien Chen, Liang-Gee Chen,
National Taiwan University, Taipei, Taiwan

3rd Place (tie)
"An 80Gbps FPGA Implementation of a Universal Hash Function based Message Authentication Code"
Bo Yang, Ramesh Karri,
Polytechnic University, Brooklyn, NY;
David A. McGrew, Cisco Systems, San Jose, CA

3rd Place (tie)
"A Modular 32-Site Wireless Neural Stimulation Microsystem"
Maysam Ghovanloo, **Khalil Najafi**,
University of Michigan, Ann Arbor, MI

CONCEPTUAL CATEGORY

1st Place
"The Economical Aphotic Sieving Machine"
Kamran Kashef, Matt Hardy,
University of Michigan, Ann Arbor, MI

2nd Place,
"VIRAM1: A MediaOriented Vector Processor with Embedded DRAM"
Joseph Gebis, Sam Williams, David Patterson,
University of California, Berkeley, CA;
Christos Kozyrakis,
Stanford University, Palo Alto, CA

3rd Place
"SiGe Prototype Chip Design Implementing CMOS Fixed Bit-Load Drivers and Receivers for Next Generation High-Speed Board-Level Interconnect"
Jason D. Bakos, Amit Gupta, Leo Salavo, Donald Chiarulli,
University of Pittsburgh, Pittsburgh, PA

2004-05 DAC/ISSCC Student-Design-Contest Winners

OPERATIONAL CATEGORY:

Best Overall - 1st Place
"A 50MS/s (35mW) to 1kS/s (15μW) Power-Scaleable 10b Pipelined ADC with Minimal Bias-Current Variation"
Imran Ahmed, David Johns,
University of Toronto, Toronto, Canada

2nd Place
"A 1.3 TOPS H.264/AVC Single-Chip Encoder for HDTV Applications"
Tung-Chien Chen, Yu-Wen Huang, Chen-Han Tsai, To-Wei Chen, Liang-Gee Chen,
National Taiwan University, Taipei, Taiwan

3rd Place
"A side-Channel Leakage Free Coprocessor IC in 0.18μm CMOS for Embedded AES-based Cryptographic and Biometric Processing"
Kris Tiri, David Hwang, Alireza Hodjat, Bo-Cheng Lai, Shenglin Yang, Patrick Schaumont, Ingrid Verbauwhede,
University of California, Los Angeles, CA

CONCEPTUAL CATEGORY:

1st Place
"Design and Implementation of a Fractional-N Frequency Synthesizer for Cellular Systems"
Petrus J. Venter, Saurabh Sinha,
University of Pretoria, Pretoria, South Africa

2nd Place
"A 1-V IEEE 802.11a/b/g-Compliant Receiver IF-to-Baseband Chip in 0.35μm CMOS for Low-Cost Wireless SiP"
Pui-In Mak, Rui P. Martins,
University of Macau, Macao SAR, China
Seng-Pan U,
Chipidea Microelectronics (Macau), Macao SAR, China

3rd Place
"Collision Detection System using an FPGA Implemented on the FPX Platform"
Nasan N. Atay, Burchan Bayazit, John W. Lockwood,
Washington University, St. Louis, MO

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Pui-In Mak, Rui P. Martins, Seng-Pan U

Student Design Contest - 2nd Place, Conceptual Category

"A 1-V IEEE 802.11a/b/g-Compliant Receiver IF-to-Baseband Chip in 0.35µm CMOS for Low-Cost Wireless SiP"

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Volume 10
Number 3
September
2005

SOLID-STATE CIRCUITS

IEEE Solid-State Circuits Society Quarterly Newsletter

Jaeger Elected President of SSCS; Willy Sansen Elected Vice-President

At their August 29 meeting, the Society Administrative Committee elected Dick Jaeger to serve as President of the Society beginning 1 January 2006. Willy Sansen was elected to serve along with Jaeger as Vice-President. It is typical after serving two years, the Vice-President is elected President by the AdCom.

Sansen will be the first non-US based officer of the Society, the membership of which is made up of equal numbers of US and non-US based members. The President and Vice-President must have served in elected or appointed AdCom positions.

Richard C. Jaeger has served as an elected AdCom member since 1999. He has been Publications chair since the inception of the Society, and Vice President for the last two years.

He received BS and ME degrees in electrical engineering in 1966 and his Ph.D. degree in 1969, all from the University of Florida, Gainesville. From 1969 to 1979 he was with the IBM Corporation, working on precision analog design, I2L, microprocessor architecture, and low-temperature MOS device and circuit behavior. Since 1979 he has been at Auburn University, where he is Distinguished University Professor in Electrical and Computer Engineering. In 1984 he helped found the Alabama Microelectronics Science and Technology Center and served as director of the center until 2000. He currently serves as the interim director of the Auburn University undergraduate program in wireless technology, which he founded.

He has authored or co-authored over 200 technical papers and articles and three books: Introduction to Microelectronic Fabrication, Microelectronic Circuit Design, and Computerized Circuit Analysis Using SPICE Programs. From 1980 to 1982 he served as founding Editor-in-Chief of IEEE MICRO. He was elected Fellow of the IEEE in 1986. Dr. Jaeger was a member of the IEEE Solid-State Circuits Council from 1984 to 1991, serving the last two years as Council President. He was Program Chair for the 1993 ISSCC, Chair of the 1990 VLSI Circuits Symposium, Editor of the IEEE Journal of Solid-State Circuits from 1995-1998 and recipient of the 2004 IEEE Undergraduate Teaching Award.

Richard C. Jaeger
SSCS President
2006-2007

Willy Sansen
SSCS Vice President
2006-2007

Willy Sansen has served as an elected member of the SSCS AdCom from 1999 to 2001. He received the MSc degree in Electrical Engineering from the K.U.Leuven in 1967 and a Ph.D. in Electronics from the University of California, Berkeley in 1972.

In 1972 he was appointed by the National Fund of Scientific Research (Belgium) at the ESAT laboratory of the K.U. Leuven, where he has been a full professor since 1980. During the period 1984-1990 he was the head of the Electrical Engineering Department. Since 1984 he has headed the ESAT-MICAS laboratory on analog design, which counts about sixty members and which is mainly active in research projects with industry. He is a Fellow of the IEEE and is a member of several corporate boards of directors.

He was a visiting professor at Stanford University in 1978, in 1981 at the EPFL Lausanne, in 1985 at the University of Pennsylvania, Philadelphia, in 1994 at the Ulm Hochschule

Continued on page 2

this IN issue

cant design challenges is realizing precision analog circuitry in a digital CMOS process. In the digital world, supply voltages have been shrinking in order to reduce power consumption, as feature sizes have been shrinking in order to increase density and performance. These factors in combination result in a widening of the PVT (process, voltage, and temperature) window, making precision analog design even more difficult.

Since the ability to generate precision reference voltages in a hybrid chip environment is key to achieving several key analog functions, especially D/A and A/D conversion in a digital process, Mok and Leung's findings have been of major interest.

DAC/ISSCC Student Design Contest Promotes Excellence

Founded in 1981 and incorporated into the International Solid-State Circuits Conference in partnership with the Design Automation Conference in 2002, the Student Design Contest has become a premier international competition for electronic systems designs prepared by graduate and undergraduate students as part of their studies. "Both DAC and ISSCC are the renowned conferences in IC design," said "Elvis" Pui-In Mak, a winner of last year's 42nd annual competition. "Their jointly held contest, therefore, can be considered the number one contest among all the others. Winners represent 'state-of-the-art' achievements in IC design."

Variety and Novelty

Contest projects encompass two categories: "Operational" designs that have been fabricated and tested, and "Conceptual" designs that have been simulated extensively and include test plans, but have not yet been fabricated or tested. The chief requirement for an operational design is the inclusion of "measurements demonstrating that it works as expected," said David Greenhill, a 2004 contest co-chair. The criteria for a conceptual design are "based on simulation and a plan for how the design will be tested if and when it is built."

Mr. Greenhill praised the "very wide range of different design styles" submitted for competition. The biggest challenge for the judges is the breath of papers," he said. "Somehow they have to compare apples and oranges and decide which are best." The most fun for the judges is being exposed "to what is being designed in Academia. A lot of new and novel ideas come out of this. It definitely makes the judges think outside of their day to day design box."

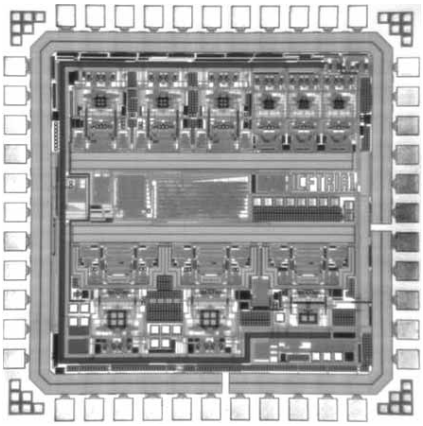
Imran Ahmed of the University of Toronto who, with David Johns, was the Overall and Operational Category winner last year, thought the competition helped advance his academic goals. "The process of putting together a submission has a 100% return in aiding one to further develop their research writing/presentation skills," he said. "In addition, the design contest process is a nice way to become familiar with the publications process."

Cash Prizes

Contestants vie for prizes donated by the Conferences and by industry supporters, including the Association of Computing Machinery (ACM) Special Interest Group on Design Automation (SIGDA), the Microelectronics Advanced Research Corporation (MARCO) and the Semiconductor Research Corporation (SRC) in 2004. Prize winners show their work at the annual DAC meeting in June and at the ISSCC in San Francisco in February. "If there is one thing that always makes a graduate student happy," Mr. Ahmed said, "it's money, which makes winning the $5,000 prize money the best part of the experience. Having a reason to legitimately take time during school to go visit California comes a close second."

Networking

The best part of the whole experience, Elvis Mak said, was the opportunity to meet and share ideas with admired researchers. "Many experts in related fields expressed an interest in our work and provided important comments during the discussion. It was my good fortune to meet face to face with some professors and researchers whose papers I had only been able to read, and see their photos in the JSSC."



Winners of the 42nd Annual Student Design Contest

OPERATIONAL CATEGORY

1st Place (Best Overall) A 50MS/s (35mW) to 1kS/s (15 É W) Power Scaleable 10b Pipelined ADC with Minimal Bias Current Variation. Imran Ahmed, David Johns - Univ. of Toronto, Toronto, ON. Canada

2nd Place A 1.3 TOPS H.264/AVC Single-Chip Encoder for HDTV Applications. Tung-Chien Chen, Yu-Wen Huang, Chen-Han Tsai, Ching-Yeh Chen, To-Wei Chen, Liang-Gee Chen - National Taiwan Univ., Taipei, Taiwan

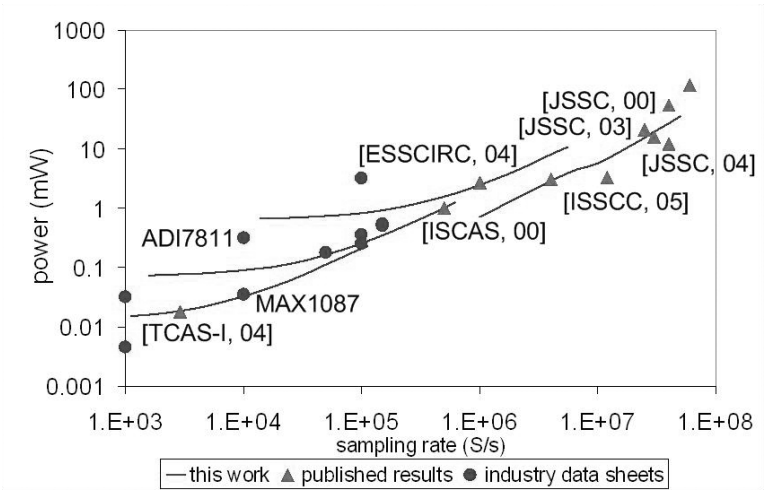
3rd Place A Side-Channel Leakage Free Coprocessor IC in 0.18É m CMOS for Embedded AES-based Cryptographic and Biometric Processing. Kris Tiri, David Hwang, Alireza Hodjat, Bo-Cheng Lai, Shenglin Yang, Patrick Schaumont, Ingrid Verbauwhede - Univ. of California, Los Angeles, CA

STUDENT DESIGN CONTEST DUE BEFORE 5 pm MST, Dec. 6, 2005

Students are invited to submit descriptions of original electronic designs, either circuit level or system level. Student Design Contest paper submissions must (1) be in PDF format only, (2) contain the title of the project, (3) contain an abstract of approximately 60 words, (4) contain a complete description of the project, and (5) be no more than 6 pages (including the abstract, maximum of 10 figures/tables and references), double-columned, 9pt or 10pt font. The submission should clarify the originality, distinguishing features, and measured performance of the design. Two categories of designs - operational and conceptual - are eligible for awards. For operational designs, proof-of implementation is required, while for conceptual designs, complete simulation is necessary. Designs must have taken place as part of the students' work at the university and must have been completed after June 2004. Submitted designs should not have received awards in other contests. Selected designs will be presented at the conference (and at ISSCC in February 2006). Additional submission guidelines are available on the DAC web site.

2005 Contest Chairs: Alan Mantooth (University of Arkansas) and Bill Bowhill (Compaq Computer Corporation)

More information may be found at: www.dac.com "Call for Papers"



From "A 50MS/s (35mW) to 1kS/s (15É W) Power Scaleable 10b Pipelined ADC with Minimal Bias Current Variation," by Imran Ahmed and David Johns - Univ. of Toronto, Toronto, ON. Canada, providing a comparison of their results with industry data sheets.

CONCEPTUAL CATEGORY

1st Place Design and Implementation of a Fractional-N Frequency Synthesizer for Cellular Systems. Petrus J. Venter, Saurabh Sinha - Univ. of Pretoria, Pretoria, South Africa

2nd Place A 1-V IEEE 802.11a/b/g-Compliant Receiver IF-to-Baseband Chip in 0.35É m CMOS for Low-Cost Wireless SiP. Pui-In Mak, Rui P. Martins - Univ. of Macau, Macao SAR, China. Seng-Pan U - Chipidea Microelectronics (Macau) Ltd., Macao SAR, China

3rd Place Collision Detection System using an FPGA Implemented on the FPX Platform. Hasan N. Atay, Burchan Bayazit, John W. Lockwood - Washington Univ., St. Louis, MO

Advice to Applicants

"The key aspect to a successful submission," Mr. Ahmed said, "is to carefully organize and write your submission in such a way that a person who does not know anything about your work will get enough basic ideas out of it that they will want to read more about it, either through your thesis or published papers. Trying to explain every small detail complicates the discussion and distracts the reader from the key points you have. However, to make your paper also appealing to experts in your field, you should provide a concise summary of your results and, most importantly, compare against previous works to put your work in context,"

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Being named an IEEE Fellow is a lifetime honor. It is recognized and respected by your colleagues throughout the industry. It is recognition for major technical contributions. Many Fellows add the title to their business cards.

The Fellow nomination form is four pages long. The nominator does not have to be an IEEE Fellow or even an IEEE member. It is not difficult to complete and should focus on the technical achievements of the nominated candidate. Self-nomination is not allowed; however, collaboration between nominator and candidate is almost universal. A minimum of five and a maximum of eight references are required from current IEEE Fellows. A complete list of IEEE Fellows is available on line at:

A 1-V IEEE 802.11a/b/g-Compliant Receiver IF-to-Baseband Chip in 0.35-µm CMOS for Low-Cost Wireless SiP

Pui-In Mak
Analog and Mixed-Signal VLSI Lab., University of Macau, Macao SAR, China
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(On leave from Instituto Superior Técnico, Lisbon, Portugal)
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ABSTRACT

The proliferation of multiple WLANs and the continual scaling of CMOS technologies stimulate the development of low-voltage multistandard transceiver solutions. Instead of approaching a pricey nano-CMOS system-on-chip (SoC), we developed a 1V-workable IEEE 802.11a/b/g-compliant receiver IF-to-baseband chip in 0.35-µm CMOS for system-in-package (SiP), which cost-efficiently interfaces the technology-flexible analog radio with the sub-1V nano-CMOS digital baseband.

Categories and Subject Descriptors

B.7.0 [**Integrated Circuits**]: General.

General Terms

Design, Performance, Verification.

Keywords

CMOS, IEEE 802.11a/b/g, Low-IF, Multistandard, System-in-Package, System-on-Chip, Zero-IF.

1. INTRODUCTION

Widespread uses of wireless local-area networks (WLANs) in recently years have opened up a sizeable and expanding marketplace for wireless industry to continuously improve their product functionalities without compromising on costs. Features such as a high-level of integration, low-voltage operation, low-power dissipation and multistandard compliant are all essential to minimize the cost, take advantages of sub-1V nano-CMOS technologies and enable long-lasting connectivity and seamless interswitching between different WLAN standards. IEEE 802.11a, b and g are the three prominent WLAN standards we exploit today. Dissimilarity in their physical layer (PHY), regrettably, obstructs the systems from reaching the sought features.

Briefly, 802.11b is a 2.4-GHz complementary code keying (CCK)-based system with 22-MHz channel bandwidth and 5.5-11 Mb/s data rate. Whereas both 802.11a and g are orthogonal frequency-division multiplexing (OFDM) system with 20-MHz channel bandwidth and 6-54Mb/s data rate, but separately operate in the 5 GHz and 2.4 GHz, respectively [1]. A complete transceiver solution for them can be a system-on-chip (SoC) or a system-in-package (SiP).

Since the announcement of the world's first CMOS SoC design for IEEE 802.11a/b/g WLANs [2], numerous other solutions (even they are not yet a complete SoC) have been reported [3]-[5]. In digital world, sub-1V 90-nm CMOS is expected to deliver substantial improvements in speed, power reduction, integration and density compared with today's 0.13-µm technology. In contrast, nano-CMOS becomes an anathema in terms of analog and mixed-signal circuit performances, as shown in Fig. 1. Threshold voltage scaling is not keeping pace with supply-voltage reduction that must scale down with the gate-oxide thickness. Very fundamental circuits that are capable to process large signal swing cannot be fully functioned when the supply is close to the sum of the NMOS and PMOS threshold voltages, such as floating switches and common-mode feedback circuits. Indirect implementation of them with the help of auxiliary circuitry is normally unavoidable, i.e., more power and silicon area. In addition, substrate crosstalk induced signal integrity also sophisticated the realization of a mixed-signal SoC transceiver.

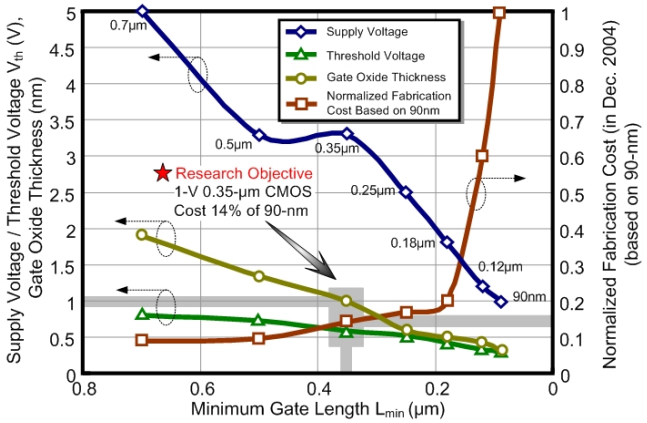

Fig. 1 Roadmap of CMOS scaling and the research objective.

Alternatively, SiP offers more flexibility. Chips based on different technologies can be packed together as one chipset without substrate noise issue. Cutting-edge nano-CMOS technologies can be independently utilized for the digital baseband, whereas the established analog library can be safely reused in the analog radio and analog baseband without doing technology migration repetitively, saving design time while reducing risk. This work ─ a 1V-workable 0.35-µm CMOS 802.11a/b/g-compliant receiver IF-to-baseband chip ─ is targeted to be a low-cost companion [Fig. 1] of a 90-nm CMOS digital-baseband processor in a 1-V SiP design with one power manager.

After this introduction, a low-IF/zero-IF reconfigurable receiver employed a two-step channel-selection technique [6] is presented, which joins the beneficial features of low-IF and zero-IF architectures together such that different applications can be processed in their preferred operating modes with simple digital control, and simultaneously, relaxes the design specifications of the radio frequency synthesizer [6]. The exploited design methodology leveraging the speed and accuracy of the verifications in analog, digital and mixed-signal domains is

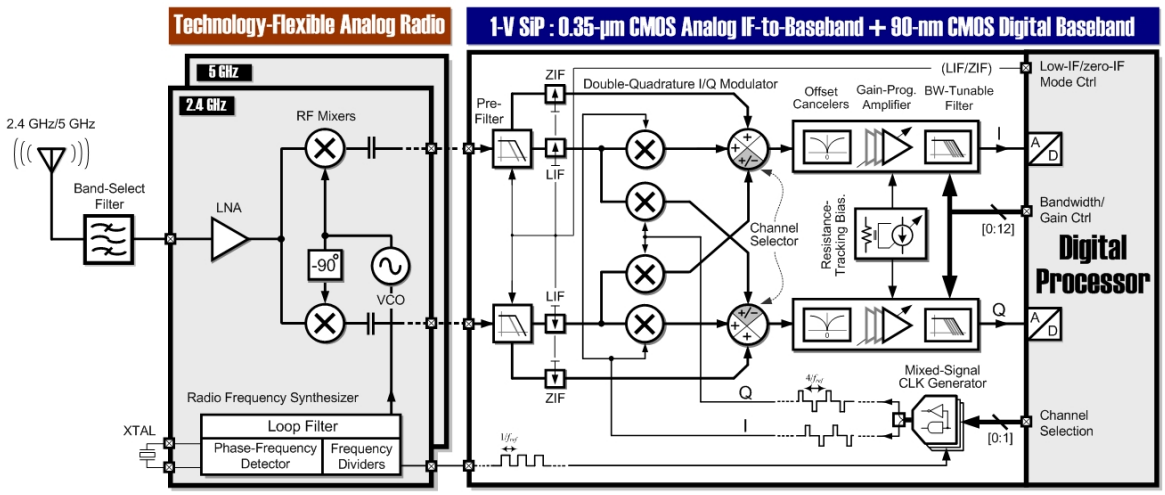

Fig. 2 Receiver architecture.

addressed next. Afterward, a series of low-voltage low-power circuit techniques workable at only 1-V supply with 0.35-μm CMOS transistors (typical mean: VT_N=0.65V and VT_P=0.5V) are described. The layout design and verifications, and test plan are summarized finally.

Those architecture-to-circuit-level solutions are the originalities of the work that are very different from the other non-low-voltage-designed 802.11a/b/g WLAN solutions [3]-[5].

2. RECEIVER ARCHITECTURE

The characteristics of the standards are the fundamental criteria for architectural choices. 802.11b is a wideband and spread-spectrum standard, direct conversion (zero-IF) is the most efficient way once the low-frequency disturbance (DC offset and flicker noise) is eliminated, for instance, by AC-coupling. Conversely, although 802.11a and g are wideband also, the OFDM technique causes removal of the low-frequency disturbance by notch filtering very problematic, a slight frequency deviation in the radio frequency synthesizer will place the notch on the channel sub-carriers rather than the unwanted low-frequency disturbance [7]. To alleviate the problem, a low-IF architecture with a half-channel-spacing IF can be utilized for both 802.11a and g, since the image is now the first adjacent channel that only 16 dB larger than the desired one. Practically achievable image rejection of ~33 dB will be adequate.

Such architectural considerations lead to the receiver as shown in Fig. 2. The analog IF-to-baseband chip interfaces the analog radio to the digital baseband with two possible operating modes, but shares only one power manager in split of the large inconsistency of the employed technologies, i.e., a 90-nm CMOS digital-baseband processor and a 0.35-μm CMOS analog IF-to-baseband chip. The analog radio is technology flexible, today mainstream CMOS or other technologies such as SiGe and BiCMOS are also alternatives. The overall operations are described as follows:

The two frequency bands, 2.4GHz and 5GHz, require two sets of low-noise amplifiers (LNAs) and RF mixers for amplification and RF-to-IF downconversion, respectively. The pre-filter and double-quadrature I/Q modulator offer two modes: filtering and downconversion in low-IF mode, or simply filtering with reduced bandwidth in zero-IF mode. The modulator also serves as an IF channel selector such that the whole channel selection can be partitioned efficiently between the frequency synthesizer and the modulator. The modulation signals are generated by an I/Q-mismatch insensitive mixed-signal clock generator. The bandwidth-tunable filter purifies the channel spectrum for different bandwidths, and the gain-programmable amplifier optimizes the signal swing to full-scale for A/D conversion. Offset-cancelers are embedded in both the filter and amplifier to suppress nonlinearity, 1/*f* noise and DC offset. The cut-off frequency is stabilized by utilizing a resistance-tracking biasing circuit. Their different modes of operation, channel selection, gain and bandwidth controls are done by digital.

3. DESIGN METHODOLOGY

The scope of a low-IF/zero-IF reconfigurable, low-voltage low-power receiver required innovative design and simulation permutations. Our design methodology with a mixture of available design tools is summarized in Fig. 3.

An abstract-system model is built by using *MatLab/Simulink* and the provided toolboxes for functionality verifications and virtual

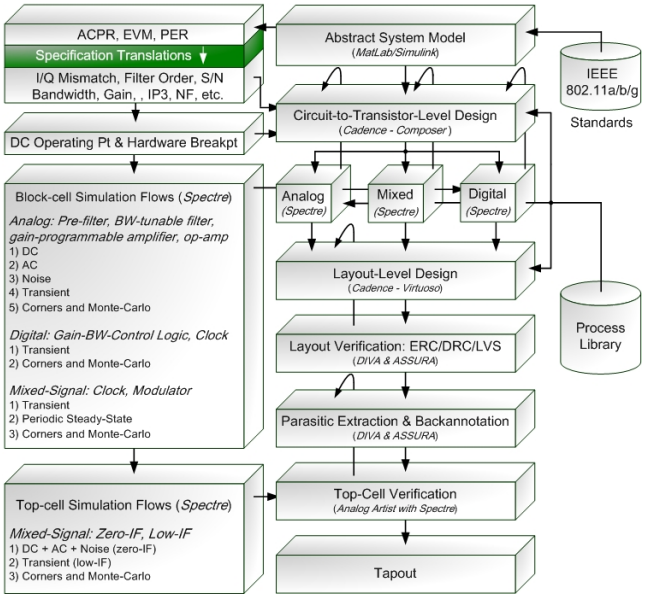

Fig. 3 Design methodology.

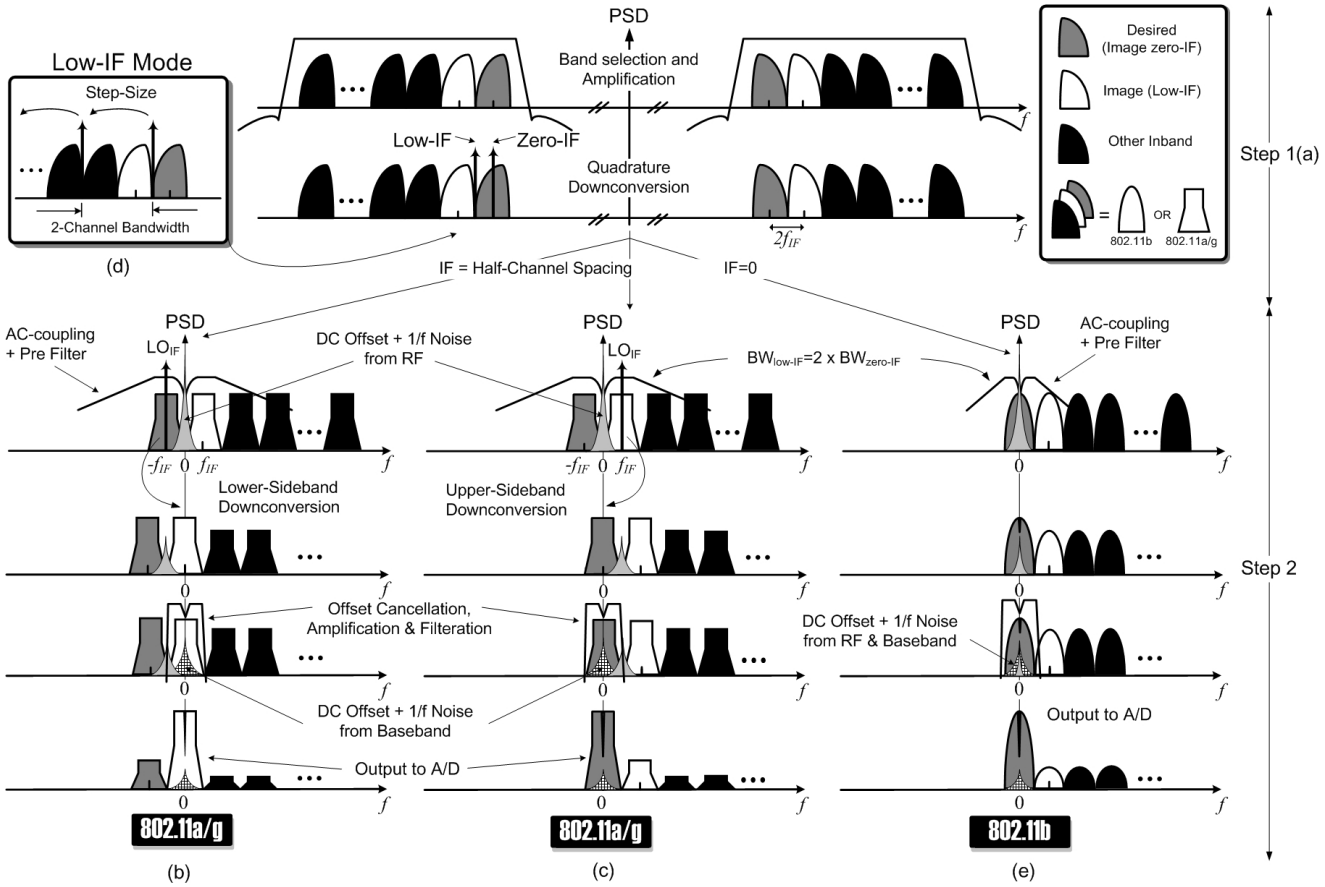

Fig. 4 Spectra-flow illustrations. (a) Step-1: RF-to-IF downconversion for 802.11a/b/g. (b) Step-2: IF-to-baseband lower-sideband downconversion. (c) Step-2: IF-to-baseband upper-sideband downconversion. (d) Low-IF channel-selection scenario at RF. (e) Step-2: zero-IF mode.

measurements of adjacent-channel power ratio (ACPR), error-vector magnitude (EVM) and packet-error rate (PER). Results from the models were translated to circuit-level specifications such as I/Q mismatch, filter order, 3rd-order intercept point (IP3) and noise figure (NF), etc. Circuit-to-transistor-level design was carried in *Cadence Composer*. Our experience told us that DC operating points (e.g., input and output common modes) should be set before circuit architectures were chosen, on the ground that differential pair and analog switches only work on the DC level closed to the supply rails. Hardware breakpoints were assigned for block measurements in case of partly malfunction. All analog cells were full-custom designed, whereas the digital ones were based on standard cells with a scaled-up physical size to compensate the increased delay of low-voltage implementation (gate delay $\propto$ 1/supply). Constraint-driven optimization reduced the number of iterations in the design of paramount analog cells such as op-amp gain, bandwidth and phase margin tradeoffs. The first verifications of analog and digital blocks were done in *Spectre* progressively from static (DC, AC) to dynamic (transient), that helps to facilitate the verification and optimization. The mixer was simulated at last as it is the crossing point of analog and digital cells, also the changing point of low-IF and zero-IF modes. Iteration between the design and simulation stages continued, dependent upon system performance.

Layout design was completed in *Cadence Virtuoso* after careful floorplanning and pin-out assignments. DRC and LVS cleared layout was extracted to get the ubiquitous parasitic. Imbalanced parasitic at the important nodes (e.g., op-amp inputs) were equalized by doing backannotation and extraction repeatedly. Top-cell verifications in low-IF and zero-IF modes were executed separately in different workstations to save the simulation time and facilitate debugging. Deliberately setting the input waveform and changing the circuit states speeded up the top-cell verification, for instances, DC, AC and noise analysis run in parallel involved only one-time netlisting and DC analysis, but determined many static behaviors simultaneously (e.g. bandwidth and stopband attenuation). Whereas a short-transient simulation with an input level that can get largest output swing and with the largest gain step applied in between measured the worst dynamicity (e.g. settling time and signal-to-noise ratio). Both Monte-Carlo and corner simulations were executed iteratively before tapout.

4. OPERATING PRINCIPLES

4.1 Low-IF Mode

Figure 4(a)-(c) describes the operation in low-IF mode pictorially. No matter the operation is for 5-GHz 802.11a or 2.4-GHz 802.11g, after amplification by the LNA, the desired channel and its image will be downconverted together to the identical IF (which is half-channel spacing) but with a complex-conjugate representation [Fig. 4(a)]. The low-frequency disturbance, located in between the desired signal and its image, is now easily cancelable by AC-coupling, whereas the high-side injected image is suppressed by

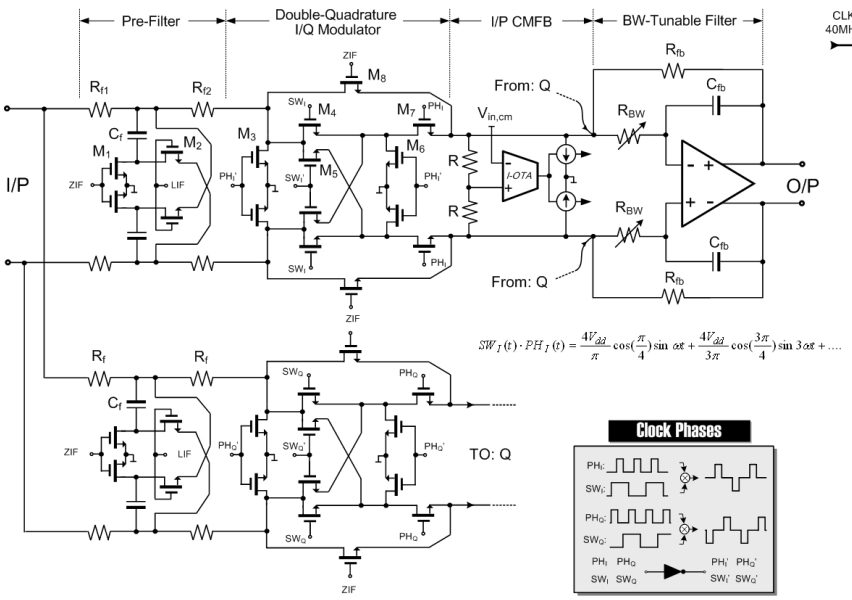

Fig. 5 Pre-filter, double-quadrature I/Q modulator and BW-tunable filter.

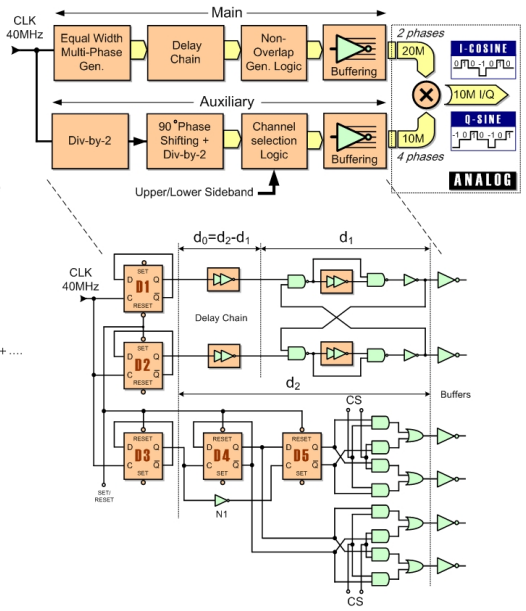

Fig. 6 Mixed-signal clock generator.

the pre-filter. Now, suppose the double-quadrature I/Q modulator can flexibly select either of them from IF to baseband without using any frequency synthesizer, a channel selection is accomplished between the desired channel and its image without any prerequisite needed in the radio [Fig. 4(a)-(c)]. In the followed filter and amplifier, offset cancellation is possible as the OFDM channel has no sub-carrier at DC and the IF-to-baseband downconversion imposes very small frequency error. This coarse-at-radio fine-at-baseband channel selection, namely *two-step channel selection* [6], provides many advantageous features to the radio frequency synthesizer as described as follows:

First, the step-size of the frequency synthesizer can be doubled [Fig. 4(d)], which implies that the division ratio (also named as modulus) in the phase locked-loop (PLL) will be halved since the finally selection is done at the IF. If an integer-*N* PLL frequency synthesizer is utilized, the reference frequency that must be equal to the step-size can be accordingly doubled to shorten the PLL settling time by 50%, and to enlarge the loop bandwidth of the PLL for suppressing the in-locked oscillator phase noise. Moreover, higher reference frequency also increases the PLL damping ratio, improving the PLL stability. Furthermore, since the division ratio is proportional to the close-in phase noise of the PLL, halving that ratio also reduces the power of the close-in phase noise by a factor of 4 and simplifies the frequency divider anatomy because half of the locking positions are saved. The detailed relationships among all of these issues are clearly analyzed and discussed in [8].

4.2 Zero-IF Mode

For the 802.11b, direct downconversion is preferred [Fig. 4(e)] since offset cancellation with cutoff-frequency less than 10 kHz generates insignificant intersymbol interference (ISI). The bandwidth of the pre-filter is correspondingly reduced by a factor of 2, and the double-quadrature I/Q modulator is bypassed. The followed operations including offset cancellation, filtration and amplification are all analogous to those in low-IF mode.

5. CIRCUIT AND LAYOUT DESIGNS

The entire system is fully differential, and mainly consists of three parts. The pre-filter, the double-quadrature I/Q modulator and the bandwidth-tunable filter are one functional block. The mixed-signal clock-phase generator is the second one. The third ones are the gain-programmable amplifiers and its offset-canceler embedded op-amp. The applied techniques are summarized next.

5.1 Pre-Filter, Double-Quadrature I/Q Modulator and Bandwidth-Tunable Filter

The simplified schematic is shown in Fig. 5, where only the I-channel is shown. Starting from the most left-hand side, the pre-filter is constructed by simple passives, resistor R_{f1} and capacitor C_f, with its cut-off frequency overdesigned to account for the process variations. The dual modes mean two different bandwidths; one is two times larger than the other for low-IF/zero-IF operation [Fig. 4]. A cost-efficient and accurate way to implement such a bandwidth doubling is by connecting the grounded capacitors C_f's, to their out-of-phase paths by a swapper formed by M_1 and M_2. The forward resistors, R_{f1} and R_{f2}, together serve as a linear *V-I* converter for the following switching mixers. Conventionally, 1-V supply cannot offer enough overdrive to the MOS-transistor mixers, M_4 and M_7. However, by using input common-mode feedback, the differential input terminals of the op-amp can be independently bias to a voltage level differ from the output common mode, which must be close to half of the supply to maximize the signal swing. By using NMOS transistors as the switches and sets the input common-mode level to 0.1V, at least 200-mV overdrive can be maintained over the process corners. Moreover, input common-mode feedback also allows the DC operating point of the RF mixer bias independently to the pre-filter. The joint switching of M_4 by SW_I and M_7 by PH_I, with specific clocking waveforms, modulates the signal current equivalent to multiplying the signals by a set of I/Q local-oscillator signals (the details are described together with the clock generator in the next subsection).

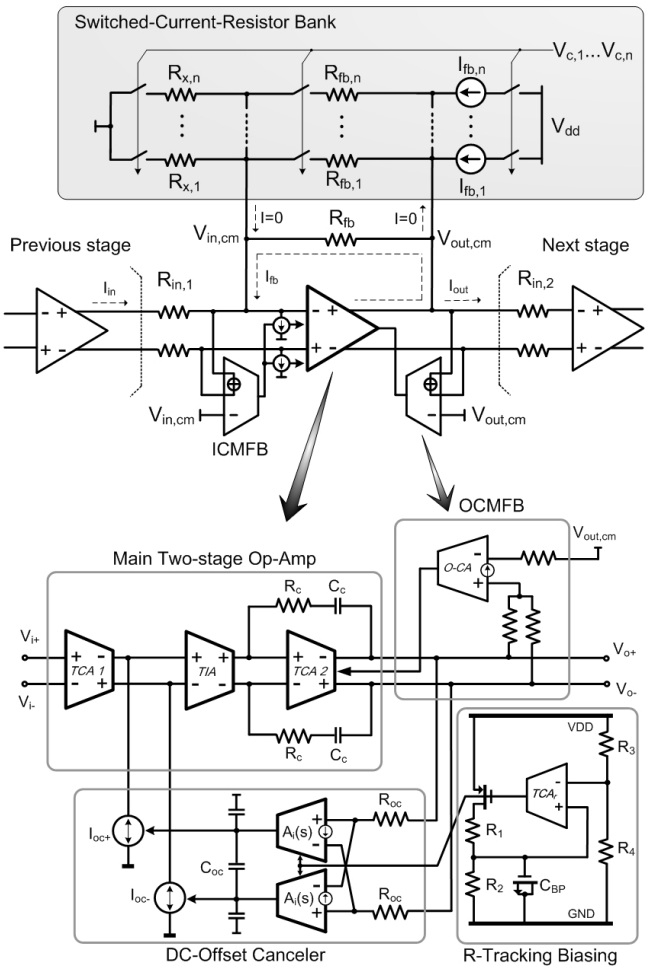

Fig. 7 Gain-programmable amplifier with offset-canceler embedded op-amp.

After mixing, *I-V* conversion and filtering are performed by for the succeeding filter. The bandwidth adjustability for different standards is assigned to R_{BW} because of minimum nonlinearity penalty as they experienced very small signal swing and no potential difference. R_{BW} is a switched-resistor bank with 100 steps controlled by 7 bits.

One more identical filter is cascaded behind the stage after withdrawal of the modulator to obtain the required stopband rejection. The gain distribution between the two filters is 12-dB front and 10-dB back, which are optimized to fulfill the noise and linearity specifications.

5.2 Mixed-Signal I/Q Clock Generator

The major source of I/Q mismatch is the phase and gain mismatch of the I/Q local-oscillator signals. Fig. 6 shows both the block diagram and schematic of the proposed mixed-signal I/Q clock generator that is inherently I/Q-mismatch insensitive.

The D-flip flops, *D1* and *D2*, followed by a simple non-overlap-clock generator produces the two equal-duty-cycle out-of-phase main clocks, which are used to drive the switch M_7. Since the two main clocks can only have two possible analog values (i.e., the supply rails) and the generation is fully symmetrical, the gain mismatch can be neglected. To general the 90º phase shift, an

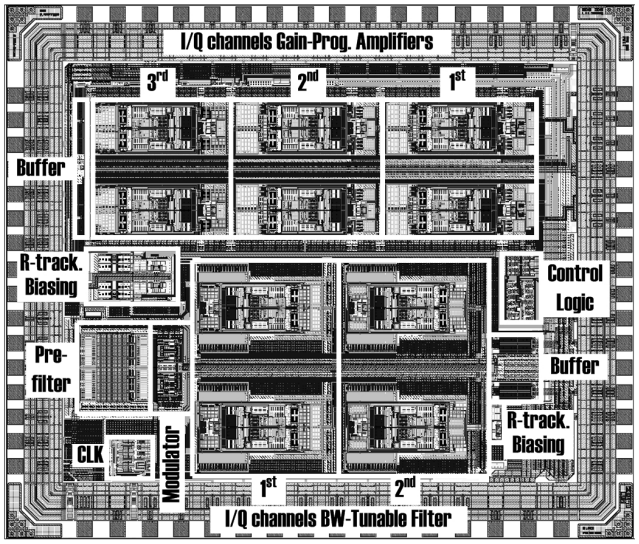

Fig. 8 Layout plot.

auxiliary clock stream is designed to drive switch M_4, which are divided from the same main clock with *D3*, and having 90º phase shift of each other by the cooperation of inverter *N1*, *D4* and *D5*. It is noted that the inverter *N1* can induce phase error between the two quadrature-phased clocks. However, it is unimportant because when they are swapping the differential terminals (by switches M_4 and M_5); the main clocks are always in the zero-crossing. Thus, the tolerable timing mismatch can be as large as half of a period of the main clock. In this work, it is 25ns! Such a large value enables the clock generator passes all process and component-mismatch corners. In addition, the non-overlap and double-switching features of the mixing provides another three benefits: 1) the M_4 can be designed big in their size for better matching and linearity because only the M_7 contribute charge injection. 2) Clock-to-modulator isolation keeps high even they have the identical frequency. 3) The parasitic capacitance associated on the M_4 can be auto-reset by the M_3 and the M_6 every time the PH_1 is not high, which eliminates the memory effect so as to improve the output spectrum purity.

The logic operations after *D5* are used to implement the channel selection. Swapping the phases (i.e., 0º or 180º) of the quadrature phase output obtains the pseudo positive-sine or negative-sine waves for selecting either the upper or lower sideband. In this way, the channel selection is transparently performed on the control path, without generating any transient effects on the signal path.

The cost of such a mixed-signal I/Q clock generation method is the 30% degradation in conversion gain as compared with the conventional one, which, however, does not tolerate any timing error.

5.3 Gain-Programmable Amplifier and Offset-Canceler-Embedded Op-Amp

Voltage-mode inverting amplifier (IA) has been used for many years for programmable-gain control. Tuning the forward and/or feedback impedance levels can achieve variable gains, but results different feedback factors. Variation in feedback factor makes gain-dependently change in closed-loop bandwidth, phase response, and linearity performance.

The proposed low-voltage constant-feedback-factor IA is shown in Fig. 7. The principle is described as follows: by adding the

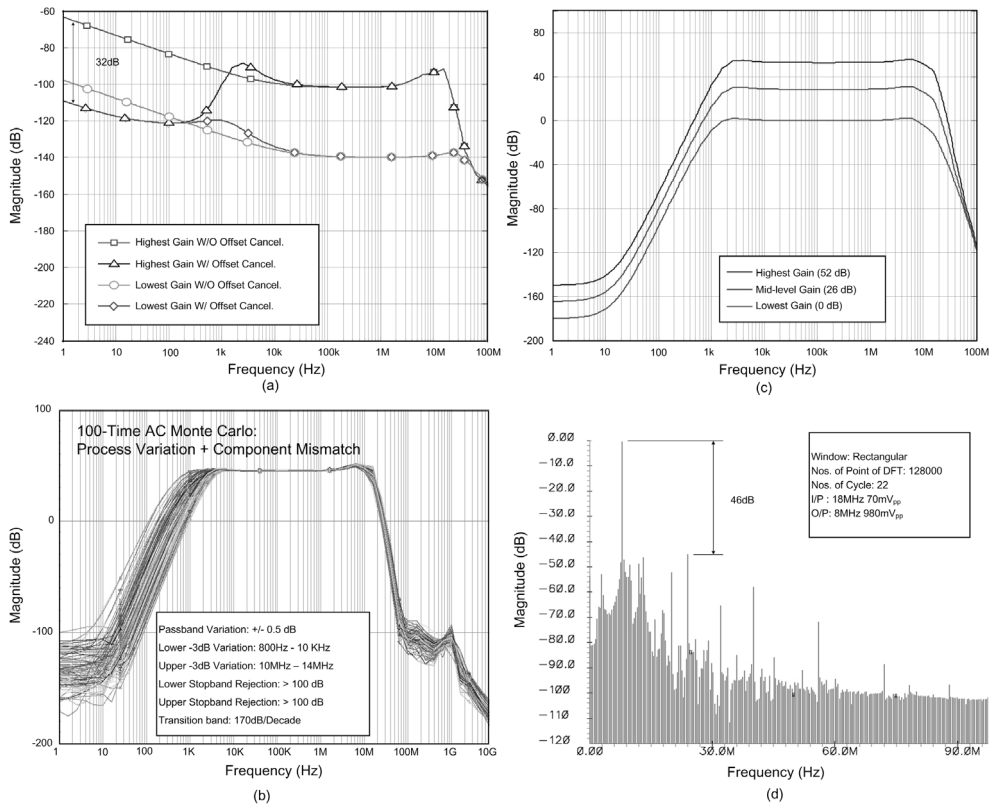

Fig. 9 Post-layout simulation results. (a) Output noise (zero-IF). (b) AC response (zero-IF). (c) Monte-Carlo AC responses (zero-IF). (d) FFT response (low-IF).

highlighted switched-current-resistor bank to the IA, the gain-changing-induced direct current (I_{fb}) flows from the op-amp output to its input can be maintained constant. Like this, first, the output swing of the op-amp can be kept constant as well, and second, the input and output common-mode feedbacks (ICMFB/OCMFB) will not track the current sourcing or sinking at every gain steps. Thus, the stability can be improved and power consumption can be minimized. Another advantage is on the feedback factor β, which can maintain constant for all gain or attenuation levels by selecting the $R_{x,n}$ satisfy,

$$\beta = \frac{R_{in,1} // R_{x,1} \cdots // R_{x,n}}{R_{in,1} // R_{x,1} \cdots // R_{x,n} + R_{fb} // R_{fb,1} \cdots // R_{fb,n}} = \frac{V_{in,cm}}{V_{out,cm}} \quad (1)$$

Another two stages are cascaded together, offering totally -22 to 30 dB amplification/attenuation controllability with 2-dB step size.

For the two-stage op-amp, the front stage consists of a transconductance amplifier, *TCA1*, followed by a transimpedance amplifier, *TIA*, whereas the back stage is a *TCA* that compensated by R_c and C_c. In between is an offset canceller. The R_{oc} converts the output voltage to current for the following *gm-C* integrator formed by $A_i(S)$ and C_{oc} to extract the DC imbalance, which then negatively feedbacks to the first-stage output of the op-amp by using two push-pull current sources I_{oc+} and I_{oc-}. Since those current sources are added on the low-impedance nodes, no significant disturbance to the op-amp high-frequency response is achieved. The lower -3dB point is kept practically constant by using a resistance-tracking basing scheme, which nullifies the resistance dependence. The noise generated from the offset-canceler is not significant as it will be lower by the first gain stage (after input referred).

5.4 Layout

The layout plot is shown in Fig. 8 where the main blocks are highlighted. The circuit is under fabricated in *Austriamicro-systems* (AMS) 0.35-μm 4M2P CMOS process. The dual channels, I and Q, occupy an active area of 7.2mm^2 and will be encapsulated in a standard CQFP64. Separated analog and digital *VDDs* with common *GND*, ample substrate contacts and on-chip MOS decoupling minimize the mixed-signal crosstalk and substrate-noise interference. The most noisy clock lines are sandwiched in between *VDD* and *GND* metal plates to minimize the inductance of the current return path. All resistors and capacitors, made by poly for good linearity, are protected by building over *N*-well, and are pieced by using unit element for accurate matching and ease of fine-step tuning.

6. VERIFICATIONS

6.1 Post-Layout Simulation Results

Fig. 9(a)-(b) summarized parts of the post-layout simulation results. The output passband noise density is less than 10μV/Hz, while the 1/*f* noise is suppressed by more than 32 dB by the offset canceler [Fig. 9(a)]. Because the use of the constant-feedback-factor gain-programmable amplifiers, the lower and upper -3dB points remain practically constant at all gain levels [Fig. 9(b)]. The robustness of the chip is demonstrated in a 100-time AC Monte-Carlo simulation [Fig. 9(c)], no dangerous yield is observed. The spurious free dynamic range (SFDR) is 46dB with $0.98V_{pp}$ output swing [Fig. 9(d)]. The power consumption is 30mW (29mW analog, 1mW digital) from 1V.

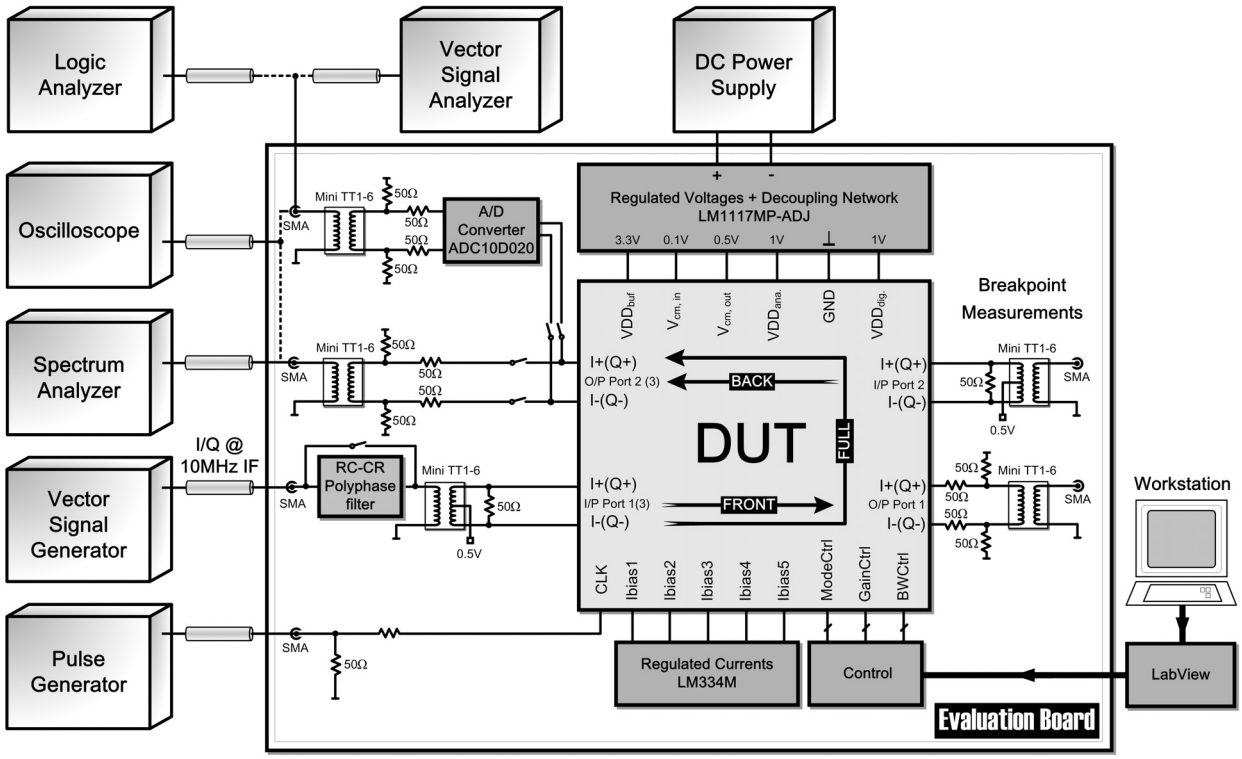

Fig. 10 Test setup.

6.2 Test Plan

Shown in Fig. 10 is the planned testbench. The 1-V core is buffered by a set of 3.3-V source follower, and then impedance matched to the 50-ohm port of the testers. I/Q isolation will be measured by applying the signal only at I or Q channel, while measuring the signals at both of them. I/Q imbalance induced error can be measured by adding artificial mismatch in the hand-constructed *RC-CR* polyphase filter. The fairly large number of pins (64) is due to the computer controls of gain and bandwidth through *LabView*. Thanks to the initial breakpoint assignment, the front-end mixer plus filters and the gain-programmable amplifier are capable to be characterized separately or together without complicated routing. (as labeled: FRONT, BACK, and FULL)

Measurements of the chip under modulated signals will be done by utilizing an *Agilent* E4438C ESG vector signal generator for generating the 802.11a/b/g channel spectrums, and the digitized output (by using two 10-bit 20-MS/s A-to-D converters ADC10D020) will be examined by an *Agilent* 89641 6-GHz vector signal analyzer and/or 16702B logic analyzer, which is synchronized with a 54830D *Agilent* Infiniium oscilloscope. FFT-based spectrum analysis will be done in a *Rohde & Schwarz* FSU8 8-GHz spectrum analyzer with an external tracking generator FSU-B9 for measuring also the magnitude responses.

7. CONCLUSIONS

System-in-package (SiP) technology offered extraordinary design-efficient and lower cost solutions than system-on-chip (SoC) one such as library reusability and crosstalk insusceptibility. Digital chips can constantly trace the nano-CMOS scaling, while analog and mixed-signal ones can be migrated progressively, if overall gains benefits.

This paper demonstrated a low-voltage (1V) low-power (30mW) IEEE 802.11a/b/g–compliant receiver IF-to-baseband chip in 0.35-µm CMOS, which matched the standard supply of pricey 90-nm CMOS to form a low-cost 1-V SiP. The multistandard-compliant was enabled by the low-IF/zero-IF reconfiguration, whereas the low-voltage and low-power operation were the efforts of the circuit techniques that interfaced the analog radio with the digital baseband by using a pre-filter, a double-quadrature I/Q modulator, a two-stage bandwidth-tunable filter, a set of offset-canceler and a three-stage gain-programmable amplifier. All the control units of the analog blocks were replied on the digital processor. Rigorous testing will be performed and the experimental results will be reported in 2005.

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