A 0.127-mm^2, 5.6-mW, 5th-Order SC LPF with +23.5-dBm IIP3 and 1.5-to-15-MHz Clock-Defined Bandwidth in 65-nm CMOS

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***Abstract*—This paper proposes two techniques for improving the linearity and power efficiency of switched-capacitor (SC) circuits. The first is a high-speed *switched-current-assisting (SCA)* path that helps the main (folded-cascode) OTA to deliver most of the desired charge to the *integration capacitor*, leaving the final error correction to be completed by the main OTA. The second is a *pre-charging (PC)* path that assists the main OTA to speed up the charging of the *load capacitor*. Both SCA and PC paths share one auxiliary (differential-pair) OTA that features a high speed-to-power efficiency. The prototype is a bandwidth-scalable 5th-order Butterworth SC lowpass filter (LPF) for software-defined radios. Fabricated in 65-nm CMOS, the LPF exhibits a decade-wide tunable bandwidth (1.5 to 15 MHz) solely defined by the clock, leading to a compact die size (0.127 mm^2). Under the same power (5.6 mW) and bandwidth (10 MHz) targets, the IIP3 reaches +23.5 dBm (+15.3 dBm) and the cutoff accuracy is 97% (82%) with (without) the SCA + PC paths. The achieved Figure-of-Merit (0.014 fJ) compares favorably with the state-of-the-art.**

***Index Terms*—bandwidth, CMOS, linearity, lowpass filter (LPF), operational transconductance amplifier (OTA), software-defined radio, switched capacitor (SC).**

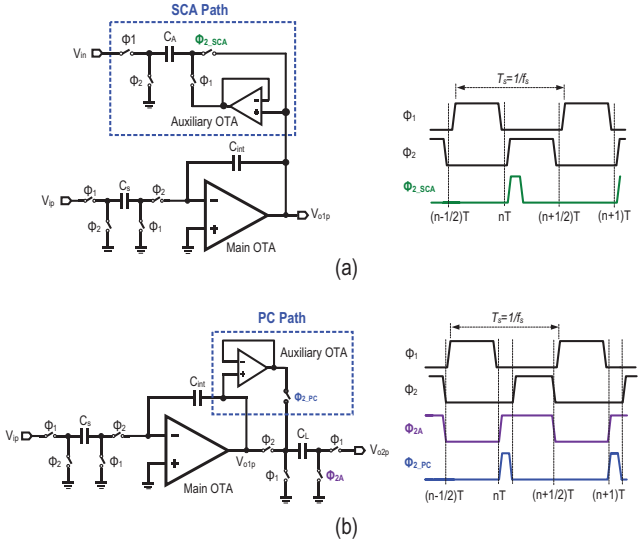

Fig. 1. SC integrator (a) with SCA path, and (b) with PC path.

I. Introduction

The linearity, power and area efficiencies of a bandwidth-scalable low-pass filter (LPF) for software-defined radios are decisively important in order to support a number of wireless applications with low hardware complexity and cost. Although the active-*RC* [1] and g_m-*C* [2] LPFs can fulfill the linearity requirements of most wireless standards, the bandwidth tuning still heavily relies on scaling of supply [3], current [4] and/or switching elements [2]. The former two can lead to variation of more than one parameter, while the latter impacts the chip area that is increasingly expensive in nanoscale CMOS. A better alternative should be the switched-capacitor (SC) LPF [5] that allows wide and continuous tuning of bandwidth solely defined by the clock, avoiding any calibration loop or backup tuning elements. Yet, the passive open-loop SC LPF [5] is mainly suitable for IIR/FIR realization, which can hardly offer a sharp roll-off as the typical active SC LPFs that use operational transconductance amplifiers (OTAs). On the other hand, the main challenges of OTA-based SC LPFs are more on the linearity and bandwidth-to-power efficiency.

This paper introduces a switched-current assisting (SCA) technique and a pre-charge (PC) technique suitable for OTA-based SC circuits like the channel-selection LPF as realized in this work. The basic principles, circuit details and experimental results are presented next.

II. Basic Principles of SCA and PC Techniques for a SC Integrator

For a typical SC integrator [Fig. 1(a), without the SCA path and Φ_{2_SCA}], the input signal (V_{ip}) is captured in the sampling capacitor C_s during Φ_1, while the main OTA should push the sampled charge from C_s to the integration capacitor C_{int} during Φ_2. Obviously, the finite gain-bandwidth product (GBW) and intrinsic distortion of the OTA can result in an imperfect charge transfer in every clock period T_S, degrading the accuracy and linearity of the integrator.

To alleviate the GBW (power) to performance tradeoff, a SCA path is introduced. The SCA path samples the inverting input (V_{in}) in Φ_1 with the help of an auxiliary OTA in unity-gain feedback, which copies V_{o1p} to one plate of C_A to ensure only the desired charge is transferred to C_{int} during Φ_{2_SCA}. In this way, the main OTA only entails to complete the rest error correction task, which is much less speed demanding. To be analytically compared later, it is more beneficial to allocate extra power to the auxiliary OTA than the main OTA.

The SCA path is dedicated for assisting the charging of C_{int}, but a SC integrator in general can also be loaded by another SC branch to continue the signal processing by the subsequent circuitry. To enhance the charging speed of the load capacitor C_L, a PC path [Fig. 1(b)] can be added. Before Φ_2 that entails the main OTA to charge C_L, Φ_{2_PC} allows the

auxiliary OTA to pre-charge C_L. Interestingly, referring to Fig. 1(a), only one extra route from the output of the auxiliary OTA to C_L can render the two techniques combinable in one SC integrator, accelerating the charging time of both C_{int} and C_L more power efficiently.

III. Analytical Comparison of SC Integrators with and without the SCA Path

As the SCA and PC techniques are similar in nature, only the SCA is analyzed and compared. For the settling error resulting from a limited OTA's GBW, we can study the effectiveness of the SCA path using the equivalent circuit of a SC integrator in the integrating phase [Fig. 2(a)], where C_{in}, G_O and C_O denote the OTA's input parasitic capacitance and output conductance, capacitor, respectively. Supposing that $2C_s = C_{int}$, the input V_{ip} of the integrator can be modeled as a negative unit step signal V_{step} applied at the left terminal of C_s. Without the SCA path, the output $V_{o1p}(t)$ can be expressed as (ignore C_{in}, G_O and C_O for simplicty,)

$$V_{o1p}(t) = -\frac{C_S}{C_{int}} \cdot V_{step} \cdot \left(1 - \frac{(1+\frac{C_S}{C_{int}})}{\frac{C_S}{C_{int}}} e^{-\left(\frac{G_{OTA}\,t}{C_S}\right)}\right) \quad (1)$$

The step responses of $V_{o1p}(t)$ under different G_{OTA} (1x, 2x and 4x) are simulated as shown in Fig. 2(b). A better settling accuracy can either be achieved by increasing G_{OTA} or prolonging the integrating time. For high-speed applications, only the former is feasible, leading to a hard tradeoff with the power. Here, the charging speed of the SCA path can be sized to be much faster than that of the main OTA (i.e., only limited by the sizes of C_A and on-resistance of the switches S_{SCA}). Thus, a short SCA operating time (Φ_{2_SCA}) with an anti-phase input V_{in} ($= -V_{ip}$) is adequate to deliver most of the desired charge for the integration. For instance, for a 1% overall settling error, the auxiliary OTA helps settling to 5% error with an extra power of 20% to that of the main OTA. From the following equation:

$$V_{o1p\_SCA}(t) = V_{SCA} + \left(-\frac{C_S}{C_{int}} \cdot V_{step} - V_{SCA}\right) \cdot \left(1 - \frac{(1+\frac{C_S}{C_{int}})}{\frac{C_S}{C_{int}}} e^{-\left(\frac{G'_{OTA}\,t}{C_S}\right)}\right) \quad (2)$$

V_{SCA} is the voltage set up by SCA path. The required total G_{OTA} can be decreased from $\frac{14.26 \cdot C_S}{t_{clk}}$ to $\frac{8.12 \cdot C_S}{t_{clk}}$. Therefore the speed-to-power efficiency is improved 1.76X, thanks to the fast settling of V_{SCA} of the SCA path. Indeed, the main OTA is primarily response to the error correction from 5% to 1%.

The linearity of a SC integrator is normally limited by the gain nonlinearity of the main OTA. Fig. 2(c) shows the ratio of V_x/V_{ip} under the step responses with different G_{OTA}. The peak value of V_x can be expressed as a function of V_{ip}, C_s, C_{in}, C_{int} and C_O, and is weakly dependent on G_{OTA}. With a large V_{ip}, the weak nonlinearity of the main OTA can be modeled at the output current as follows (assuming differential realization),

$$i_o = G_{OTA} \cdot V_x + G_{OTA3} \cdot V_x^3 \quad (3)$$

where the 3rd-order term comes from the integration of the current. Traditionally, to improve the linearity, G_{OTA} can be boosted to shorten the settling time of V_x/V_{ip}. The proposed SCA path, in a different way, enhances the linearity by *canceling* the voltage at the input of the main OTA. As a result, the virtual ground remains close to zero [black curve in Fig. 2(c)] during the entire integration window, thereby lowering the distortion generated by the main OTA.

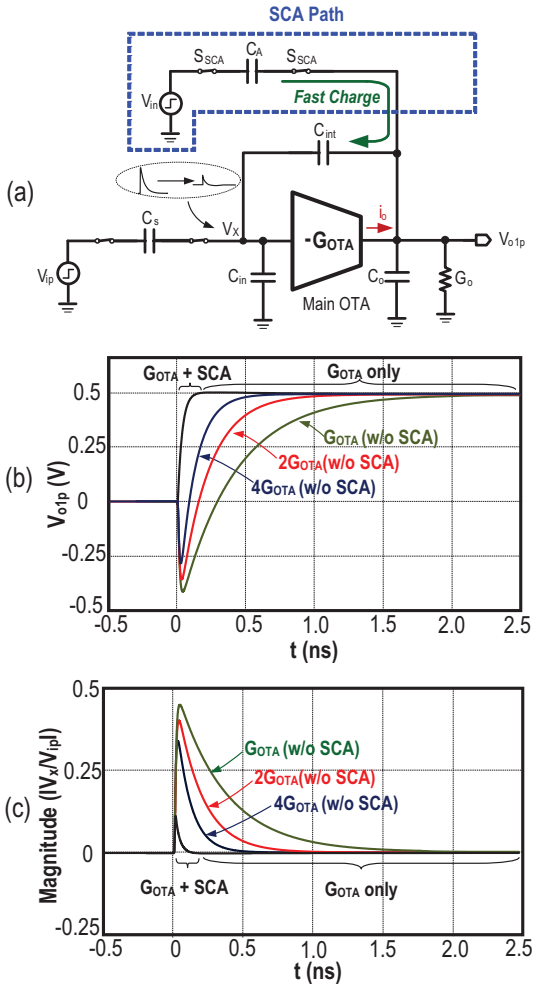

Fig. 2 (a) SC integrator with the SCA path. (b) V_{o1p} under a step response. (c) V_x/V_{ip} under a step response.

Although the SCA and PC paths also induce noise and non-linearity penalties [1], they are more manageable as both are operated at the output node of the integrator and are turned ON only in a short period. It can be determined that, by optimally sizing C_A amongst the different trade-offs, the SCA path can be made insignificant (confirmed by simulations) to the overall noise and linearity metrics of the SC integrator. Detailed proofs are omitted here due to space constraints.

IV. A 5TH-Order Butterworth SC LPF Prototype

The proof-of-concept prototype is a fully-differential 5th-order Butterworth SC LPF targeting one-decade bandwidth tunability from a few MHz (WCDMA) to over 10 MHz (WLAN). It is structured with one Uniquad and two Biquads in

cascade (Fig. 3). To maximize the dynamic range, the high-Q (1.62) Biquad is located at the last stage minimizing the swing at internal nodes. The SCA and PC paths can be disabled such that their effectiveness can be assessed fairly. The optimized unit capacitor C_{unit} is 288 fF, which balances the layout efforts with the required matching in the employed ST GP/LP 65-nm CMOS technology.

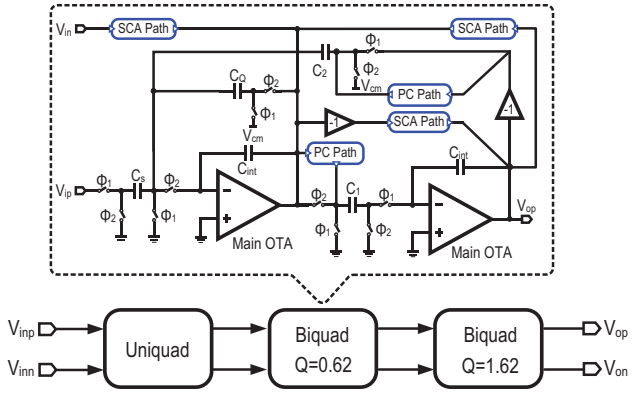

Fig. 3. Simplified block diagram of the LPF with SCA + PC paths.

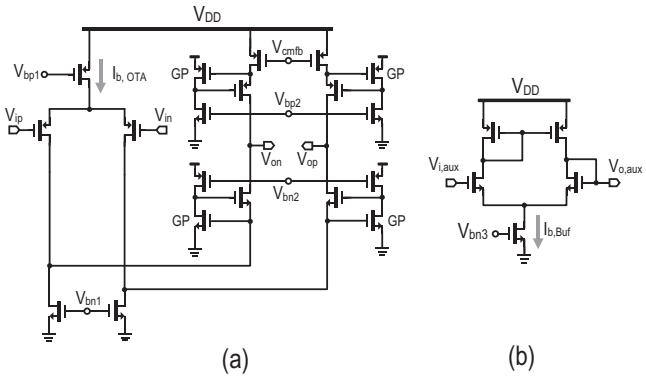

Fig. 4. (a) Main OTA and (b) auxiliary OTA.

To optimize the speed-to-power efficiency the main OTA [Fig. 4(a)] is based on a single-stage folded-cascode topology with local gain boosting. Each gain-boosted cell features one GP device sized with a long channel length (L = 180 nm) to lower their threshold voltages, leveraging the limited output swing of such OTA architecture. A continuous-time common-mode feedback circuit was chosen for its better power supply rejection at high frequency. The total bias current of the main OTA is 500 µA, which results in a 64-dB DC gain and a 380-MHz unity-gain frequency (UGF) at a 600-fF capacitive load. The auxiliary OTA [Fig. 4(b)] is a simple differential pair with a current-mirror load, showing a 31-dB DC gain and a 150-MHz UGF at a 600-fF capacitive load. $I_{b,Buf}$ is 100 µA (~20% of that of the main OTA).

The clock generator is based on a typical non-overlapping scheme (not shown) with proper delay cells and AND/OR functions to realize all required phases. Proper device sizing ensures correct operation over a wide range of clock rate, with a power efficiency of 6.5 to 14 µW/MHz.

V. Experimental Results

Fig. 5 shows the die micrograph of the SC LPF. Because of no tuning elements for bandwidth control, the active die area is very compact (0.127 mm^2, excluding the test buffer). The factual performance of the LPF is properly de-embedded using the testbrench reported in [6]. The signal path is powered at 1.2 V for better overdrives and signal swing, whereas the clock generator is operated at 1 V for lowering the dynamic power.

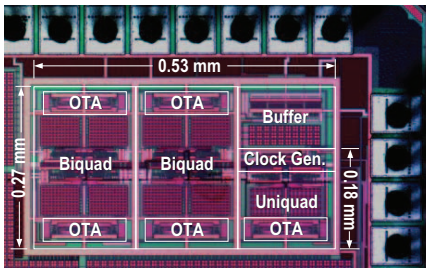

Fig. 5 Die micrograph of the fabricated 5th-order SC LPF.

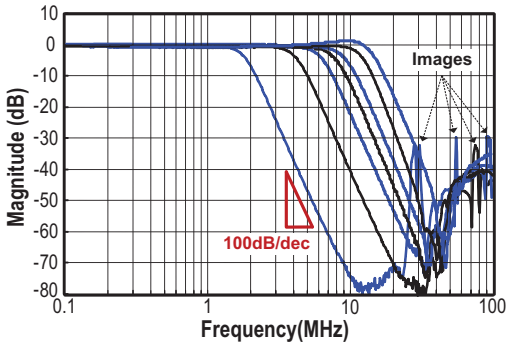

Fig. 6 Measured normalized gain responses at different clock rates from 30 to 350 MHz.

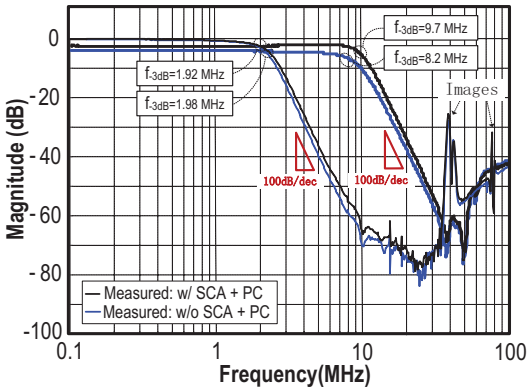

Fig 7. Measured gain responses with and without the SCA + PC techniques. The targeted cutoffs are set at 2 and 10 MHz by the clock.

Solely set by the clock rate the SC LPF measures a consistent 100-dB/decade stopband rejection profile (Fig. 6) over a wide range of bandwidth from 1.5 to 15 MHz (upper-limited by the main OTA's GBW). The corresponding power consumption rises from 2.3 to 7.8 mW. The normalized gain

responses at 2-MHz and 10-MHz –3-dB cutoff frequencies, with and without the SCA and PC paths, are plotted in Fig. 7. For the 10-MHz target, the passband gain is improved from –4 to –2.3 dB, while cutoff accuracy is enhanced from 82% to 97%. The measured input-referred noise density (IRN) is roughly the same (35 nV/√Hz) with and without the SCA + PC techniques as expected.

The in-band linearity is assessed at the 10-MHz bandwidth. With a two-tone test (5 MHz and 5.2 MHz) applied, the IIP3 can be improved from +15.3 dBm to +23.5 dBm after enabling the SCA and PC paths as shown in Fig. 8.

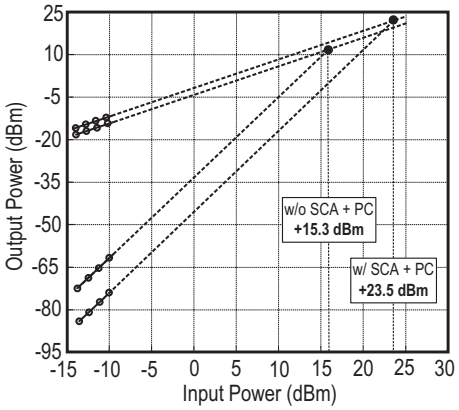

Fig. 8 Measured IIP3 with and without the SCA + PC techniques.

Table I. Effectiveness of the SCA + PC Techniques.

		Without SCA + PC	With SCA + PC
Power @ 10 MHz Bandwidth	Main OTA	4.2 mW	3.0 mW
	Auxiliary OTA	N/A	1.2 mW
	Clock Gen.	1. 4 mW	1. 4 mW
	Total	5.6 mW	5.6 mW
Cutoff Accuracy @ 10 MHz		82%	97%
In-band IIP3		+15.3 dBm	+23.5 dBm
-1-dB Compression Point		+5.2 dBm	+7.9 dBm
IRN		35 nV/√Hz	35 nV/√Hz

Table II. Performance Comparison with the State-of-the-Art.

	This Work	JSSC'11 [2]	ISSCC'12 [3]	JSSC'09 [4]	ISSCC'13 [5]
Technology	65 nm	90 nm	90 nm	180 nm	65 nm
Architecture	Active SC + SCA + PC	Gm-C	Ring Osc. Integrator	Gm-C	Gm + Passive SC
Filter Order, *N*	5th, Butterworth	6th, Butterworth	4th, Butterworth	3rd, Butterworth	7th, IIR
Bandwidth (MHz), BW	1.5 to 15	8.1 to 13.5	7 to 30	0.5 to 20	0.4 to 30
Bandwidth Tuning	Clock Rate	Coarse (Cap Bank) Fine (Bias Current)	Supply Voltage	Bias Current	Clock Rate
In-Band IIP3 (dBm)	**+23.5 @ 10MHz BW**	+22.1 @ 10MHz BW	16.7@ 7MHz BW	+20.5 @ 10MHz BW	+16 @ 2.9MHz BW
IRN (nV/√Hz), P_N	35	75	23.7 to 32.8	12 to 425	2.85
Area/Pole (mm²/Pole)	**0.0254**	0.04	0.0725	0.077	0.06
Power (mW), P_C	2.3 to 7.8	4.35	2.9 to 19.1	4.1 to 11.1	1.96
FOM (fJ) *	**0.014**	0.024	0.0228	0.072	0.00038

$$* \text{FOM} = \frac{P_{C/N}}{BW \cdot \left(\left(\frac{IIP3}{P_N}\right)^{2/3} \cdot N^{4/3}\right)}$$

The performance summary with and without the SCA + PC techniques is given in Table I, whereas the comparison with the state-of-the-art solutions [2-5] is given in Table II. This work is advantageous for its: 1) highest linearity without sacrificing the power; 2) best area-per-pole efficiency being very suitable for nano-scale CMOS realization; 3) easy bandwidth scaling solely defined by the clock rate (no calibration nor backup elements); and 4) competitive figure-of-merit (FOM) to other Butterworth LPFs [2-4] except the IIR [5], which suffers from a slow stopband roll-off degrading the passband gain.

VI. CONCLUSIONS

Two circuit techniques have been proposed for improving the power-area efficiency and linearity of SC circuits. The SCA path helps the main OTA to deliver most of the desired charge to the integration capacitor, whereas the PC path speeds up the charging of the load capacitor. Both share one auxiliary OTA that leads to an improved SC integrator with better linearity and cutoff accuracy. The proof-of-concept prototype is a 5th-order Butterworth SC LPF fabricated in 65-nm CMOS. It measures a decade-wide tunable bandwidth from 1.5 to 15 MHz solely controlled by the clock. The corresponding power consumption is from 2.3 to 7.8 mW. Because of no extra tuning element, a compact die size is achieved (0.127 mm^2). At a 10-MHz bandwidth, the low power consumption (5.6 mW), high IIP3 (+23.5 dBm) and low IRN (35 nV/√Hz) correspond to a competitive FOM (0.014 fJ). The SCA and PC techniques are applicable to other circuits like SC delta-sigma modulators.

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REFERENCES

[1] S. V. Thyagarajan, S. Pavan and P. Sankar, "Active-RC Filters Using the Gm-Assisted OTA-RC Technique" *IEEE J. Solid-State Circuits*, vol.46, no. 7, pp. 1522–1533, Jul. 2011.

[2] M. S. Oskooei, N. Masoumi, M. Kamarei, and H. Sjoland, "A CMOS 4.35-mW, +22-dBm IIP3 Continuously Tunable Channel Select Filter for WLAN/WiMAX Receivers" *IEEE J.Solid-State Circuits*, vol.46, no. 6, pp. 1382–1391, Jun. 2011.

[3] B. Drost, M. Talegaonkar, and P.K. Hanumolu, "A 0.55V 61dB-SNR 67dBSFDR 7MHz 4th-Order Butterworth Filter Using Ring-Oscillator-Based Integrators in 90nm CMOS," *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, *Digest*., pp. 360-362, Feb. 2012.

[4] T. Lo, C. Hung, and M. Ismail, "A Wide Tuning Range G_m-C Filter for Multi-Mode CMOS Direct-Conversion Wireless Receivers," *IEEE J.Solid-State Circuits*, vol. 44, no. 9, pp. 2515–2524, Sep. 2009.

[5] M. Tohidian, I. Madadi, and R. B. Staszewski, "A 2mW 800MS/s 7th-Order Discrete-Time IIR Filter with 400kHz-to-30MHz BW and 100dB stop-band rejection in 65nm CMOS," *IEEE Int. Solid-State Circuits Conf. (ISSCC)* , *Digest*., pp. 174-175, Feb. 2013.

[6] S. Pavan and T. Laxminidhi, "Accurate Characterization of Integrated Continuous-Time Filters," *IEEE J. of Solid-State Circuits*, vol. 42, no. 8, pp. 1758–1766, Aug. 2007.