A 2×V_{DD}-Enabled TV-Tuner RF Front-End Supporting TV-GSM Interoperation in 90nm CMOS

Pui-In Mak and R. P. Martins [1]

Analog and Mixed-Signal VLSI Laboratory, FST, University of Macau, Macao, China (E-mail: pimak@umac.mo)
1 – On leave from Instituto Superior Técnico (IST) / TU of Lisbon, Portugal

Abstract

Presented is a 2×V_{DD}-enabled 90nm-CMOS TV-tuner RF front-end consisting of a power-efficient *cascode-cascade-inverter* LNA, a linearized *C*-2*C* attenuator using a reliably-overdriven control, dual cascode I/Q mixer drivers and an inductive-peaking gain-roll-off compensation path. In TV-GSM-inter-operation mode, the circuit incooperating with a customized preselect filter exhibits a 46dB gain range, 68dB rejection at GSM-900 uplink, –5.5dBm IIP3, and 3.9dB noise figure at 26.2dB gain. The 0.28mm^2 core draws 15mW.

I. Introduction

Enabled by ultra-scaled CMOS featuring high-f_T transistors, wideband RF front-ends emerge as a low-cost approach to realize multistandard radios [1]. Concurrent reception over a wide spectrum demands the RF circuits to feature high linearity. This paper describes a 170-860MHz multistandard TV-tuner RF front-end using V_{DD}-upscaled RF techniques to improve the power efficiency and linearity. Needless of specialized devices, the limitations induced by insufficient voltage headroom can be resolved economically. The targeted mobile TV applications are T-DMB, DVB-H, ISDB-T and MediaFLO and both typical and TV-GSM-interoperation are supported. The voltage stressed on each device is restrained within the detrimental reliable limits, which include the absolute maximum rating (AMR), negative bias temperature instability (NBTI), hot carrier injection (HCI), time dependent dielectric breakdown (TDDB) and electrostatic discharge (ESD). Counting them in the formation of each block ensures the device reliability even under an elevated V_{DD}, while creating other possibilities for performance optimization.

II. System Design

The stress-conscious differential RF front-end (Fig. 1) relies on a LNA, a *C*-2*C* attenuator, dual I/Q mixer drivers and a gain-roll-off compensation path. Unlike the synthesis of full-band (48-860MHz) TV tuners [1] that entail RF tracking filter or up-down superheterodyne to resolve the problem of harmonic mixing, mobile-TV tuners covering just 170-860MHz have a relaxed requirement on it. In fact, only the VHF-III band (170-240MHz) suffers from the problem; channels in UHF band (470-860MHz), after mixing with a rail-to-rail local oscillator featuring strong 3rd and 5th harmonics, become the co-channel interferers of VHF III band. Targetting a harmonic rejection ratio of 60dB, a concurrent use of separated preselect filters and a polyphase mixer scheme is reliable to meet the goal, avoiding needing interstage off-chip components.

In TV-GSM co-integrated handhelds, the presence of GSM-900 uplink poses a stringent rejection profile to the TV-Tuner preselect filter. The typical isolation between the TV tuner and GSM transceiver is limited to 10dB. A commercial TV-tuner filter [2] offering just 30dB notching at 900MHz is inadequate to meet the goal (58dB). Moreover, due to a limited *Q* factor, the passband is sloped by the notching. In this work, in order to prevent intermodulation distortion induced by the GSM uplink (with a power level up to +33dBm), while maintaining a flat passband, a customized external preselect filter and a gain-roll-off compensation technique are enforced. They together lead to high rejection at GSM uplink and a flat passband concurrently.

III. Circuit Design and Simulation Results

The LNA is structured with 4 inverters (A_1-A_4) in cascode-cascade configuration to cope with the 2×V_{DD} and enhance the

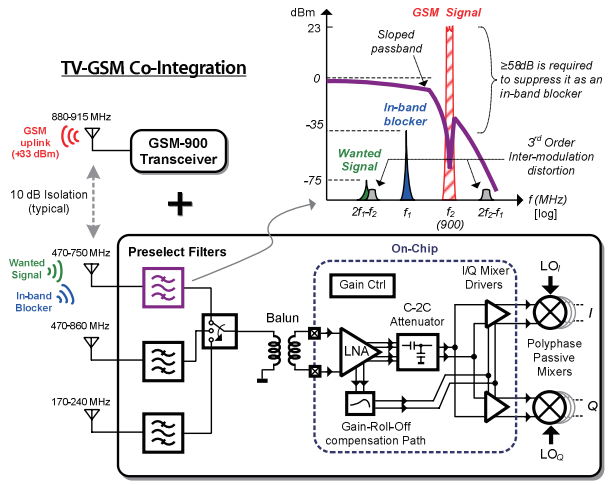

Fig. 1 TV-tuner RF front-end supports VHF III (170-240MHz), UHF (470-860MHz), and narrower UHF (470-750MHz) for TV-GSM interoperation.

power efficiency (Fig. 2). Each inverter operates at a net voltage of 1×V_{DD} and is self-biased by feedback resistor R_{fb}. N_X is of low impedance offering a simple wideband input match. *Double capacitive cross-coupling* boosts the effective transconductance (G_m) of A_1 and A_2 by roughly 3× when comparing with a single transistor. Proper sizings led to matched terminal voltages, i.e., $|V_{DS}|=|V_{GD}|=|V_{GS}|=0.5\times V_{DD}$. Given the transistor threshold $|V_T|\approx$ 0.3V, the G_m-to-I_{b1} ratio is ~30V^{-1}, and the reliable output swing of each inverter reaches 0.6V_{pp} according to the 10-year lifetime guidelines of AMR, HCI, NBTI and TDDB. A_3 and A_4 are made bypassable for a low-gain option. Mode changing by *SW* entails no shift of bias points, assuring LNA's reliability. N_X biased midway the supply offers the flexibility in improving the ESD robustness, i.e., 3 vertical substrate PNP diodes (D_3's and D_4's) together with the reverse diodes (D_1 and D_2) and power clamp ensure that the RF inputs can withstand ±4kV human body model zapping tests. The induced parasitic capacitance is 0.2pF. The linear input swing retains rail-to-rail at a 0.1% THD.

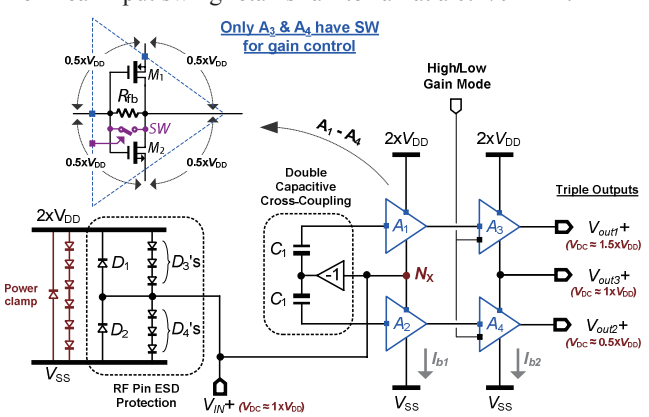

Fig. 2 2×V_{DD} cascode-cascade-inverter LNA with ESD protection.

The coarse-gain control is based on a linearized passive *C*-2*C* attenuator using a reliably-overdriven control (Fig. 3). The input capacitor is split into two for passively combining the LNA's upper (V_{out1}+) and lower (V_{out2}+) outputs. The attenuation range is from 0 to –30dB with –6dB/step. The elevated V_{DD} offers extra voltage headroom to overdrive all switches, minimizing their size and induced nonlinearity. The main reliability concern

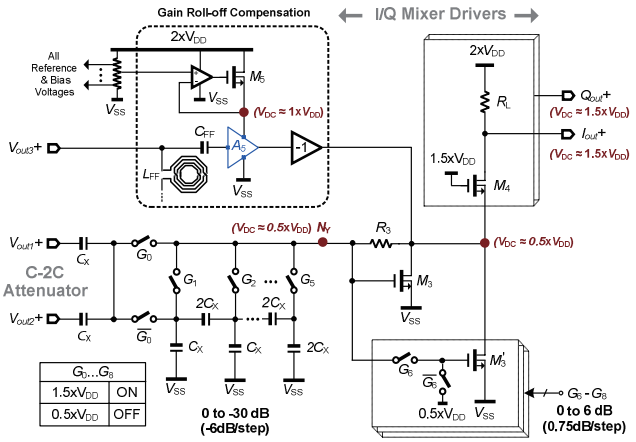

Fig. 3 *C*-2*C* attenuator, I/Q mixer drivers and gain roll-off compensation path.

is NBTI because all switches conduct no static current, and to overcome it, switches are realized by triple-well NMOS as they are far less affected by NBTI than PMOS. The terminal voltage N_Y is set to $0.5\times V_{DD}$. With such, all gain-control logics [G_0-G_8] can be reliably up-shifted to $1.5\times V_{DD}$ in ON-state, leading to ≥7.3dB improvement of IIP3 among the gain-control range. A simple resistor ladder realizes the required level shifting.

The low-impedance output node V_{out3}+ (Fig. 2) is exploited for gain-roll-off compensation. Confirmed by on/off-chip co-simulation, a feedforward path from V_{out3}+ with inductive peaking (by L_{FF}) and amplification (by A_5) realizes a low-Q highpass characteristic, counteracting the passband roll-off induced by the preselect filter. L_{FF} is a symmetrical inductor achieving higher inductance at lower area usage. An error amplifier loop around M_5 offers a regulated $1\times V_{DD}$ to drive A_5.

The dual I/Q mixer drivers (Fig. 3) using a cascode structure benefit the most from an elevated V_{DD}. The cascode NMOS device M_4 having V_{GS}=V_{DS}=$1\times V_{DD}$ is of long channel length (L=1.2μm) to avoid NBTI and punchthrough, while retaining HCI and TDDB reliabilities. A $0.6V_{pp}$ linear output swing is attained without jeopardizing the reliability limits in terms of RF stress [3]. This structure shows 3dB higher IIP3 and 45dB better reverse isolation than a typical $1\times V_{DD}$ common-source amplifier dissipating the same power. The fine-gain control uses the AC-switching part of M_3 (i.e., M'_3), covering a 0 to 6dB gain range with 0.75dB/step. Again, all bias points are unaltered against gain. A resistor ladder generating all reference and bias voltages avoids wrong voltage buildup (remove) sequences during power-on (off) transients.

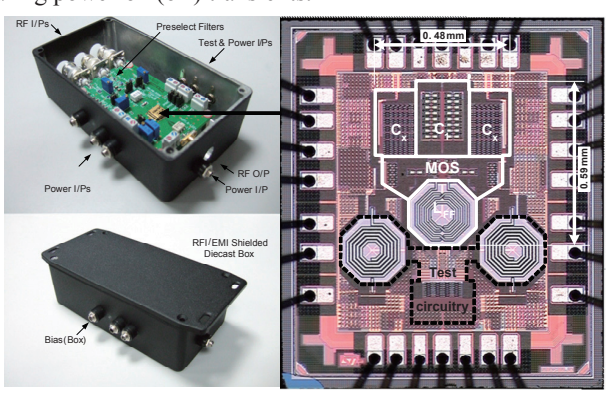

Fig. 4 Fixture for resisting the ambient GSM signals and chip micrograph.

IV. Experimental Results and Benchmarks

The fixture for resisting the ambient GSM signals in tests and the chip micrograph are shown in Fig. 4. The die occupies $0.28mm^2$ and is filled symmetrically by obligatory dummy tiles to flatten the mechanical strain. The RF performances were tested with three different preselect filters, but, due to a limited space, only the results for TV-GSM interoperation are presented in details (Fig. 5). The voltage gain is 26.2dB and the noise figure (NF) is 3.9dB. The in-band $|S_{11}|$ is <–10dB. The rejection at GSM uplink is 68dB, while inducing 0.7dB roll off in 470-750MHz. Figure 6(a) and (b) show the voltage gain and gain error, NF and IIP3, measured against the gain control words. The gain step error is <±1dB in a 46dB gain range. When the LNA is switched to low-gain mode, an IIP3 of ≧–1.6dBm with a NF of 6.4dB is adequate to pass the DVB-H L1 test with low senstivity loss. The circuit core draws 15mW. No performance degradation was noted after three days of continous operation. Comparing with the prior arts [4]-[6] (Table I), this work is advantageous for its lowest power consumption, multistandard conformity and TV-GSM interoperability.

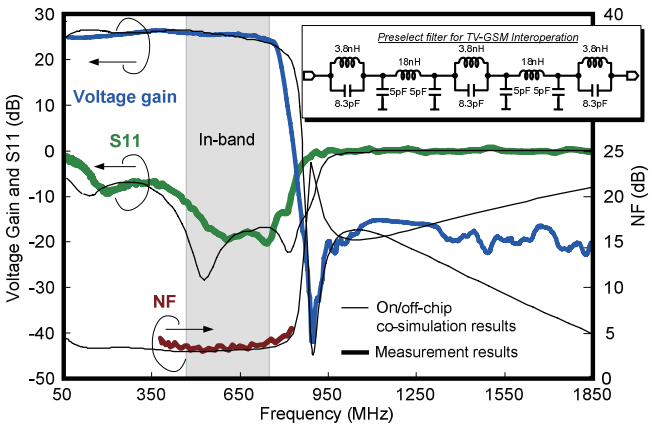

Fig. 5 Measured and simulated RF performances under the use of a 470-750MHz preselect filter for TV-GSM interoperation.

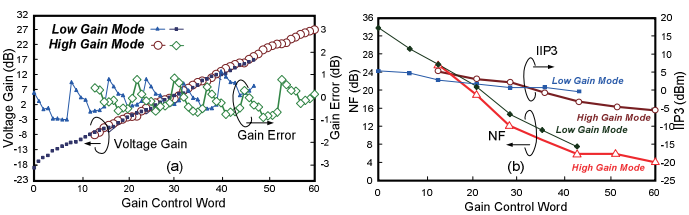

Fig. 6 (a) Voltage gain, gain error, (b) NF and IIP3 versus gain steps at 600MHz.

Table I. Performance summary and comparison with the prior arts.

	This work			L. Tripodi et al ESSCIRC'07 [4]	J. Xiao et al JSSC' FEB 07 [5]	T. Kim et al VLSI'05 [6]	
Frequency (MHz)	170 – 240	470 – 750	470 – 862	470 – 862	470 – 870	174 – 245	450 – 862
NF (dB)	3.8	3.9	3.5	2.6	4.3	3.0	4.5
Max. Voltage Gain (dB)	24.9	26.2	26.5	23	16	28	25
Rejection at GSM-900 uplink (dB)	67	68	2	n/a	n/a	n/a	n/a
ESD Protection/level (V)	Yes / 4k[1]			no	no	Yes / n/a	
IIP3 (dBm) @ gain	–5.5 @ 26.2 –1.6 @ 16 (low-gain mode)			–5.4 @ 23 +0.6 @ 9	–1.5 @ 16	–5 to –4 @ 25	
Variable Gain Range (dB)	46			14	33	50	
Power (mW) @ V_{DD} (V)	10 @ 2 (LNA + C-2C Attenuator) 15 @ 2 (+ also I/Q Mixer Drivers)			40 @ 1.2	22 @ 1.8	16 @ 1.8	
Active Area (mm^2)	0.283 (include I/Q Mixer Drivers)			0.067	0.32	0.52	
Circuit Topology	Differential			Single-End in Differential Out	Single End	Differential	
Technology	90nm CMOS			90nm CMOS	0.18μm CMOS	0.18μm CMOS	

1 - The ESD protection level is based on human body model (HBM) simulation

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