A Charge Pump Based Timing-Skew Calibration for Time-Interleaved ADC

Peng Zhang[1, 2], Zhijie Chen[1,2], He-Gong Wei[2], Sai-Weng Sin[2], Seng-Pan U[2], Zhihua Wang[1], Rui Paulo Martins[2, 3]
1. Institute of Microelectronics, Tsinghua University, Beijing, China
[1]mb05512@umac.mo
2. Analog and Mixed Signal VLSI Laboratory, FST, University of Macau, Macau, China
[2]TerrySSW@umac.mo
3. On leave from Instituto Superior Técnico/TU of Lisbon, Portugal

***Abstract*—This paper presents a background-calibration technique of timing skew for time-interleaved analog-to-digital converters (TIADCs). Without any kind of additional calibration signals, the timing skew between any two adjacent interleaved channels is detected by the capacitive charge pumps, and minimized by the digitally controlled delay elements (DCDEs). The calibration behaviors are analyzed and verified on transistor-level simulations. An 8-bit 4-channel TIADC is used as an example for demonstration. The simulation results show that the proposed technique can improve the SNDR from 35.1 dB to 49.6 dB at Nyquist input frequency as the extreme case.**

***Index Terms*—timing skew, calibration, ADC, time-interleaved (TI), charge pump**

I. INTRODUCTION

Digital signal processing systems operating on analog signal inputs are often limited by the sampling rates of analog-to-digital converters (ADCs). For the purpose of considerable increase of an ADC's sampling rate, a time-interleaved ADC (TIADC) system is universally used [1]. Unfortunately, the overall signal-to-noise-plus-distortion ratio (SNDR) of TIADCs is often extraordinarily degraded by timing-skew errors induced by the device mismatch in the delay units or clock buffers, as well as the mismatch among clock signal routes. For instance, a four-channel 8-b 1.6 GS/s TIADC requires the skew as small as 0.71 ps (rms) to attain an SNDR of 49-dB. This requirement is difficult to achieve especially for chips fabricated by advanced nanometer CMOS technologies with down-scaled device size.

Previously, in order to address the issue of timing-skew errors, a front-end sample-and-hold amplifier (SHA) is implemented in front of all the interleaved channels [2], but the SHA has to operate at stringent speed, accuracy and low-noise environments, leading to the enormous power. Various calibration technologies were proposed to overcome the problem, including two processes of the error detection and correction. The timing skew can be measured by using a foreground-calibration signal [3], such as ramp signal, or by blind estimation method [4]. When the timing skew has been measured accurately, the error correction can be done by analog methods which adjust the sampling clock phase slightly.

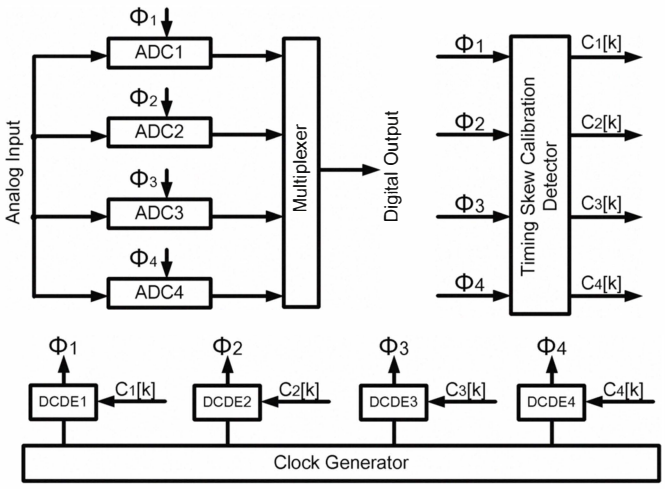


Fig. 1. The timing-skew calibration with a four-channel TIADC

This paper presents a low-complexity timing-skew calibration technique, of which circuits can be all implemented on transistors without any kind of calibration signals. A charge pump and a comparator are utilized to measure timing skews among the channels of a TIADC. Based on the proposed timing-skew measurement, we can employ a self correction loop, adjusting the sampling clock phase, to significantly reduce the negative influence of timing skew. Transistor-level simulation has been provided on the case of a four-channel TIADC in order to verify the proposed technique.

The rest of this paper is organized as follows. Section II introduces the calibration architecture with the TIADC. Section III describes the implementation of the proposed timing-skew calibration. Section IV presents the simulation results and section V gives the conclusion finally.

978-1-61284-857-0/11/$26.00

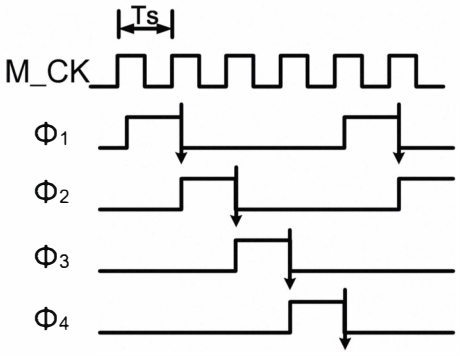


Fig. 2. Timing diagram of four-channel TIADC

II. CALIBRATION ARCHITECTURE

Fig. 1 shows the block diagram of the calibration architecture with the TIADC, consisting of four ADCs in parallel, ADC_1 to ADC_4, a digital multiplexer at the output, a timing-skew calibration detector and a clock generator. The four identical channels are driven respectively by four different clocks with equally-spaced phases, Φ_1 to Φ_4. Furthermore, the digitally controlled delay elements (DCDEs) can be independently adjusted by the digital control signal, $C_1[k]$ to $C_4[k]$, generated from a timing-skew calibration detector based on negative feedback. The ADC analog input is sequentially sampled and quantized by each channel to produce an 8-bit digital stream, and finally the digital streams from the four channels are multiplexed to generate the final ADC digital output.

III. PROPOSED TIMING-SKEW CALIBRATION

For a high-speed TIADC, it is imperative to minimize the mismatches among sampling instants. In Fig. 2, the moments of the falling edges of Φ_n (n = 1 to 4), which are sensitive to mismatches among clock drivers and routes, directly determine the sampling instants. In other words, the timing skews of the circuits are determined by the accuracy of the falling edges of Φ_n (n = 1 to 4).

A. Calibration Signal Generation

In order to calibrate timing-skew errors, several signals used in error estimation are generated by the master clock and the sampling phase Φ_n (n = 1 to 4). An example of calibration signal generation for Φ_1 is shown in Fig. 3. A master-slave D-Flip Flop is used to provide master output Φ_1 and slave output ψ_1. Therefore, Q_n (n = 1 to 4), utilized in following timing-skew estimation, can be expressed as

$$Q_n = M\_CK \cdot \phi_n \cdot \psi_n, (n = 1,2,3,4) \quad (1)$$

Fig. 4 shows the timing diagram of all calibration signals, Q_1 to Q_4. In Fig. 4(a), due to the differences of timing skews, the high levels of Q_n (n = 1 to 4) are not the same. Therefore, the timing skew of each channel can be estimated by measuring the high levels of Q_n (n = 1 to 4), and if all the high levels of Q_n (n = 1 to 4) are equal by the calibration, the timing skews are minimized, as seen in Fig.4(b).

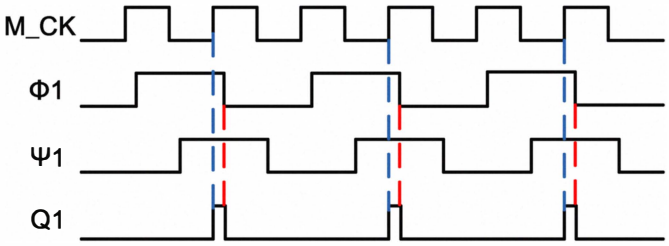
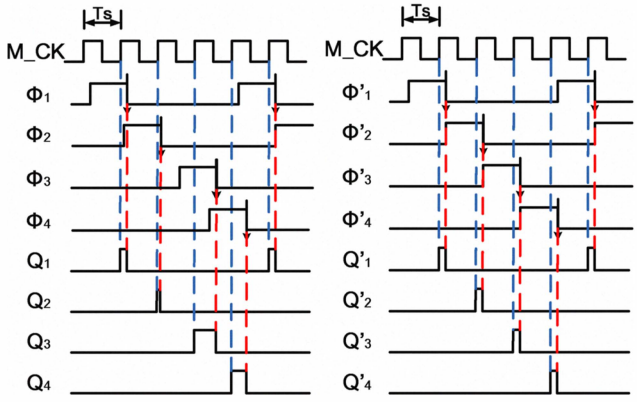


Fig. 3. Timing diagram of Q_1 generation



(a) (b)

Fig. 4. Timing diagram of calibration signals
(a) with timing skew (b) without timing skew

B. The Circuit of Timing-Skew Estimation

Referred to Fig. 4, to estimate the amount of timing skew, Q_1 is assumed as the reference signal, so the high levels of Q_n (n = 2 to 4) are to approach that of Q_1 in order to calibrate the timing skew errors. An example of Q_2 estimation is illustrated below, and the proposed circuit diagram is showed in Fig. 5(a).

Before the calibration is activated, the "reset" switch is closed and, thus, the voltage of the top plate of the sampling capacitor C_S resets to V_{cm}. At the same time, Q_1 to Q_4 are off. Then, as soon as "reset" turns off, Q_1 and Q_2 start working. As seen in Fig. 5(b), the capacitor C_S is charged by the current source I_1 when Q_1 is high, and discharged by the current source I_2 when Q_2 is high, respectively. Besides, when "latch" is high, the voltage of the top plate of Cs is determined by the distinction of the high level between Q_1 and Q_2 if I_1 equals to I_2, and the output of the comparator $P_1[k]$ can check whether the high level of Q_1 is longer than that of Q_2 or not. Thus, $P_1[k]$ is able to represent the timing skew of the second interleaved channel relating to the first one, and it realizes the timing-skew estimation. We can obtain $P_2[k]$ and $P_3[k]$ for the error detection of the third and fourth channels, similarly and respectively.

The digital output of the timing-skew estimation passes through a timing-skew calibration detector, and is then applied to the DCDEs to adjust the delay of the clock path.

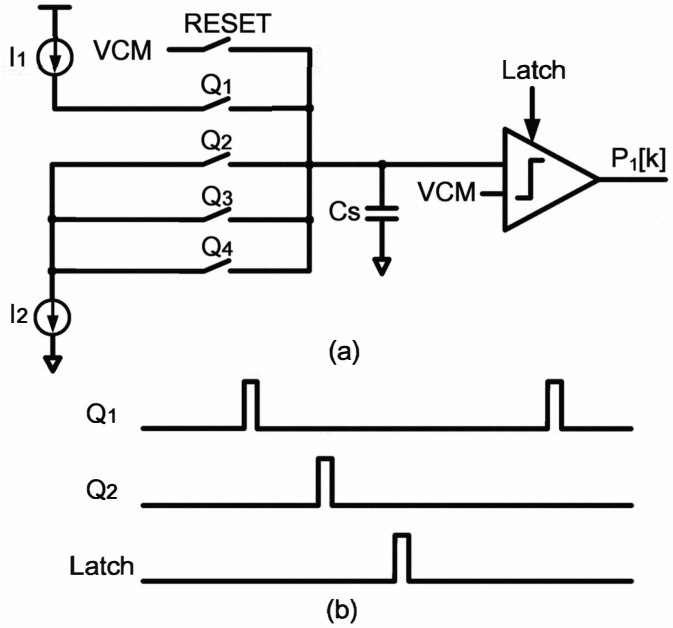


Fig. 5. Circuit and timing diagram of timing-skew estimation

(a)circuit diagram, (b)timing diagram

The calibration cycle repeats until the feedback drives the voltage of the top plate of C_S to V_{cm} (further explained in Section II-C). The $P_1[k]$ will alternate between 0 and 1s and the calibration is done for the first channel. Similarly, we can obtain $P_2[k]$ and $P_3[k]$ for the error detection of the third and fourth channels, respectively.

The adjusting precision and range of the DCDE is analyzed and calculated below. The effect of timing skews on the SNDR of a TIADC is given by [5-6]

$$SNDR = 20\log(\frac{1}{2\pi f_{in}\delta_\tau}) - 10\log(1-\frac{1}{M}) \quad (2)$$

where f_{in} is the frequency of the ADC input signal and M is the number of channels. If the timing-skew errors are treated as Gaussian random variables, δ_τ is the standard deviation. From (2), for instance, the timing skew of a four-channel 8-b 1.6 GS/s TIADC, must be less than 0.71 ps so that the ADC is able to attain 49-dB SNDR. As a result, the resolution of the DCDE is 0.7 ps, and according to the 50 times Monte-Carlo simulations, the range of timing-skew is not more than 10 ps based on 65 nm CMOS process. Therefore, a 4-bit DCDE is necessary.

In order to improve the range and accuracy of the timing-skew estimation with the calibration technique above, C_S and I (I equals to I_1 and I_2) must be determined after careful consideration to meet the reasonable compromise between the range and precision of the error detection. The relationship between C_S and I can be expressed as

$$C_S = \frac{Q}{V_{comp}} = \frac{I \cdot t_c}{V_{comp}} \quad (3)$$

where V_{comp} is the input range of the comparator in Fig.5(a) and t_c is the charging or discharging time of C_S.

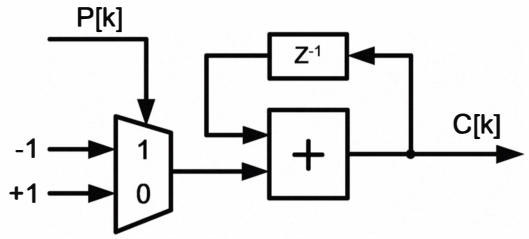


Fig. 6. The architecture of the timing-skew correction

Also, the changing range of V_{comp} is from 0 to 1 V, and t_c is the high levels of Q_n (n = 1 to 4). On one hand, for the range of the error estimation, it is necessary that

$$\begin{cases} V_{comp} = 1V \\ t_c \geq 10ps \end{cases} \quad (4)$$

On the other hand, since the DCDE is 5 bit, the precision of the comparator used in the error estimation is at least 4 bits. Hence, for the accuracy of the timing-skew detection, it is required that

$$\begin{cases} t_c = 0.7ps \\ \frac{1}{32}V \leq V_{comp} \leq \frac{1}{16}V \end{cases} \quad (5)$$

According to the eq. (3), (4), (5) and the requirement of low power consumption, C_S and I are 5 fF and 225 uA, respectively, which makes a balance between the adjusting range and precision of the timing-skew detection circuit.

C. Timing skew correction

Fig. 6 illustrates an example of the architecture implemented to compensate for timing skew of the second channel ADC. Also, the relationship between P[k] and C[k] can be given below,

$$C[k+1] = C[k] - 2P[k] + 1, (k \geq 0) \quad (6)$$

where P[k] is the digital output of the timing-skew estimation, and C[k], of which the initial condition C[0] is set to be the middle of the adjusting range (1000), is the input signal of DCDE to control the delay of the clock path. Consequently, the timing-skew calibration is done by creating the negative feedback between P[k] and C[k]. Similarly, the timing-skew correction of the third and fourth channels can be implemented by the architecture above.

IV. SIMULATION RESULT

The proposed calibration method has been verified by transistor-level simulation based on the 65 nm CMOS process. The following parameters are used in the simulation:

- 4 parallel 8-b ADCs.
- Sampling frequency f_s = 1.6GS/s.
- Sinusoidal input signal with frequencies between 1.6 MHz and 782.8 MHz.

Fig. 7 shows the simulated SNDR during the initial convergence of the timing-skew background-calibration algorithm, which improves the SNDR by 14 dB. Fig. 8 shows

the ADC's output FFT spectrum at 1.6 GS/s with 782.8 MHz sinusoidal input. After the calibration is activated, the SNDR is improved from 35.1 dB to 49.6 dB and the spurious-free dynamic range (SFDR) is improved from 38.4 dB to 69.8 dB. Fig. 9 illustrates the SNDR of the ADC versus input frequency. Without timing skew calibration, the performance degrades sharply as f_{in} rises. With the calibration, the SNDR remains relatively flat and the ADC performance is no longer limited by timing skew.

V. CONCLUSION

This paper proposes a background-calibration technique which can effectively eliminate the negative influence of timing skew and, therefore, significantly improve the performance of the ADC. Furthermore, compared with the majority of calibration algorithms in existence, the calibration method of this paper is more practical, due to the entirely implementation of the calibrating circuit and the independency of any additional calibration signal which occupies the dynamic range of the signal. Finally, simulations have been done on a four-channel TIADC to validate that the proposed technique works well.

ACKNOWLEDGMENT

This work was financially supported by Research Grants of University of Macau and Macao Science & Technology Development Fund (FDCT).

REFERENCES

[1] S. Limotyrakis, S. D. Kulchycki, D. K. Su, and B. A. Wooley, "A 150MS/s 8-b 71-mW CMOS time interleaved ADC," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1057-1067, May 2005.

[2] L. Sumanen, M. Waltari, and K. A. I. Halonen, "A 10-bit 200-MS/s CMOS parallel pipeline A/D converter," *IEEE J. Solid-State Circuits*, pp. 1048-1055, Jul. 2001.

[3] Huawen Jin, Edward K. F. Lee, "A Digital Background Calibration Technique for minimizing Timing-error Effects in Timing-interleaved ADCs", *IEEE Trans. on Circuits Syst. II, Analog and Digital Signal Processing*, vol. 47, no. 7, pp. 603-613, July 2000.

[4] Steven Huang and Bemard C. Levy, "Blind Calibration of Timing Offset and Gain mismatch for Four-channel Timing-Interleaved ADCs", *IEEE Trans. on Circuits Syst. I, Reg. Papers*, vol. 54, no. 4, pp. 863-876, Apr. 2007.

[5] Seng-Pan U, Sai-Weng Sin, and R. P. Martins, "Exact Spectra Analysis of Sampled Signals With Jitter-Induced Nonuniformly Holding Effects," *IEEE Trans. on Instrumentation and Measurement*, vol. 53, no. 4, pp. 1279-1288, Aug. 2004.

[6] N. Kurosawa, H. Kobayashi, K. Maruyama, K. Sugawara, and K. Kobayashi, "Explicit analysis of channel mismatch effects in time-interleaved ADC systems," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 38, no. 3, pp. 261-271, Mar. 2001.

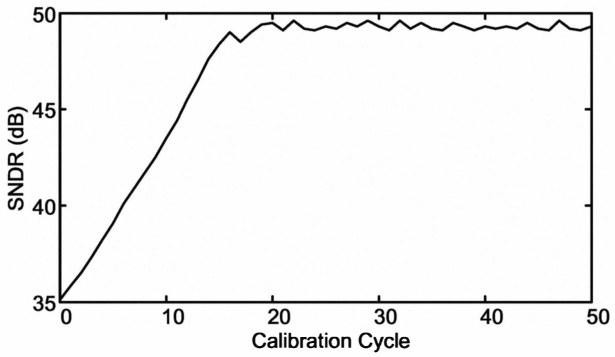


Fig. 7. The simulation result of SNDR during convergence of timing-skew calibration (fin = 782.8 MHz and fs = 1.6 GS/s).

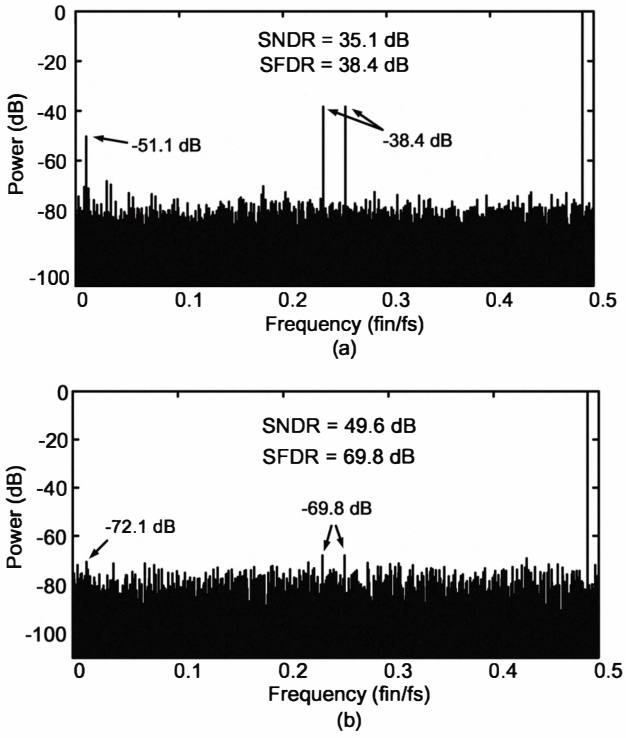


Fig. 8. ADC output spectrum (a) without calibration (b) with calibration (fin = 782.8 MHz and fs = 1.6 GS/s).

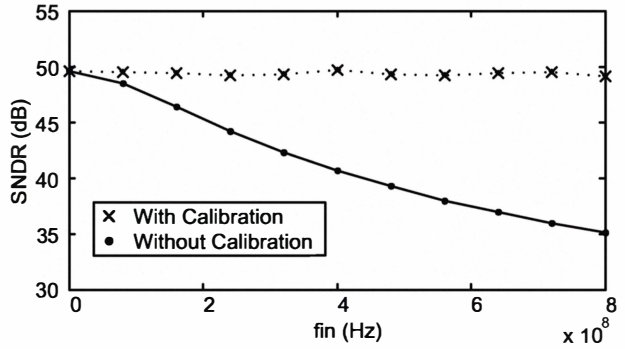


Fig. 9. SNDR versus input frequency at fs = 1.6 GS/s