A Frequency Up-Conversion and Two-Step Channel Selection Embedded CMOS D/A Interface

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***Abstract*—A multi-functional D/A interface for a novel two-step-up wireless transmitter architecture is described. A current-mode analog-double-quadrature sampling (A-DQS) technique is proposed in a two-channel 10-bit 120-MSample/s current steering D/A converters (DACs) to realize not only D/A conversion, but also baseband-to-IF image-reject upconversion, and IF channel selection for simplifying the radio front-end channel selection complexity. Realized with 0.35-μm CMOS in *Cadence*^{TM}, the active die area is 2.55 mm^2. The integral (INL) and differential (DNL) nonlinearities are better than ±0.42 LSB and ±0.38 LSB, respectively. The spurious-free dynamic range (SFDR) is > 56 dB. The power dissipation is 163 mW from 2.5-V analog/1.8-V digital supplies.**

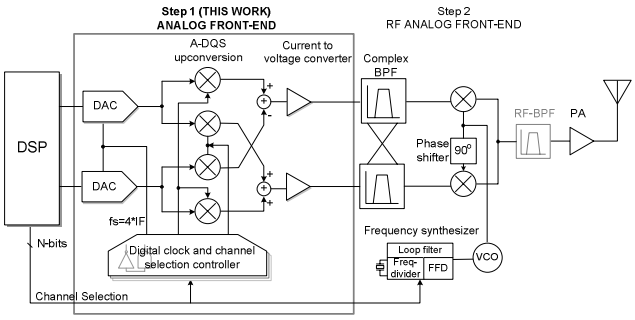


Fig. 1. Proposed two-step-up wireless transmitter.

1. INTRODUCTION

The trend of wireless communications will unite the wireless personal-area networks (WPANs), local-area networks (WLANs) and wide-area networks (WWANs), thereby, multi-standard wireless transceiver integrated circuits (ICs) will be in increasing demand for future support of all wireless environments with low-power and low-cost CMOS implementations within decades. Unfortunately, the traditional commercial transceiver topologies still require some power-hungry off-chip components [1],[2], and they are no longer feasible and contradict to the state-of-the-art scope of System-On-a-Chip (SoC).

A two-step channel-selection technique, which was originally employed in low-IF/zero-IF wireless receiver, can be migrated to the transmitter counterpart [3], as shown in Fig. 1. Such technique not only reduces the PLL frequency synthesizer (PLL-FS) settling-time and phase-noise requirements, but also simplifies the anatomy of the frequency divider. This paper will focus on the transmitter analog front-end (AFE) design and implementation, which has distinguishable different from its receiver counterpart. The targeted applications will cover Bluetooth, WCDMA and IEEE 802.11a.

After the introduction, the proposed transmitter architecture and its baseband circuit implementation are addressed in Section 2 and Section 3, respectively. In Section 4, the post-layout simulation results of the D/A interface are provided. Finally, the conclusion is summarized in Section 5.

2. TRANSMITTER ARCHITECTURE

The proposed transmitter, shown in Fig.1, implements a novel two-step frequency up-conversion, where the baseband-to-IF up-conversion has been embedded between the current steering D/A core and the current-to-voltage converter. The efficiency of the architecture relies on the A-DQS technique presented schematically in Fig. 2 [3]. After the DAC, the output signal would be in current mode, and sampling the *I* and *Q* channels with sampling frequency equal to 4 times the IF will be equivalent to an integer-weighted double-quadrature mixing, implying an I/Q mismatch insensitive. Moreover, only clock phases and simple digital circuitry are necessary for the mixing and mode control, there is no IF local oscillator and frequency synthesizer are required. After that, the complex up-converted signal will pass through a pair of complex bandpass filter (C-BPF), which not only serves as a smoothing filter, but also rejects the image signal when there

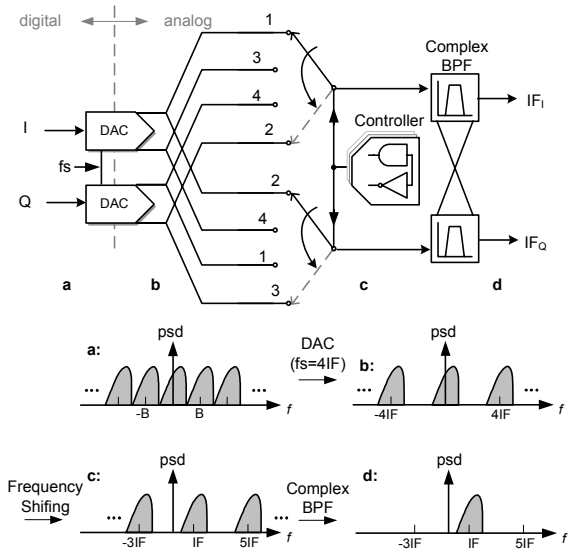


Fig. 2. Detailed D/A interface.

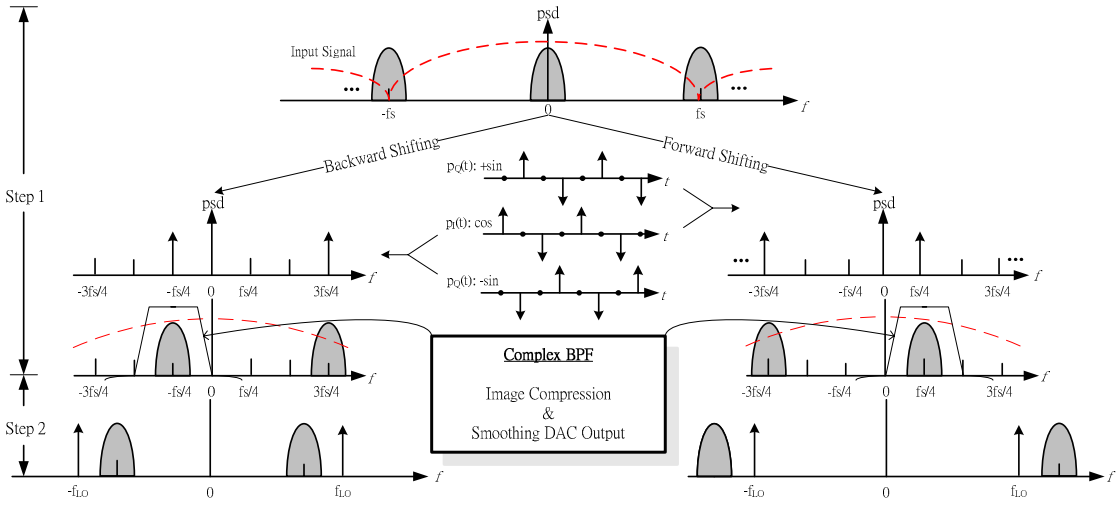


Fig. 3. Spectra flows of two-step channel selection in the proposed transmitter architecture.

is *I/Q* mismatch. Since the operating frequency of the D/A core is 120-MHz, the filter requirements are not fairly stringent. Furthermore, the offset cancellation can easily be adopted in the filter in order to allow individual biasing and to eliminate any offset wandering effects, since the signal would be now at the IF. On the other hand, in the RF analog front-end [Fig.1], the complex IF signal can be up-converted to real radio frequency (RF) by conventional quadrature mixers. Finally, depending on the required quality of the output spectrum, the RF bandpass filter (RF-BPF) might not be necessary.

2.1 Current-mode A-DQS for frequency up-conversion and IF channel selection

A charge-mode switched-capacitor (SC) down-converter for a reconfigurable receiver has been recently presented [3] that includes four mixers operating in complex-to-complex frequency conversion namely analog-double quadrature sampling, A-DQS. Here, the concept would be extended to the transmitter path but adopting in current-mode operation to take the inherent advantage of the current-steering DAC (with the consequent circuit minimization), and before the succeeding current-to-voltage converter that would be required for the voltage operation of the following transmitter stages. Moreover, by changing the sampling sequence for IF channel selection [4], the forward shifting (FS) or backward shifting (BS) is easily achieved, as shown in Fig. 3, where the orthogonal samplers $p_I(t)$ and $p_Q(t)$ are expressed as:

$$p_I(t) = \sum_{n=-\infty}^{\infty}\left[\delta(t-nT_s) - \delta(t-nT_s - T/2)\right]$$
$$p_Q(t) = \sum_{n=-\infty}^{\infty}\left[\pm\delta(t-nT_s - T/4) \mp \delta(t-nT_s + T/4)\right] \quad (1)$$

with a sampling frequency f_s = 4·IF. For FS, it will be necessary to consider Eq. 1 with the upper sign, whereas for BS, the lower sign must be considered. Then, the complex signal can be shifted to one side of the center frequency by adjusting the digital controller switching sequence. Therefore, the channel selection can be separated into two steps: the first comprising a baseband-to-IF up-conversion, with one center frequency carrying the baseband signal into two different IF channels by using the shifting property; and the second including a complex-to-real signal up-conversion, where the PLL-FS transports the IF signal to RF, resulting in a relaxation of the carrier frequency by 50%.

2.2 Current steering D/A interface

The D/A interface, shown in Fig. 4, has been designed for different standards, ranging from 1-MHz to 20-MHz channel spacing. Two different center frequencies are generated as 0.5× and 1.5× of the maximum signal bandwidth, i.e., 10 MHz and 30 MHz, respectively. Therefore, the upper limit of the D/A interface output frequency would be 40 MHz.

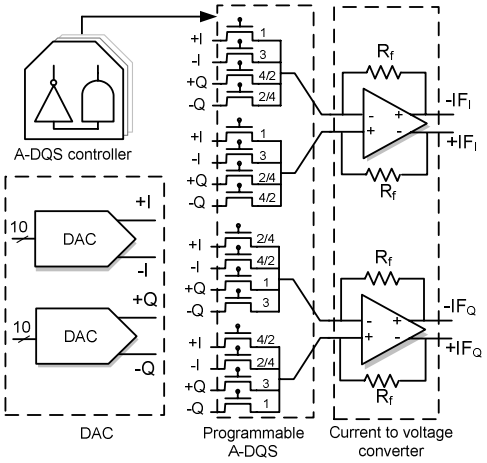


Fig. 4. General circuit architecture of the D/A interface.

A 10-bit DAC is utilized to achieve around -60-dBc adjacent channel power (ACP) rejection. Since the required sampling rate imposed by the A-DQS technique is 4×up-conversion center frequency, thereby, a 120-MSample/s oversampling DAC (OSDAC) has been designed, that also can simplify the requirements of the following complex bandpass filter.

3. CIRCUIT IMPLEMENTATION

3.1 Current-steering D/A core

The current steering DAC structure presents evident cost and power consumption advantages when shouldering high speed and high-resolution operation, being intrinsically faster and more linear than other type of architectures. Fig. 5 shows the floor plan of the designed segmented DAC that includes a 4-bit binary and 6-bit unary sub-DAC, using an area-efficiency method to achieve better DNL performance [5].

In the current cell, the output impedance will directly affect the linearity performance, but the cascade configuration of the switch and current source implies a sufficiently high impedance to achieve the INL and SFDR specifications. For the current design, the dimensions of the unit current source transistor are, a 10.35-µm gate-width and a 92.8-µm gate-length, for a 99.7% yield specification.

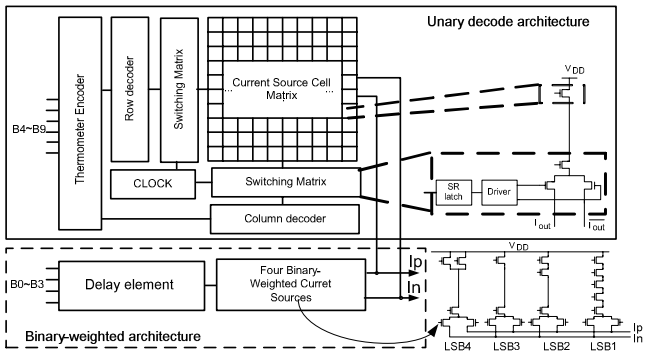
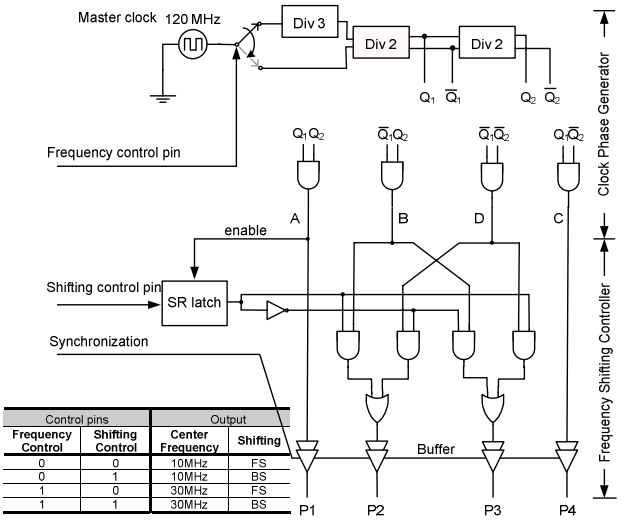


Fig. 5. Floor plan of the 10-bit segmented current steering DAC.

3.2 A-DQS controller

Regarding the A-DQS controller it is composed by two main parts: the clock phase generator and the frequency-shifting controller, as shown in Fig. 6. The master clock at 120 MHz will control the generation by the frequency divider of the clock signal, either at 10 MHz or 30 MHz, through the frequency control pin input. This clock signal will be generated by digital logic and it will comprise 4-clock phases, A, B, C and D, each with a pulse width of 1/4 but with the same frequency.

The frequency-shifting controller imposes the phase sequence arrangement of A, B, C and D through logical operation and commanded by the conversion shifting. Obviously, the channel selection cannot be triggered inside the sampling sequence time-frame thus the channel selection



Control pins		Output	
Frequency Control	Shifting Control	Center Frequency	Shifting
0	0	10MHz	FS
0	1	10MHz	BS
1	0	30MHz	FS
1	1	30MHz	BS

Fig. 6. Circuit diagram of the A-DQS controller.

must be enabled at the beginning of phase A. Finally, the driving signals P1, P2, P3 and P4 are synchronized by the operation of the buffers.

3.3 Current-to-voltage converter (output buffer)

The current-to-voltage converter, following the A-DQS up-conversion, has also embedded an output buffer for driving the following stages. Since, the input node of the converter is the virtual ground of the opamp, the fluctuation of the DAC output is comprised inside a small variation margin leading to higher stability in current generation. However, the main challenge lies on the high-gain and high-bandwidth fully-differential opamp, that was designed adopting a two-stage telescopic amplifier architecture with gain and bandwidth boosting in the first stage [6]. Proper wide-swing has been employed also to bias with equal I/O common mode levels at 1 V (with 2.5-V supply), and being stabilized by improved continuous-time common-mode feedback (CMFB).

3.4 Layouts

The D/A interface layout was implemented with *Cadence Virtuoso* in a 0.35-µm CMOS technology (with 3M2P), as shown in Fig. 7. The substrate noise coupling and dI/dt noise were reduced through the use of careful floor planning, guard-rings and shielding in sensitive places. A symmetric distribution was also applied especially for the current-source matrix (designed highly compacted for gradient error reduction), which has been separated into 4 units placed in a double common-centroid geometry [7]. Also, in the case of the INL bounded switching sequence it was implemented in the DAC row column decoding. Moreover, large arrays of matching objects exhibiting proximity errors next to the gradient errors are also inserted as dummy current sources at the matrix edges for optimal matching, thus, allowing the current source units, within a certain radius around, to observe the same electrical surrounding environment.

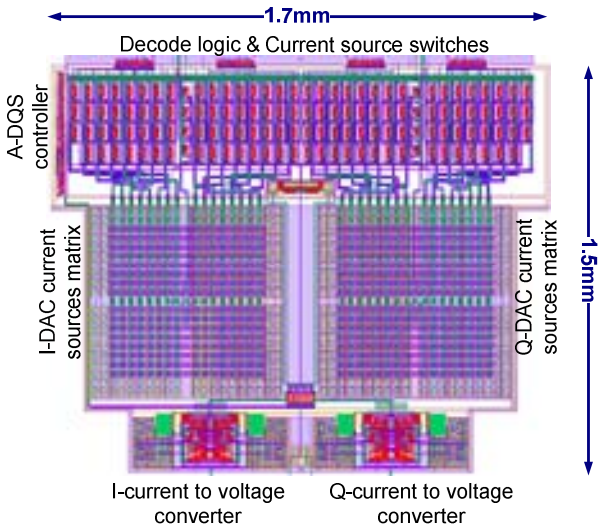


Fig. 7. D/A interface layout.

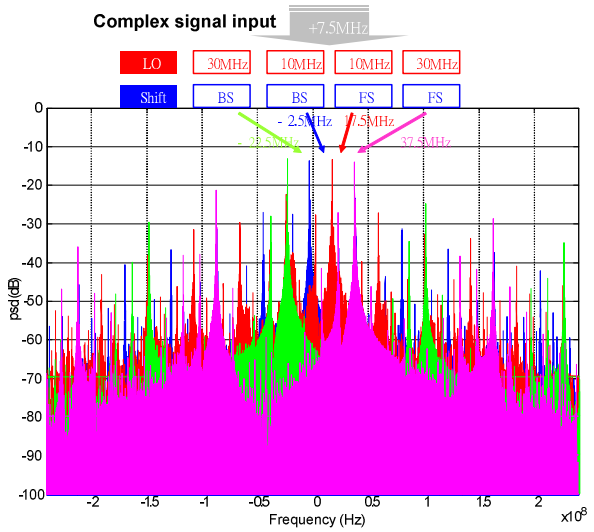


Fig.8. Post-layout functional simulation in the frequency domain.

4 Simulation Results

To evaluate the overall performance of the D/A interface, in the time and frequency domain, a functional post-layout simulation was developed with the main results presented in Table 1. The most important transmitter performance issue is its spectral purity. Under a 120-MHz sampling frequency the SFDR will be close to 56 dB at 1 MHz. Since the proposed D/A interface is designed for multistandard applications it was focused on a maximum signal bandwidth of 20 MHz and to test its functionality a complex input signal within that range was injected. The tested signal is then up-converted to 4 different frequency channels, for different oscillation frequencies with the shifting scheme controlled by an A-DQS technique. A simulation results obtained in the frequency domain with a complex test input signal at 7.5 MHz is illustrated by Fig. 8.

Table 1. Performance summary.

D/A Interface Post-Layout Simulated Performances	
Power consumption	163 mW
|INL|	≤ 0.43 LSB
|DNL|	≤ 0.36 LSB
Propagation delay (rise)	4.54 ns
Propagation delay (fall)	3.52 ns
Settling time (rise)	12.45 ns
Settling time (fall)	14.50 ns
Rise time	8.6 ns
Fall time	9.3 ns
SFDR @ 1MHz	56.34 dB

5 Conclusions

A multistandard-compliant two-step-up transmitter D/A interface was introduced. In addition to the DAC and output buffers, a highly effective two-step channel-selection technique was embedded to perform baseband-to-IF upconversion as well as IF channel selection, thus simplifying the frequency synthesizer settling time and phase noise requirements. Those functionalities consume a total of 163 mW and occupy an active silicon area of 2.55 mm^2. The combination of this design with the receiver presented in [8] forms the basis for the future implementation of the entire transceiver.

Acknowledgment

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