# NTF Zero Compensation Technique For Passive Sigma-Delta Modulator

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***Abstract*— A novel technique is proposed to compensate zeroes of Noise Transfer Function (NTF) for single loop low pass passive switched capacitor sigma-delta modulator (PSDM). PSDM uses switched capacitor (SC) integrator as a loop filter. Poles of loop filter are zeroes of NTF. The proposed technique for SC integrator shifts the poles of SC integrator from inside the unit circle to z=1 at DC. As a result zeroes of NTF for PSDM also get modified and shifts, which greatly improves the noise suppression and noise-shaping performance. Simulation results in simulink, shows that the technique of proposed SC integrator for 2nd Order PSDM with 4-bit quantizer having oversampling ratio (OSR) = 32 improves 18dB SNDR over traditional SC integrator.**

## I. INTRODUCTION

Sigma-Delta modulator can attain medium to high resolution by noise-shaping and oversampling. Sigma-Delta circuitry can be implemented by DT (discrete-time) or CT (continuous-time). Discrete-time circuit implementation uses SC network with operational amplifier while CT (continuous-time) circuit is implemented by R and C network with operational amplifier for higher speed. Passive Sigma-Delta Modulator [1-3] is the promising area of low power and high dynamic range. Its loop filter can be defined as analog switches and capacitors only. Comparator is the only active component in the PSDM, so operational amplifier can be avoided. The SC integrator implementation is very simple and consumes no power as compared to operational amplifier. Switched capacitor integrator has charge leakage phenomena, which causes only a portion of charge from input capacitor is transfer to integrating capacitor. This results in NTF zero of PSDM to move inside the unit circle at DC in z-domain. It degrades the noise attenuation in signal band and destroys the noise-shaping property of sigma-delta modulator.

In this paper, NTF zeroes compensation technique is presented which can significantly improves the noise shaping of low-pass PSDM and results in higher SNDR. A 2nd order PSDM is simulated in the simulink to verify the NTF zeroes compensation technique. The organization of the paper is as follows. In section II basic understanding of real integrator and traditional switched capacitor integrator are presented. Section III presents, the proposed switched capacitor integrator. Section IV provides the modeling and simulation results and the section V conclude the paper.

## II. REVIEW OF INTEGRATOR MODEL

### A. Real Integrator Model

The commonly used delaying active integrator has transfer function H(z) as equation(1).

$$H(z) = \frac{z^{-1}}{1-z^{-1}} \qquad (1)$$

It has zero at origin and pole z=1 at DC of the unit circle in z-domain as shown in Figure 1.

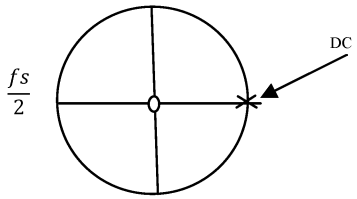


Figure 1. Pole-zero constellation plot for real integrator

### B. Passive Switched Capacitor Integrator (Leaky Inegrator)

Switched capacitor integrator with non-overlapping clock can be realized by analog switches and capacitor only as shown in Figure 2.

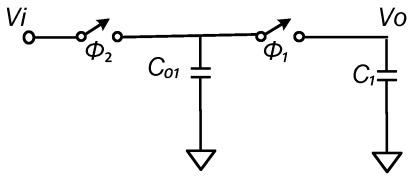


Figure 2. Switched Capacitor Integrator

The transfer function [4] of the switched capacitor integrator is

$$H(z) = \frac{\alpha z^{-1}}{[1-(1-\alpha)z^{-1}]} \qquad (2)$$

Where α defines the ratio of capacitor as

$$\alpha = \frac{C_{01}}{C_1+C_{01}} \qquad (3)$$

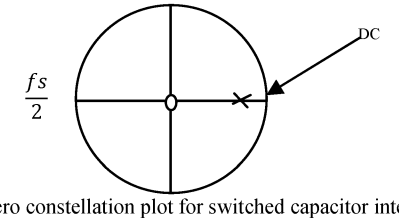


Figure 3. Pole-zero constellation plot for switched capacitor integrator

So this ratio of capacitors defines the pole position on unit circle and gain for the switched capacitor integrator. For stability, the pole position now still at DC but is shifted inside the unit circle as shown in Figure 3.

## III. Proposed Switched Capacitor Integrator

We propose a new SC integrator which removes the effect of leakage from the SC integrator as shown in Figure 4. So the transfer function of SC integrator behaves like a real integrator. The main leakage term in the denominator cancels and so it is a real integrator.

A model of delaying switched capacitor integrator is presented to prove the concept.

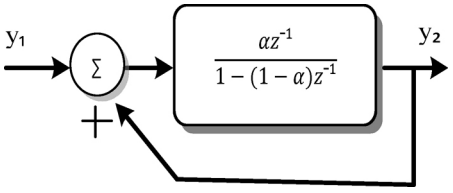


Figure 4. Proposed delaying switched capacitor integrator

Here is the mathematical prove of the proposed switched capacitor integrator

$$y_2 = (y_1 + y_2)\frac{\alpha z^{-1}}{[1-(1-\alpha)z^{-1}]} \qquad (4)$$

$$y_2\left[1 - \frac{\alpha z^{-1}}{[1-(1-\alpha)z^{-1}]}\right] = \frac{\alpha z^{-1}}{[1-(1-\alpha)z^{-1}]} y_1 \qquad (5)$$

$$y_2\left[\frac{1-z^{-1}+\alpha z^{-1}-\alpha z^{-1}}{[1-(1-\alpha)z^{-1}]}\right] = \frac{\alpha z^{-1}}{[1-(1-\alpha)z^{-1}]} y_1 \qquad (6)$$

$$y_2[1-z^{-1}] = \alpha z^{-1} y_1 \qquad (7)$$

$$y_2 = \frac{\alpha z^{-1}}{1-z^{-1}} y_1 \qquad (8)$$

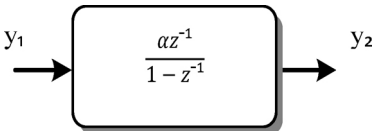


Figure 5. Proposed delaying switched capacitor integrator model

So the equation (8) proves that it become a real delaying integrator with numerator co-efficient as shown in Figure 5. The pole of the switched capacitor integrator is shifted from inside the unit circle to z=1at DC.

Now considering non-delaying switched capacitor integrator, a delay is compensated in the feedback path so it needs at least one delay in the feedback as shown in Figure 6. So proposed model will be

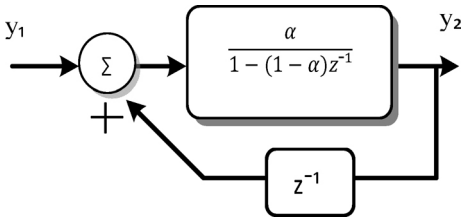


Figure 6. Proposed non-delaying switched capacitor integrator

This will result into non-delaying integrator and forward co-efficient in numerator as normal SC integrator.

$$y_2 = (y_1+y_2 z^{-1})\frac{\alpha}{[1-(1-\alpha)z^{-1}]} \qquad (9)$$

$$y_2\left[1 - \frac{\alpha z^{-1}}{[1-(1-\alpha)z^{-1}]}\right] = \frac{\alpha}{[1-(1-\alpha)z^{-1}]} y_1 \qquad (10)$$

$$y_2\left[\frac{1-z^{-1}+\alpha z^{-1}-\alpha z^{-1}}{[1-(1-\alpha)z^{-1}]}\right] = \frac{\alpha}{[1-(1-\alpha)z^{-1}]} y_1 \qquad (11)$$

$$y_2[1-z^{-1}] = \alpha y_1 \qquad (12)$$

$$y_2 = \frac{\alpha}{1-z^{-1}} y_1 \qquad (13)$$

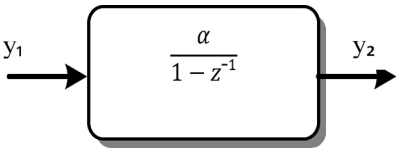


Figure 7. Proposed non-delaying switched capacitor integrator model

The equation (13) proves that assuming a delay $z^{-1}$ in the feedback path, even this also verifies that pole of the integrator does not lies inside the unit circle at DC in z-plane. This means that the leaky term $\alpha z^{-1}$ of SC integrator automatically canceled, and a real integrator operation returns with numerator co-efficient. The Figure 7 shows a block of proposed non-delaying SC integrator.

## IV. Modeling and Simulation Results

In this section, a design example of 2nd order PSDM is modeled for traditional SC integrator and proposed SC integrator. Matlab modeling and simulation results are presented.

### *A. DESIGN EXAMPLE*

As proof of the concept, 2nd Order PSDM model is presented and simulated in simulink for traditional SC integrator and proposed SC integrator.

First a 2nd Order PSDM with traditional SC integrator model is presented in Figure 8. The signal swing in front of quantizer is very small so large gain G is required and quantizer is the only active component. The poles of loop filter are zeroes of the NTF [5]. Traditional SC integrators causes zeroes of NTF to moves inside the unit circle at DC, which effects proper noise attenuation in signal band and degrade the noise-shaping of PSDM.

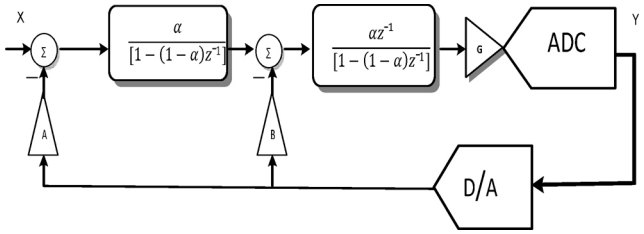


Figure 8. 2nd Order PSDM with traditional switched capacitor integrator model

The NTF(z) of Figure 8 for 2nd order PSDM is given by

$$NTF(z) = \frac{[1-(1-\alpha)z^{-1}]^2}{D(z)} \qquad (14)$$

$$D(z)=[1-(1-\alpha)z^{-1}]^2+AG\alpha^2 z^{-1}+BG\alpha z^{-1}[1-(1-\alpha)z^{-1}]$$

Where A & B are the feedback co-efficient, G is the gain and $\alpha$ =0.2 defines the ratio of capacitors for SC integrator in the loop filter.

Now the proposed SC integrator with 2nd Order PSDM model is simulated as shown in Figure 9.

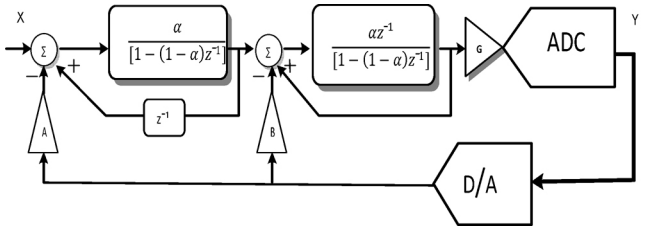


Figure 9. 2nd Order PSDM model with proposed integrator model

The NTF(z) of the proposed integrator model is

$$NTF(z) = \frac{[1-z^{-1}]^2}{D(z)} \qquad (15)$$

$$D(z)=[1-z^{-1}]^2+AG\alpha^2 z^{-1}+BG\alpha z^{-1}[1-z^{-1}]$$

Equation (14) & (15) describes NTF(z) of traditional and proposed SC integrator. From equation (15), the NTF(z) zeroes shift to z=1 at DC for proposed SC integrator, which eliminates noise from signal band and improves the SNDR as compared to the traditional SC integrator. A comprehensive system level performance analysis for 2nd Order PSDM considering both types of SC integrators is performed as shown in Figure 10 and Figure 11. OSR versus SNDR for different no of quantizer bits for both types of SC integrators models are simulated. The OSR ranges from 5 to 150, while no of quantizer bit from 2 bit to 8-bit and SNDR is compared for both type of integrator models. As an example for a 4-bit quantizer traditional SC integrator having OSR=32 results in SNDR=67dB while proposed SC integrator model with same no of quantizer bit and OSR results in SNDR=85dB. Its output spectrum for traditional and proposed SC integrators with input signal Vi = 0.94v is shown in Figure 12.

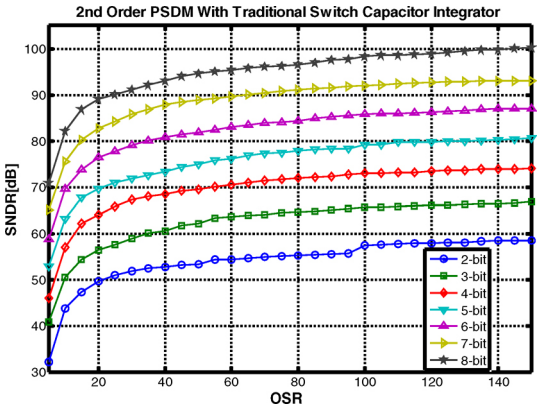


Figure 10. 2nd Order PSDM for traditional switched capacitor integrator

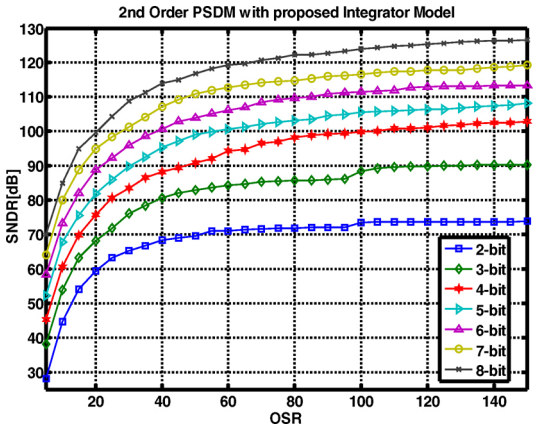


Figure 11. 2nd Order PSDM for proposed switched capacitor integrator

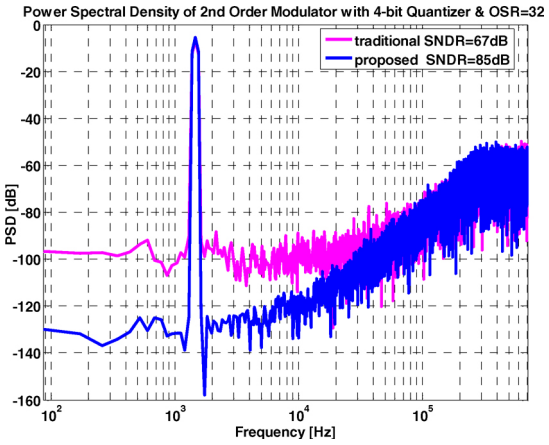


Figure 12. Matlab Simulated PSD for both integrator models

Dynamic range comparison of 2nd Order PSDM having OSR=32 with 4-bit quantizer for both types of SC integrators is plotted in Figure 13. Proposed SC integrator clearly has more than 20dB higher dynamic range as compared to traditional SC integrator. Simulation results of 2nd Order PSDM for different no of quantizer bits for different OSR are summarized in Table I.

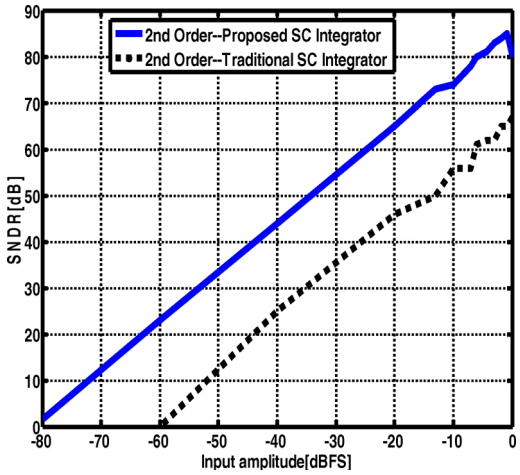


Figure 13. Dynamic range comparison for 2nd Order PSDM with 4-bit quantizer & OSR=32

TABLE 1: 2nd Order PSDM Results for proposed integrator

| *Specification* | *Value* | | | | |
|---|---|---|---|---|---|
| Peak SNDR | 85dB | 89dB | 95dB | 80dB | 94dB |
| SNDR improvement | 18dB | 20dB | 22dB | 20dB | 24dB |
| OSR | 32 | 40 | 40 | 40 | 60 |
| Quantizer | 4-bit | 4-bit | 5-bit | 3-bit | 4-bit |

### *B. INTEGRATOR WITH INCOMPELETE CHARGE TRANSFER*

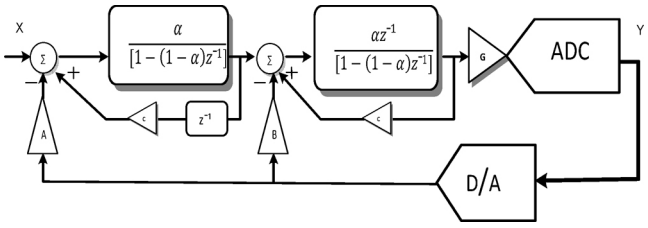


Figure 14. PSDM Model with non-ideal effects for 4-bit quantizer & OSR=32

The proposed integrator model for 2nd order PSDM having non-ideal effect, incomplete charge transfer effect C in the feedback path is modeled in Figure 14. The parameter C can be used to estimate the charge lost during the feedback path from output to the input of switched capacitor integrator. Performance degradation due to charge loss property is shown in Figure 15.

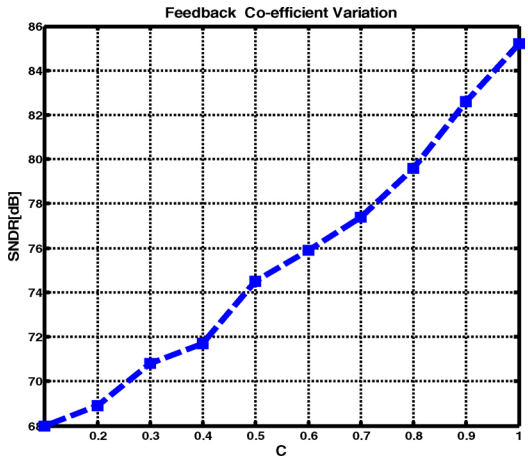


Figure 15. Feedback parameter C versus SNDR [dB]

## V. CONCLUSION

A novel technique for passive switched capacitor integrator is proposed in this paper, which significantly improves the noise-shaping performance of PSDM. Moreover, it can remove the charge leakage phenomena proved mathematically and also simulink simulation is performed to verify this technique. Finally a design example of 2nd Order PSDM with 4-bit quantizer for OSR=32 is simulated and performance is compared between the traditional switched capacitor integrator and proposed switched capacitor integrator. The proposed model of switched capacitor integrator for 2nd order PSDM with 4-bit quantizer having OSR=32 achieves 18dB higher SNDR as compared to its traditional switched capacitor integrator.


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