A Novel Half-Band SC Architecture for Efficient Analog Impulse Sampled Interpolation

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ABSTRACT

Half-band filtering technique is an efficient approach especially for 2-fold sampling rate alterations. This paper proposes novel Switched-Capacitor (SC) architectures for sampled-data analog half-band impulse sampled interpolations whose system responses are also immune to the input sample-and-hold filtering effect distortion. Three alternative architectures are investigated with their corresponding comparative superiority from the view-points of required number of amplifiers and passive SC branches as well as clock phases. An effective multistage implementation of SC interpolation based on the newly proposed half-band interpolators is also described with further comparison among traditional designs.

1. INTRODUCTION

By the continuous developments of the design of high performance analog signal conditioning interfaces, together with the rapidly growing evolution of multirate mixed-mode signal processing systems [1], the investigation of precise and efficient-architecture sampling rate alteration systems has increasingly become the research area in demand [2-9]. A new efficient impulse sampled analog interpolation design [10-13] based on either Direct-Form (DF) or Active-Delayed Block (ADB) polyphase structures for lower and higher-order FIR or even IIR system function has been recently proposed with the inherent elimination of the undesired input sample-and-hold (S/H) filtering effect distortions that occurred in previously available designs [3,5,7]. The sampling rate converters with a small alteration ratio, especially of *2*, are practically indispensable not only in some specific applications but also in multistage implementations by cascading with integer or even rational impulse sampled sampling rate converters [13-14] to achieve the systems with a large conversion ratio, or a prime number alteration ratio but nevertheless stringent specifications, respectively, thus leading to an efficient and practical design with respect to the analog circuitry. Nevertheless, the efficiency with regard to the power and silicon consumption of SC implementation by employing currently available structures will be reduced with the decrease of the sampling rate alteration ratio, especially at a minimum of *2*. This paper proposes novel SC non-recursive architectures based on ADB polyphase structures for impulse sampled 2-fold interpolation with efficiently employing the half-band filtering technique, which is specifically adequate and effective for increasing or decreasing the sampling rate by a factor of *2* due to its advantageous property that approximately half of the filter coefficients are exactly zero [15-16]. A multistage design based on SC half-band interpolators will be further discussed for illustrating its superiority when compared with the single stage and even the traditional multistage designs.

2. ENHANCED SC HALF-BAND ARCHITECTURE FOR ADB POLYPHASE STRUCTURE

For the smallest alteration ratio $L=2$, the interpolation filter length is normally much greater than $2L$; hence, the canonic ADB polyphase structures [11] become more practical when compared with DF polyphase structures [3,10] for real SC realization that will decompose non-recursive transfer function into $B+1$ blocks according to

$$H(z)=\sum_{n=0}^{N-1}h_n z^{-n}=\sum_{b=0}^{B}\left(\sum_{n=0}^{L-1}h_{n+bL}z^{-n}\right)\cdot(z^{-L})^b \qquad (1a)$$

$$B=\left\lfloor\frac{N-L}{L}\right\rfloor \qquad (1b)$$

where $\lfloor x \rfloor$ denotes the smallest integer equal to or greater than x, and each block, which contains only L coefficients, is realized by using DF polyphase structures with sharing of the common ADB serial delay line – $(z^{-L})^b$. However, it is obvious that when L reduces to 2, it requires a large number of ADB's or OA's (1 OA per ADB), thus resulting high power dissipation and relatively reduced accuracy. The enhancement in order to reduce the value of B, which denotes the demanded number of ADB, can be the increase of the coefficients in each block or the delay of the common ADB's.

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I. With Double-Delay ADB's for N>7L : Doubling the delay of ADB's from original canonic z^{-L} to z^{-2L} simultaneously leads to an increase of coefficients in each block from L to $2L$, so that the overall transfer function of $L=2$ can be expressed as

$$H(z)=\sum_{b=0}^{B}\left(\sum_{n=0}^{2L-1}h_{n+2bL}z^{-n}\right)\cdot(z^{-2L})^{b}=(h_0+h_1z^{-1}+h_2z^{-2}+h_3z^{-3})+(h_4+h_5z^{-1}+h_6z^{-2}+h_7z^{-3})\cdot z^{-4}+\cdots \quad (2a)$$

$$B=\left\lfloor\frac{N-2L}{2L}\right\rfloor=\left\lfloor\frac{N-4}{4}\right\rfloor \quad (2b)$$

Therefore, from (1) and (2), the number of ADB is reduced. However, such architecture requires complex and inefficient implementation of DF polyphase SC branches with delay terms of z^{-2} and z^{-3} in each block [3, 10]. Only when the half-band filtering technique is employed, such structure becomes especially practical and efficient, since the impulse response coefficients with odd number indices (h_1, h_3, ...) in half-band filters are zero except the center coefficient h_M (with odd M and odd total filter length $2M+1$) [15-16]. Thus, the longest delays terms z^{-3} in each polyphase filter are usually omitted. The non-recursive transfer function of half-band filter can be expressed as

$$H(z)=h_Mz^{-M}+\sum_{n=0}^{M}h_{2n}\cdot z^{-2n}=h_Mz^{-M}+\sum_{n=0}^{(M-1)/2}h_{2n}\cdot\left(z^{-2n}+z^{-2(M-n)}\right) \quad (3)$$

where M is an odd number and impulse response h_n (odd length of $2M+1$) satisfies the condition of

$$h_n=\begin{cases}1, & n=M\\ 0, & n=1,\ 3,\ 5,\ \cdots,\ 2M-1\ (except\ M)\end{cases} \quad (4)$$

Thus, the enhanced ADB polyphase structure with double-delay for half-band interpolation can be derived as

$$H(z)=\left(h_Mz^{-(M-2LD)}\right)\cdot(z^{-2L})^{D}+\sum_{b=0}^{B}\left(\sum_{n=0}^{L}h_{2n+2bL}z^{-n}\right)\cdot(z^{-2L})^{b} \quad (5)$$

where D is the integer part of $B/2$. For simplicity, we consider a design example of a 2-fold FIR half-band interpolator with 27-duration impulse response coefficients in which 12 coefficients are zero. The corresponding double-delay ADB polyphase structure is illustrated in Fig.1(a). As we can see, the part with gray lines indicates that all coefficients of polyphase filter $m=1$ equal to zero except the center coefficient h_M, thus making such enhanced structure practical by means of the efficient reduction of the number of SC branches and total capacitance occupation.

In real SC realization, in order to provide the ADB with extension of its delay from z^{-2} to z^{-4}, the period ($1/f_s$ = $1/1MHz$) of original 2 clock phases 0 and 1 must be doubled to ($2/f_s$ = $1/500KHz$). Thus, additional 2 complementary clock phases 0' and 1' are necessary to guarantee that the interpolator can produce 4 outputs during $2/f_s$. The corresponding SC circuit is implemented with these 4 respective clock phases shown in Fig.2. To ensure that each ADB produces the inputs with delay z^{-4} and also in every input sampling reference period, two same input SC branches which are separately controlled by the complementary clock phases are employed in each SC ADB's. The first ADB uses doubled input PCTSC

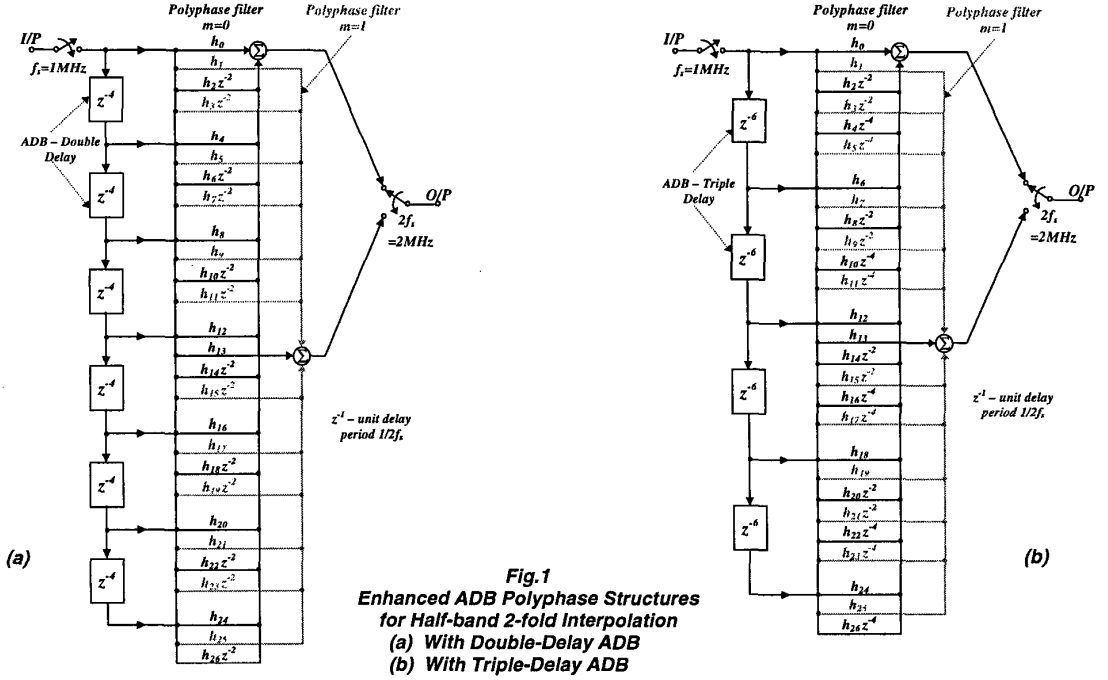


Fig.1
Enhanced ADB Polyphase Structures for Half-band 2-fold Interpolation
(a) With Double-Delay ADB
(b) With Triple-Delay ADB

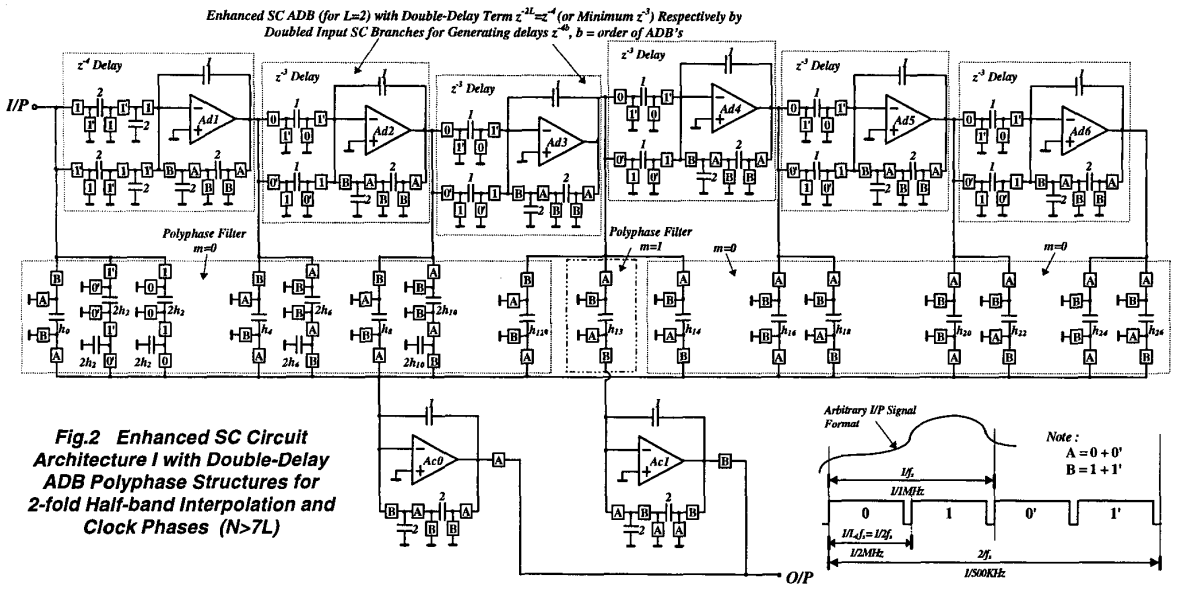


Fig.2 Enhanced SC Circuit Architecture I with Double-Delay ADB Polyphase Structures for 2-fold Half-band Interpolation and Clock Phases (N>7L)

branches for complete delay z^{-4}, while the rest *5* SC ADB's with doubled input TSI branches are used for delaying the signal by z^{-3}. Nevertheless, when taking into account the delay between the output of previous ADB and input sampling of the next ADB, this serial delay line will generate the delays separately with z^{-4b} where b (=*0, 1, ... , B*) is the order of ADB's. All $h_{2+4b}z^{-2}$ delay terms can be realized by taking into account the delays provided by the output sampling of accumulator except in block *1*, and in there, doubled SC branches are employed for term h_2z^{-2} for the purpose of allowing arbitrary input signal formats. The last *3* negative coefficients are realized by OFR branches with their required delays. It can be concluded that this enhanced structure is especially suitable for the half-band filter due to its distinguished property of having all delay terms $h_{3+4b}z^{-3}$ in each block equal to zero except for the sole center coefficient; otherwise, it needs doubled SC branches for these terms in each block for standard filter, hence increasing circuit complexity.

II. With Triple-Delay ADB's for N>7L : This kind of structure can be further modified by extending the doubled delay in ADB's to a triple one $z^{-3L} = z^{-6}$, as illustrated in Fig.1(b). Such extension of the delay in ADB renders a reduction of ADB's number to only $\lfloor (N-6)/6 \rfloor = 4$ but an increase of filter length of each block to *6*. The corresponding SC circuit is also derived in Fig.3 with the respective clock phases. There, all SC ADB's with doubled input PCTSC branches have the delay of z^{-5} except the first one with the delay of z^{-6} to compose the serial delay line with delays of z^{-6b}. In each block, it contains either no delay or delay terms from z^{-1} to z^{-5}. For half-band filter all the odd coefficients with delays z^{-1}, z^{-3} and z^{-5} are null except center coefficient, so the delay terms with z^{-2} can be realized in the same way of the double ADB case, while terms $h_{4+6b}z^{-4}$ must be realized by doubled SC branches. This structure is still attractive for its minimum ADB requirement with price of only one additional SC branch in each block for half-band filter, while standard lowpass filter needs *3* extra branches in each block for delays z^{-3}, z^{-4} and z^{-5}.

III. With One-Output-Multiplexed-Accumulator for N<7L : The above proposed structure is more adequate for half-band filter with long impulse response length, i.e. *N>7L*. For the case of lower filter length, i.e. *N<7L*, this enhanced structure has not much superiority in saving the ADB's, thus it is not worth for doubling the number of clock phases or even some SC branches in certain cases. For instance, if *N=7*, both the above two structures need totally *3* OA's (*1* ADB+*2* accumulators), while the new combination discussed here also leads to same reduction of *3* OA's (*2* ADB+*1* accumulator) with simpler phases and SC branches (always *2* less OA's than standard canonic realization). Since the odd index coefficients are zero and the middle three coefficients are always positive, such SC architecture flexibly employs z^{-2}-delay ADB's and one output accumulator with multiplexed integrating paths for saving more capacitance area and with also XY feedback [17] for stabilizing OA, as shown in Fig.4. There, two SC ADB's with delay of z^{-2} constitute a serial delay line with delays z^{-2} and z^{-5}, while the coefficient $h_{M+1}=h_4$, with delay z^{-5} can be implemented by positive PCTSC due to its always positive value. Meanwhile, this circuit also takes advantage of eliminating the realization of the second coefficient h_1 (always = 0), hence allowing arbitrary input signal formats.

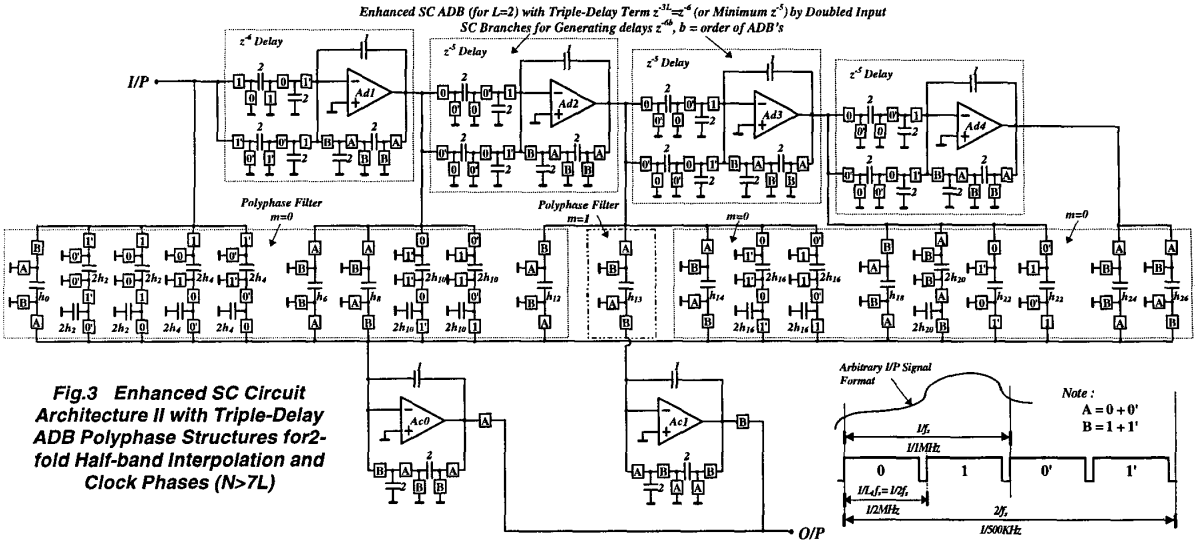


Fig.3 Enhanced SC Circuit Architecture II with Triple-Delay ADB Polyphase Structures for2-fold Half-band Interpolation and Clock Phases (N>7L)

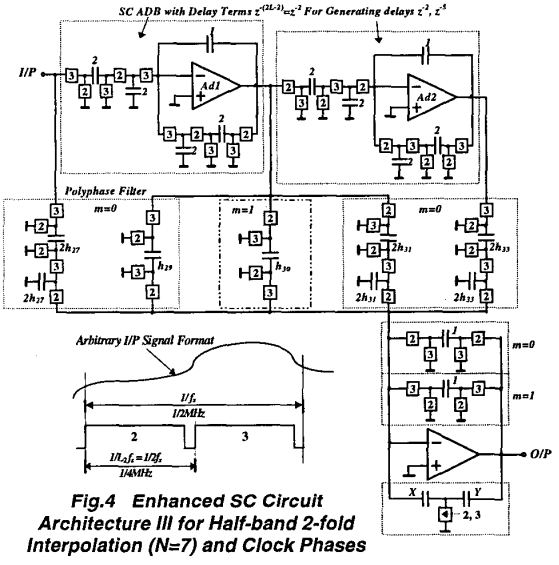


Fig.4 Enhanced SC Circuit Architecture III for Half-band 2-fold Interpolation (N=7) and Clock Phases

A comparison among the above new and previously developed circuit architectures has been examined in Table 1 in terms of components count and clock phases.

Table 1 : The Comparison Among Different Circuit Architectures for Half-band 2-fold Interpolator (N=27)

	Standard Canonic ADB Polyphase	New Enhanced Circuit Architectures		
		III. One-Output Accu.	I. Double-Delay ADB	II. Triple-Delay ADB
Number of ADB's	$B=\lfloor(N-2)/2\rfloor$	$B=\lfloor(N-3)/2\rfloor$	$B=\lfloor(N-4)/4\rfloor$	$B=\lfloor(N-6)/6\rfloor$
Total OA's	$B+2=15$	$B+1=13$	$B+2=8$	$B+2=6$
Clock Phases	$L=2$	$L=2$	$2L=4$	$2L=4$
Extra SC Branches	0	0	1	$B+1=5$

3. MULTISTAGE DESIGN BASED ON HALF-BAND 2-FOLD INTERPOLATION

A very useful utilization of half-band 2-fold interpolator could be in the multistage realization of an efficient and practical interpolation design with regard to power and silicon dissipation as well as sensitivity and accuracy. For instance, we consider an 8-fold interpolation for converting a *400KHz* bandwidth input signal with sampling rate of *1MHz* to an output signal at a *8MHz*-rate, and also the frequency-translated image attenuation of *50dB* are required. For one-stage implementation, the FIR lowpass filter length can be derived as *93*. Thus, total number of *93* passive SC branches are required in the polyphase filters, leading to a large capacitance occupation of filter taps close to *3500* units. Meanwhile, the max. coefficient capacitor spread is about *400*. Thus, these values are too high and impractical for real IC realization. Most importantly, coefficient sensitivity and capacitor ratio accuracy problems seriously limit the circuit performance to be impossible to achieve the demanded specifications [18]. Hence, the multistage designs are desirable for realization due to their inherent efficiency. Table 2 shows explicitly that the 3-stage design using new half-band circuit architectures is much superior and efficient when compared with both one- and even 3-standard-stage design no matter respect to the capacitance area, spread and SC branches as well as number & speed of OA's.

Table 2 : Comparison Among One-Stage, Standard 3-Stage and Enhanced Half-Band 3-Stage Interpolation

L=8	Filter Taps	Non-zero Taps	Cap. Area	Cap. Spread	Number of OA's & Settling Time	Total OA's
ONE-STAGE DESIGN	93	93	3495	399	19, $1/8f_s$	19
3-STAGE DESIGN (STANDARD DESIGN)	$N_1=24$ $N_2=10$ $N_3=6$	40	528	104	13, $1/2f_s$ 6, $1/4f_s$ 4, $1/8f_s$	23
3-STAGE DESIGN (NEW HALF-BAND DESIGN)	$N_1=27$ $N_2=7$ $N_3=7$	25	282	74	8, $1/2f_s$ (New-I) 3, $1/4f_s$ (New-III) 3, $1/8f_s$ (New-III)	14

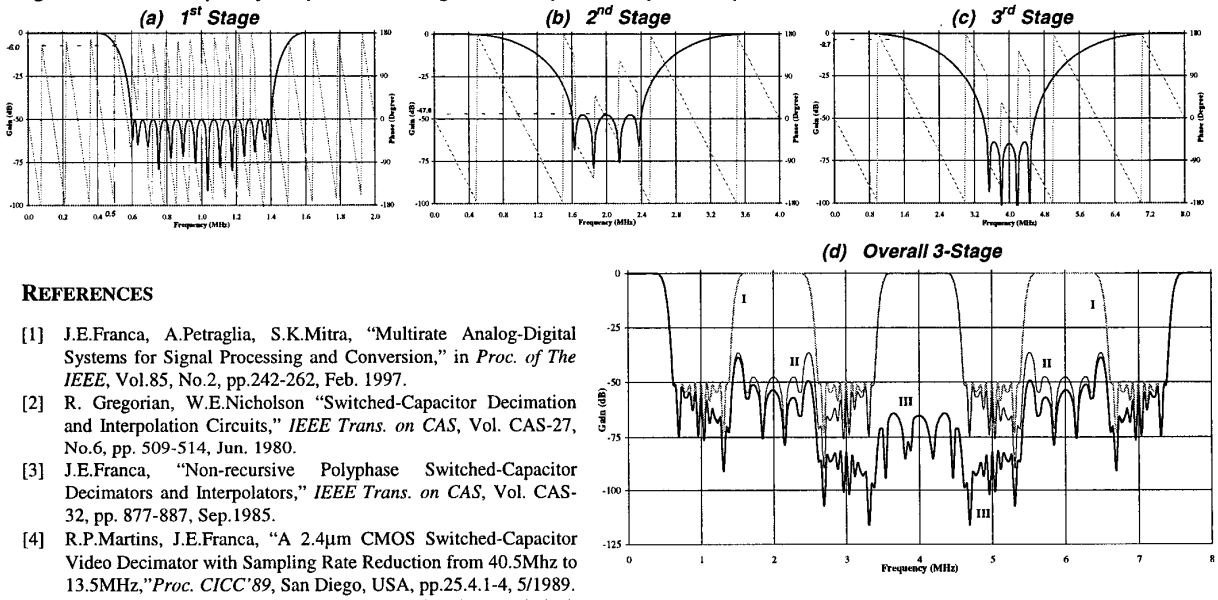
Such 3-stage 8-fold impulse sampled interpolator implemented by using the new enhanced half-band SC

circuit architectures are verified by computer simulations. The resulting frequency response of each and overall stage are obtained in Fig.5 in which Fig.5(a), (b) and (c) clearly manifest their symmetric response of the half-band filtering characteristic, and curve I, II and III of (d) are the amplitude responses of first, first two and overall three stage realizations respectively. It is obvious that all frequency-translated imaging bands formed by sampling the input signals at lower input sampling rate *1MHz* are attenuated separately to the desired loss level by this 3-stage interpolator stage by stage.

4. CONCLUSIONS

The novel SC circuit architectures for impulse sampled analog 2-fold interpolation by efficiently employing half-band filtering techniques have been proposed with a significant reduction in the power and silicon consumption with respect to the required OA's and SC branches as well as capacitance spread & area. Two alternative structures with their corresponding comparative superiority and also a simple circuit realization have been investigated for higher- and low-order applications respectively. A multistage interpolation implementation based on these new half-band SC architectures have also elaborated through a real design example for the illustration of the prominent efficiency in terms of the analog integrated circuitry over the impractical single-stage or even the traditional standard multistage realizations. Behavior-level computer simulations rigorously verify all the proposed circuit architectures and also real implementation of the multistage design.

Fig.5 Simulated Frequency Response of 3-Stage 8-Fold Impulse Sampled Interpolator Based on New SC Half-Band Architectures



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