27.1 A 0.22-to-2.4V-Input Fine-Grained Fully Integrated Rational Buck-Boost SC DC-DC Converter Using Algorithmic Voltage-Feed-In (AVFI) Topology Achieving 84.1% Peak Efficiency at 13.2mW/mm²

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Most existing switched-capacitor (SC) DC-DC converters only offer a few voltage conversion ratios (VCRs), leading to significant efficiency fluctuations under wide input/output dynamics (e.g. up to 30% in [1]). Consequently, systematic SC DC-DC converters with fine-grained VCRs (FVCRs) become attractive to achieve high efficiency over a wide operating range. Both the Recursive SC (RSC) [2,3] and Negator-based SC (NSC) [4] topologies offer systematic FVCR generations with high conductance, but their binary-switching nature fundamentally results in considerable parasitic loss. In bulk CMOS, the restriction of using low-parasitic MIM capacitors for high efficiency ultimately limits their achievable power density to <1mW/mm². This work reports a fully integrated fine-grained buck-boost SC DC-DC converter with 24 VCRs. It features an algorithmic voltage-feed-in (AVFI) topology to systematically generate any arbitrary buck-boost rational ratio with optimal conduction loss while achieving the lowest parasitic loss compared with [2,4]. With 10 main SC cells (MCs) and 10 auxiliary SC cells (ACs) controlled by the proposed reference-selective bootstrapping driver (RSBD) for wide-range efficient buck-boost operations, the AVFI converter in 65nm bulk CMOS achieves a peak efficiency of 84.1% at a power density of 13.2mW/mm² over a wide range of input (0.22 to 2.4V) and output (0.85 to 1.2V).

Figure 27.1.1 shows the system diagram of the proposed AVFI topology, which takes advantage of the quasi-Dickson topology to achieve optimal conduction and parasitic losses for rational buck/boost VCR generation. It consists of n stages of cascaded unit rational cells (RC) carrying equal charge flow, leading to low intrinsic conduction loss as in RSC and NSC under the same VCR. By feeding in either V_{IN} or V_{OUT} algorithmically into each RC stage, it can realize any arbitrary VCR, from (n+1):1 to (n+1):n in buck mode and from n:(n+1) to 1:(n+1) in boost mode, respectively. Voltage-feed-in (VFI) coefficients a_i and b_i determine the involvement of V_{IN}/V_{OUT} in each power cell, while m_i corresponds to the power cell configuration for either Dickson or charge-path folding (QF) mode operation. Depending on the VCR requirement, the AVFI algorithm achieves a unique topology by configuring each RC into one of the 8 possible modes according to the conversion type (i.e. buck/boost) and the VFI coefficients. As shown in Fig. 27.1.1, the Dickson mode involves two cases, TT (top-in-top-out) and BB (bottom-in-bottom-out), as distinguished by the dual-phase charge flow (Q_{flow}) path within an RC cell. In QF mode, the in/out Q_{flow} happens on different plates, denoted by TB and BT. In conventional Dickson topology, the cascaded power cells intrinsically ensure same plate inter-cell charge transfer (Q_{tran}), exhibiting the $C_{i,top}\rightarrow C_{i+1,top}$ or $C_{i,bot}\rightarrow C_{i+1,bot}$ pattern with small bottom-plate switching voltage (ΔV_{CB}). This is in contrast to binary (including RSC and NSC) and series-parallel topologies which incorporate Q_{tran} patterns $C_{i,top}\rightarrow C_{i+1,bot}$ and $C_{i,bot}\rightarrow C_{i+1,top}$, leading to sub-optimal ΔV_{CB} and hence excessive parasitic loss. In the AVFI topology, RCs operating in QF mode can inherently perform a Q_{tran}-path folding function to reduce the parasitic loss due to the direct cascading of TT and BB cells. An illustrative example of a 7:4 buck AVFI converter is shown in Fig. 27.1.1

Figure 27.1.2 shows the theoretical analysis of the AVFI converter with 24 VCRs (11 buck + 13 boost) with comparison to 4-stage RSC (RSC-4) and 3-stage NSC (NSC-3), over the target VCR range from 2:1 to 1:7. The AVFI achieves the same conduction loss as RSC-4 and NSC-3 in both buck and boost modes. Although NSC-3 offers more VCRs via multi-coefficients feedback, many of them show higher conduction losses and can hardly contribute to efficiency improvement especially at heavy load. Due to the quasi-Dickson property of the AVFI converter, we can demonstrate a ~50% parasitic-loss-factor (M_{PAR}) improvement in buck mode, except for 2:1 as all 3 cases result in the same topology. In boost mode, the AVFI topology shows a quasi-linear parasitic loss profile instead of exponentially increasing as in RSC-4 and NSC-3. Figure 27.1.2 also compares the theoretical performance among different topologies. C_{fly} has a bottom-plate parasitic of 8% (typical for MOSCAP), and C_{total}, V_{OUT} and I_{load} are set to 15nF, 1V and 20mA, respectively. The AVFI converter with 24 VCRs shows the best overall efficiency, with >6% efficiency improvement in most VCRs.

Figure 27.1.3 shows the implemented AVFI converter using a partitionable power stage (10MCs + 10ACs) with a scaling ratio (SR) of 5. Unlike RSC and NSC that require weighted power cells, the uniform charge-flow property in the AVFI converter can facilitate modular implementations as shown in Fig. 27.1.1. Power cell partitioning can alleviate the total number of required power cells (N_{CT}) induced by fined-grained VCRs with complete capacitor utilization. The 10MCs+10ACs structure can theoretically realize up to 79 VCRs (40 buck + 39 boost) with a 3× N_{CT} reduction (from 60 to 20). We select a total of 24 VCRs (11 buck + 13 boost) out of 79 according to the target conversion range and power level. The cell partitioning details are summarized in Fig. 27.1.3.

Conventionally, the bootstrapping technique can only accommodate for one fixed reference node across a power switch, requiring connecting the gate control voltage to the absolute system high/low levels to ensure proper switch-off state under the dynamic node conditions for FVCR. This either increases the switch on-resistance, or mandates the use of high-voltage switches. The proposed RSBD resolves this issue by adaptively selecting the proper reference node for accurate switch-off control while ensuring robust operation with low-voltage power switches to reduce the switching loss. Figure 27.1.4 details the power-cell implementation and the proposed RSBD circuit for the dual-phase control of switch T_3, which exhibits the greatest design challenge. The P/N switches ($S_{P/N}$) on the top plate ($T_{1\sim3}$) are alternatively activated in buck/boost modes. With 2b external control (*en* and *lv*), the proposed RSBD incorporates two reference-selection (*RS*) blocks that select the proper high/low reference control levels from the periodically varying node voltages. Besides, the 3 control blocks (i.e. ϕ_{ON} *ctrl.*, ϕ_{OFF} *ctrl.* and ϕ_{dis} *ctrl.*) generate the required gate control signals for the switch on-, off- and disable-states, respectively. The $\phi_{ON/OFF}$ *ctrl.* takes the selected level from the corresponding RS blocks as reference, then pump up/down the system clock to generate the required switch driving voltages V_{GP}/V_{GN} for $S_{P/N}$. The ϕ_{dis} *ctrl.* ties the $S_{P/N}$ gate terminals to the appropriate voltage level during the disable-state. The table in Fig. 27.1.4 summarizes the corresponding $S_{P/N}$ driving states for T_3.

The AVFI SC DC-DC converter (Fig. 27.1.7) occupies an area of 2.4mm² in 65nm bulk CMOS. The on-chip C_{fly} (MIM+MOS) and C_{OUT} (MOS) are ~8nF and ~6nF, respectively. Figure 27.1.5 (top) plots the measured power conversion efficiencies with V_{IN} varying from 0.23 to 2.3V at V_{OUT}=1V, showing high consistency with the simulation result except at high VCRs where the MOS capacitance degradation becomes significant. The peak efficiency is 84.1% at a power density of 13.2mW/mm². The performance is similar for V_{IN}=0.26 to 2.4V with V_{OUT}=1.2V, and for V_{IN}=0.22 to 2.15V with V_{OUT}=0.85V. Figure 27.1.5 (middle) shows the output power delivery range versus efficiency for different VCRs, demonstrating a maximum I_{OUT} of up to 80.1mA at 2:1. Figure 27.1.5 (bottom) depicts the measured transient waveforms at an I_{OUT} step from 4 to 25mA without external capacitors using pulse-skipping modulation, indicating an output ripple voltage (V_{rip}) of 60 and 90mV, respectively.

Benchmarking with state-of-the-art FVCR SC DC-DC converters in Fig. 27.1.6, this work achieves the most VCR, and the highest power density and peak efficiency without using external capacitors. Comparing with the RSC-based topology in [3], this work improves the power density by >13×, at a higher peak efficiency and over a wider VCR range.

Acknowledgements:
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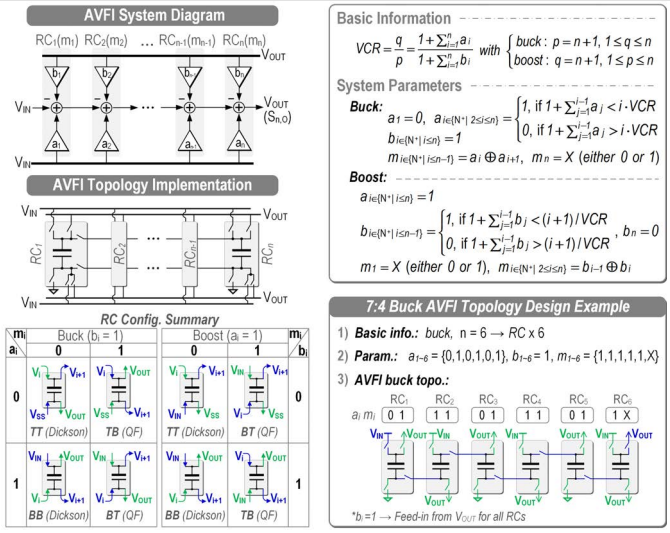


Figure 27.1.1: Proposed algorithmic voltage-feed-in (AVFI) topology with rational cells for arbitrary quasi-Dickson rational buck/boost VCR generation.

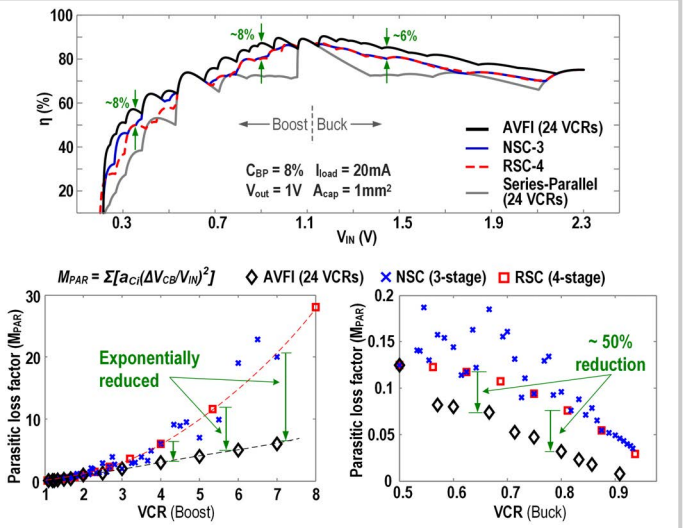


Figure 27.1.2: Simulated efficiency over V_{IN} with C_{BP}=8% (top) and parasitic loss factor (the lower the better) compared to existing topologies (bottom).

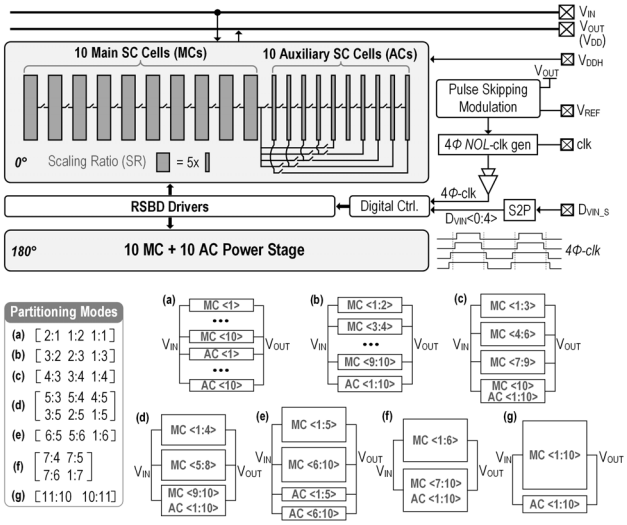


Figure 27.1.3: Proposed 10MC+10AC architecture (top) for AVFI converter with 24 VCRs (11 Buck + 13 Boost) and the cell partitioning modes (bottom).

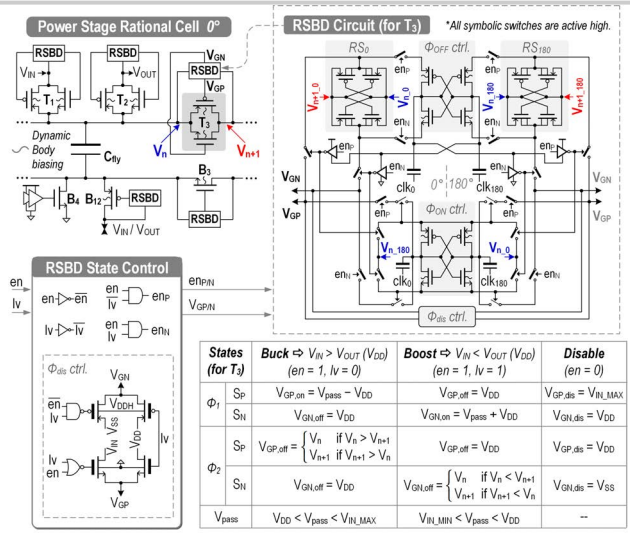


Figure 27.1.4: Rational power cell implementation and proposed RSBD for power switches.

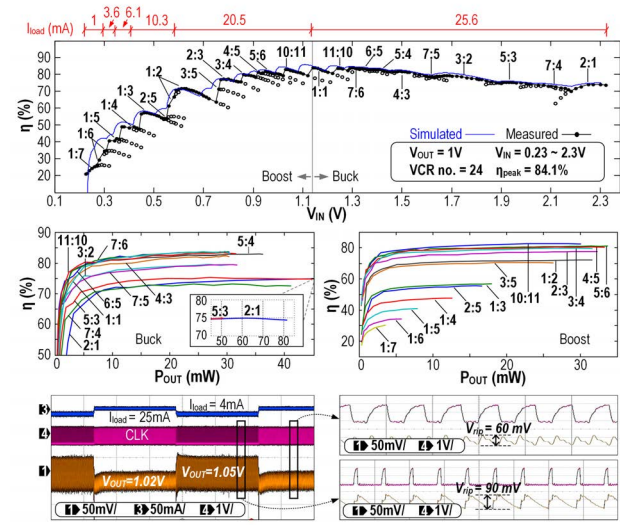
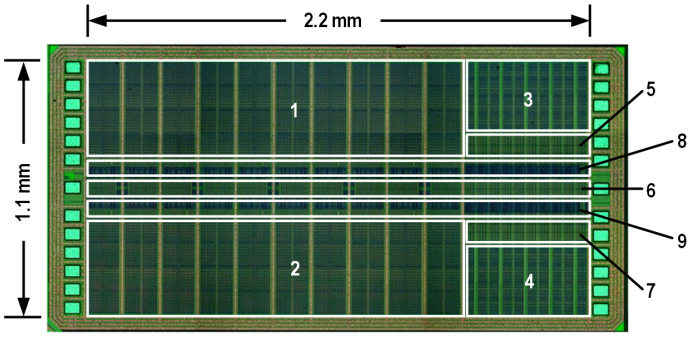


Figure 27.1.5: Measured efficiency versus V_{IN} range (top), efficiency over output power (middle) and load transient waveforms (bottom).

	This work	D. Lutz ISSCC'16	C. K. Teh ISSCC'16	M. Saadat ASSCC'15	X. Hua CICC'15	J. Jiang JSSC'17
Technology	65nm CMOS	0.35μm HVCMOS	65nm CMOS	0.25μm CMOS	65nm CMOS	130nm CMOS
Conv. type	Buck-Boost	Buck-Boost	Buck-Boost	Buck-Boost	Buck-Boost	Buck
No. of VCR	11 buck + 13 boost	8 buck + 9 boost	5 buck + 1 boost	4 buck + 4 boost	3 buck + 3 boost	6 buck
Integrated C_{fly}	MOS + MIM	MIM	MOS + off-chip 1μF	MIM	N/A	Off-chip 4μF
V_{IN} [V]	0.22 ~ 2.4	2 ~ 13	0.85 ~ 3.6	0.6 ~ 2.4	0.5 ~ 3.3	1.6 ~ 3.3
V_{OUT} [V]	0.85 ~ 1.2	5	0.1 ~ 1.9	1.2 ~ 1.5	1	0.5 ~ 3
I_{OUT_MAX} [mA]	80.1	4	10	0.1	0.0033	120
η_{peak} [%]	Buck: 84.1 Boost: 83.2	Buck: 81.5 Boost: 70.9	Buck: 95.8 Boost: 90.5	76	70.4	91
P-den@η_{peak} [mW/mm2]	Buck: 13.2 Boost: 10.2	*Buck: 0.96 *Boost: 0.15	N/A	*0.062	*0.0069	N/A

*Estimated from the corresponding literature

Figure 27.1.6: Performance comparison with state-of-the-art designs.



1~2) 10 MC C_{fly} (MIM + MOS) and C_{OUT} (MOS) for 0° and 180° branches
3~4) 10 AC C_{fly} (MIM + MOS) and C_{OUT} (MOS) for 0° and 180° branches
5~7) RSBDs + digital control
8~9) Power switches

Figure 27.1.7: Die micrograph of the proposed AVFI SC DC-DC converter with 24 VCRs.

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