

## 20.5 A Dual-Symmetrical-Output Switched-Capacitor Converter with Dynamic Power Cells and Minimized Cross Regulation for Application Processors in 28nm CMOS

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Multicore application processors in smartphones/watches use power-saving techniques such as dynamic voltage and frequency scaling (DVFS) to extend battery cycle, and supply cores with different voltages [1]. High-efficiency fully integrated switched-capacitor (SC) power converters with no external components are promising candidates [2]. Typically, SC converters with different specifications are independently designed (Fig. 20.5.1), leading to a large area overhead, as each converter has to handle its peak output power. Recently, multi-output SC converters are reported to tackle this issue. In [3], an on-demand strategy is used to control two outputs, each with a different loading range, and the outputs are not interchangeable. In [4], the two output voltages are fixed with voltage conversion ratios (VCRs) of 2x and 3x only. In [5], the controller is integrated, but the three output voltages are still from three individual SC converters. Without reallocating the capacitors in the power stages, capacitor utilization is low, as margins have to be reserved to cater for each converter's peak output power. This paper presents a fully integrated dual-output SC converter with dynamic power-cell allocation for application processors. The power cells are shared and can be dynamically allocated according to load demands. A dual-path VCO that works independently of power-cell allocation is proposed to realize a fast and stable regulation loop. The converter can deliver a maximum current of 100mA: one output can be adjusted to deliver 100mA, while the other handles a very light load; or both outputs can be adjusted to deliver 50mA each with over 80% efficiency.

Figure 20.5.1 shows the dynamic power-cell allocation strategy. The converter consists of two channels, CH<sub>1</sub> and CH<sub>2</sub>, with output voltages, V<sub>O1</sub> and V<sub>O2</sub>, respectively. Each output is regulated through frequency modulation. The switching frequencies of the two channels are f<sub>1</sub> and f<sub>2</sub>. The goal is to adjust them to be equal so that both channels have the same power density, and the converter achieves the best overall efficiency. Assume, for example, that the two channels start with the same number of power cells, but the load of CH<sub>1</sub> is larger than that of CH<sub>2</sub>. To regulate the outputs properly, we should initially have f<sub>1</sub>>f<sub>2</sub>, and assign more power cells to CH<sub>1</sub>. It means the physical boundary should migrate to the right until f<sub>1</sub> and f<sub>2</sub> are approximately equal. By balancing the power densities of the two channels with an optimal switching frequency, both switching and parasitic losses are reduced. By dynamically adjusting both the number of power cells and the optimal switching frequencies, the channels are able to provide sufficient power to the loads, and utilization of capacitors is maximized.

The power cells are connected to either CH<sub>1</sub> or CH<sub>2</sub> by channel selection switches. The boundary between the two channels is controlled by the outputs of the bi-directional shift register (SR) sel[1:m+n]. The direction of boundary shifting is determined by the frequency comparator. After each comparison, the boundary will only shift along adjacent power cells as sel[1:m+n] will only shift by one bit. As such, potential glitches due to reconnecting power cells are minimized. There are a total of 82 power cells, and they work with interleaving phases to reduce the output ripple voltage. The VCRs of the two outputs (R<sub>1</sub> and R<sub>2</sub>) are determined by the ratio selector that senses V<sub>REF</sub>/V<sub>IN</sub>.

To enable the allocation while minimizing cross regulation, a dual-path voltage-controlled oscillator (VCO) is employed, shown in Fig. 20.5.2. The VCO consists of 82 delay cells that generate the clock phases for each power cell. Each delay cell in CH<sub>1</sub> (DC<sub>1</sub>[n]) has a complementary delay cell in CH<sub>2</sub> (DC<sub>2</sub>[n]). The phases φ<sub>1[n]</sub> and φ<sub>2[n]</sub> are chosen by the MUX and then distributed to the power cell. If sel[n] = 1, DC<sub>1</sub>[n] of VCO (CH<sub>1</sub>) is enabled. At the same time, DC<sub>2</sub>[n] will be shorted by the MUX and the clock phase is redirected to the next cell. In this way, the number of delay cells in each VCO is equal to the number of its power cells, and multiphase interleaving can take effect to reduce the output ripple voltage. The frequency of the VCO is controlled by the error amplifier, and the two outputs are separately regulated, regardless of the power-cell arrangement. As the speed

of the regulation loop is much faster than that of power-cell allocation, stability is ensured. Each power cell consists of 2 flying capacitors and 8 power transistors and the VCR can be 2/3x or 1/2x. The configuration of each power cell is optimized to minimize the parasitic loss [6]. The channel selection switches, controlled by sel[n], connect the local output V<sub>OL</sub> to V<sub>O1</sub> or V<sub>O2</sub>.

Figure 20.5.3 shows the control logic that consists of the frequency comparator and the power-cell shift register. First, the one-shot signals (ck<sub>1os</sub> and ck<sub>2os</sub>) control P<sub>1</sub> and P<sub>2</sub> to charge C<sub>C1</sub> and C<sub>C2</sub> for one clock period only. The ready signals (ready<sub>1</sub> and ready<sub>2</sub>) are activated after charging is finished, and trigger the comparison between V<sub>F1</sub> and V<sub>F2</sub>. After a short delay, C<sub>C1</sub>, C<sub>C2</sub> and logic are reset. For the comparison, if V<sub>F1</sub><V<sub>F2</sub>, meaning that f<sub>1</sub>>f<sub>2</sub>, the direction signal of the shift register is then set as direct=0, and the selection signals will shift left by one bit. This frequency adjustment repeats until f<sub>1</sub> and f<sub>2</sub> are very close to each other. The frequency comparator will then issue stop=1, and shifting will be terminated. To ensure accurate charging, the current sources and capacitors (C<sub>C1</sub> and C<sub>C2</sub>) are well matched. For robust control, offsets are added to the comparators to form a hysteresis window. The whole process is driven solely by ck<sub>1</sub> and ck<sub>2</sub>, without an additional system clock.

The proposed dual-output SC converter was fabricated in a 28nm CMOS process. The active area is 1.2x0.5mm<sup>2</sup>. Fig. 20.5.4 shows the measured waveforms of the steady-state outputs, reference tracking and load transient. Measured results demonstrate that two output voltages can be independently regulated and the two switching frequencies were adjusted to be very close. The measured reference up- and down-tracking speeds were 500mV/μs and 334mV/μs, respectively. No obvious cross regulation was observed at V<sub>O2</sub>, while V<sub>O1</sub> was undergoing reference tracking. With the load at V<sub>O1</sub> switched from 4mA to 40mA, the settling time was within 500ns. The cross regulation at V<sub>O2</sub> was less than 10mV at the rising edge and negligible at the falling edge, verifying that the dual-path VCO control minimized cross regulation.

Figure 20.5.5 shows measured efficiencies with load currents I<sub>O1</sub> and I<sub>O2</sub>. The peak efficiency was 83.3% and the split load currents were 50mA for both channels. With dynamic power-cell allocation, the converter achieved over 80% efficiency consistently when I<sub>O1</sub> and I<sub>O2</sub> were larger than 15mA. Efficiency with allocation is improved by 4.8% vs. without allocation. Fig. 20.5.6 shows the performance comparison, and Fig. 20.5.7 shows the chip micrograph. Via dynamic power-cell allocation, the dual-output SC converter achieves high efficiency over a broad load range for two outputs with minimized cross regulation.

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### References:

- [1] A. Wang, et al., "Heterogeneous Multi-Processing Quad-Core CPU and Dual-GPU Design for Optimal Performance, Power, and Thermal Tradeoffs in a 28nm Mobile Application Processor," *ISSCC*, pp. 180-181, 2014.
- [2] Y. Lu, et al., "A 123-Phase DC-DC Converter-Ring with Fast-DVS for Microprocessors," *ISSCC*, pp. 364-365, 2015.
- [3] C. K. Teh and A. Suzuki, "A 2-Output Step-Up/Step-Down Switched-Capacitor DC-DC Converter with 95.8% Peak Efficiency and 0.85-to-3.6V Input Voltage Range," *ISSCC*, pp. 222-223, 2016.
- [4] Z. Hua, et al., "A Reconfigurable Dual-Output Switched-Capacitor DC-DC Regulator With Sub-Harmonic Adaptive-On-Time Control for Low-Power Applications," *JSSC*, vol. 50, no. 3, pp. 724-736, Mar. 2015.
- [5] W. Jung, et al., "A 60%-Efficiency 20mW-500μW Tri-Output Fully Integrated Power Management Unit With Environmental Adaptation and Load-Proportional Biasing for IoT Systems," *ISSCC*, pp. 154-155, 2016.
- [6] J. Jiang, et al., "A 2-/3-Phase Fully Integrated Switched-Capacitor DC-DC Converter in Bulk CMOS for Energy-Efficient Digital Circuits with 14% Efficiency Improvement," *ISSCC*, pp. 366-367, 2015.

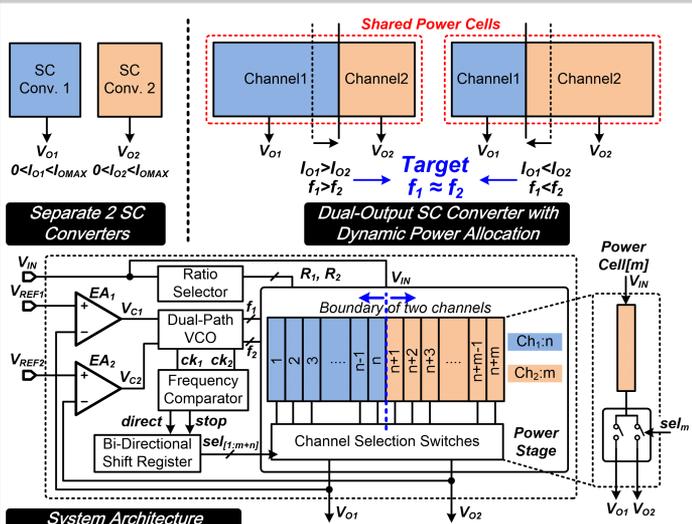


Figure 20.5.1: Strategy of dynamic power-cell allocation and system architecture of proposed dual-output SC converter.

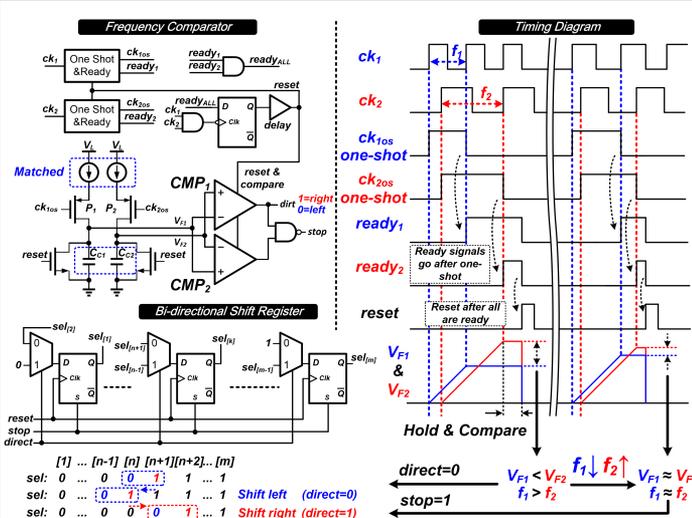


Figure 20.5.3: Circuit implementation of frequency comparator, bi-directional shift register and the timing diagram of frequency comparison.

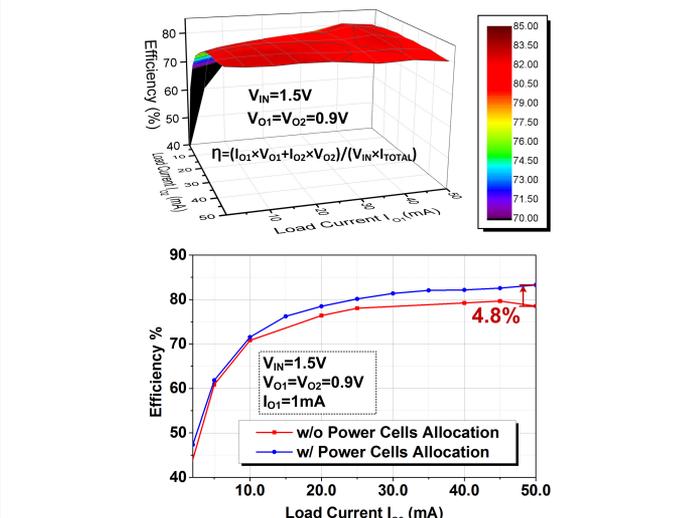


Figure 20.5.5: Measured efficiency versus loading currents with and without dynamic power allocation.

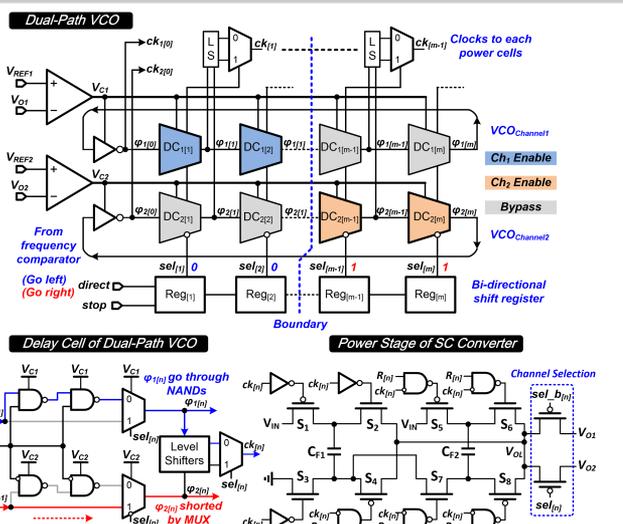


Figure 20.5.2: Circuit implementation of dual-path VCO, delay cell of dual-path VCO and power stage.

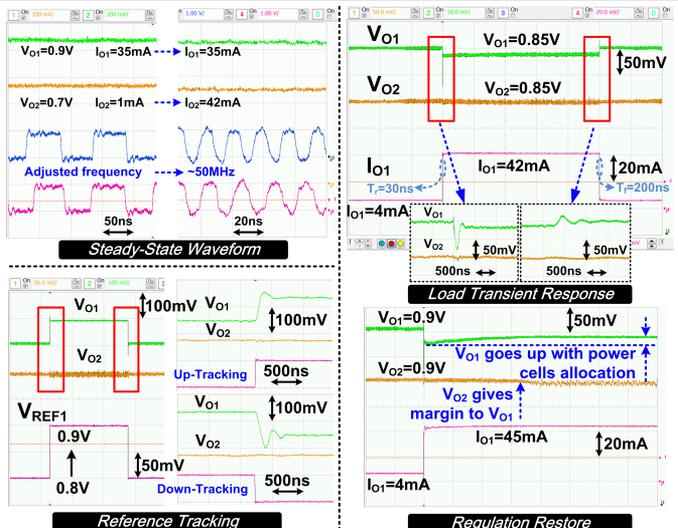


Figure 20.5.4: Measured waveforms of steady state output voltages, reference tracking and loading transient response.

| Work                   | [3] ISSCC '16                                   | [4] JSSC '15                                     | [5] ISSCC '16   | This work  |
|------------------------|---|--|---|--|
| Technology             | 65nm  | 0.35μm   | 180nm   | 28nm   |
| Topology               | Step-Up/Down                                    | Step-Up  | Step-Down   | Step-Down  |
| Number of Outputs      | 2   | 2  | 3   | 2  |
| Passive Type           | On-chip<br>Off-chip                             | Off-chip   | On-chip<br>(MIM+MOS)  | On-chip<br>(MOM+MOS)                                   |
| V <sub>IN</sub>        | 0.85-3.6V                                       | 1.1-1.8V   | 0.9-4V  | 1.3-1.6V   |
| V <sub>OUT</sub>       | 0.1-1.9V  | 2V, 3V   | 0.6V, 1.2V, 3.3V  | 0.4-0.9V   |
| I <sub>o,MAX</sub>     | 10mA  | 24mA   | 100μA*  | 100mA  |
| Total C <sub>FLY</sub> | 1μF   | 9.4μF  | 3nF   | 8.1nF  |
| η <sub>peak</sub>      | 95.8%   | 89.5%  | 81%   | 83.3%  |
| Power Density          | N/A   | N/A  | 250μW/mm <sup>2</sup>   | 150mW/mm <sup>2</sup>                                  |
| Max. Load per Output   | V <sub>O1</sub> : 1mA<br>V <sub>O2</sub> : 10mA | V <sub>O1</sub> : 12mA<br>V <sub>O2</sub> : 12mA | V <sub>O1</sub> : 33μA<br>V <sub>O2</sub> : 33μA<br>V <sub>O3</sub> : 33μA* | V <sub>O1</sub> : 0-100mA<br>V <sub>O2</sub> : 100-0mA |
| Symmetrical Outputs    | No  | No   | No  | Yes  |

\*Extracted from measurement results.

Figure 20.5.6: Comparison with prior art.

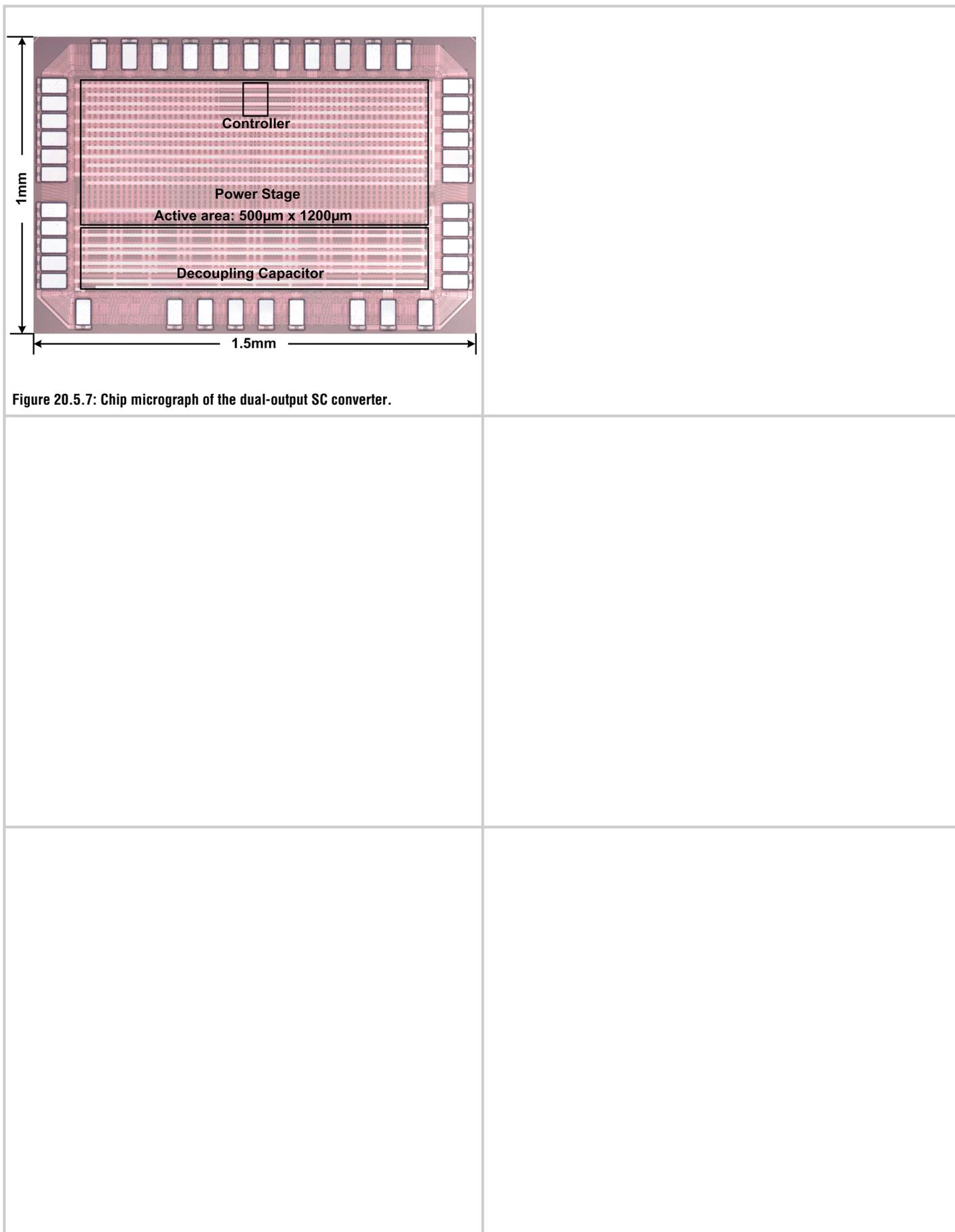


Figure 20.5.7: Chip micrograph of the dual-output SC converter.