A Background Amplifier Offset Calibration Technique for High-Resolution Pipelined ADCs

Li Ding, Sai-Weng Sin, Seng-Pan U, R.P.Martins[1]
Analog and Mixed Signal VLSI Laboratory (http://www.fst.umac.mo/lab/ans_vlsi)
Faculty of Science and Technology, University of Macau, Macao, China
E-mail – dingli19850910@msn.com
(1 - on leave from Instituto Superior Técnico / TU of Lisbon, E-mail - rmartins@umac.mo)

Abstract— **This paper describes a novel offset calibration technique of the residue amplifier (RAMP) for pipelined ADCs. The calibration operates in two phases, completely in the background, without requiring any interruption in the operation of the ADC. In the analog coarse correction phase most of the offset is compensated through the injection of a DC signal at RAMP's input. The digital fine correction phase will eliminate the remaining offset. Simulation results show that with the proposed calibration technique the over-range margin can be released and the SNDR is not degraded.**

I. INTRODUCTION

The utilization of digital assisted techniques in pipelined ADC design has become more attractive in recent years, and several digital calibration algorithms were developed to improve its performance. Traditionally, designers' attention is not focused on the offset errors of comparators and opamps since they can be easily compensated later through error correction [1]. However, with shrinking technologies and scaling down of voltage supplies, in some pipelined ADC architectures the over-range margin is not large enough to accommodate both mentioned offsets, especially for multi-bit-per-stage high resolution pipelined ADC. In this paper, a new calibration method is proposed to eliminate the offset effect of the residue amplifier. The calibration is achieved in two phases, the analog coarse correction phase and the digital fine correction phase. For the analog correction, additional compensation capacitors are added to inject a DC signal at the input of the residue amplifier. For the digital correction, the remaining offset is alleviated in the digital domain. Due to the fine correction the noise level will not increase and the SNDR will be dominated by the thermal noise. With the proposed calibration technique opamp's design will be relaxed since offset requirements will not be necessary and the over-range margin is released thus tolerating a wider error arising from the comparator.

This paper is organized as follows: First, the architecture of the pipelined ADC is described in Section II. Section III explains the random chopping method for extracting the offset of the residue amplifier. Section IV and V describe the coarse correction and the fine correction phases, respectively. Section VI shows the simulation results and the conclusions are presented in Section VII.

II. PIPELINED ADC ARCHITECTURE

The block diagram of the pipelined ADC is shown in Fig.1, with some modifications when compared with the architecture in [2]. It comprises 4 stages with a 4 bits resolution in each. In [2] the residue is amplified by a factor of 8 to allow full input range in the subsequent stage, with one bit redundancy between two adjacent stages. This will be used to provide the error correction function. In this work the amplification factor is set to be 4, value that it is used to relax opamp's design since the bandwidth of the residue amplifier is almost doubled when the gain factor is reduced by half. Because of the reduction in the gain factor the input range of the next stage is also halved, as well as the over-range margin. In this pipelined ADC architecture the input range of each stage is given by $(\frac{1}{2})^{n-1}$ V_{pp}, with an over-range margin of $(\frac{1}{2})^{n+2}$ V, where n is the index of each stage. Then, the over-range margin will be limited. A small mismatch in the opamp could saturate the subsequent stage. Therefore, the opamp offset should be calibrated to release the over-range margin for accommodating the error of the comparators.

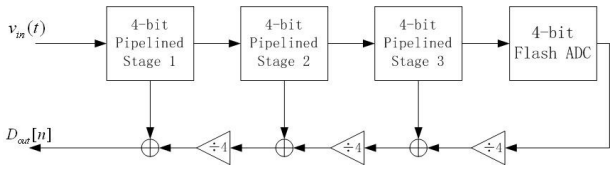

Fig.1: Pipelined ADC Architecture

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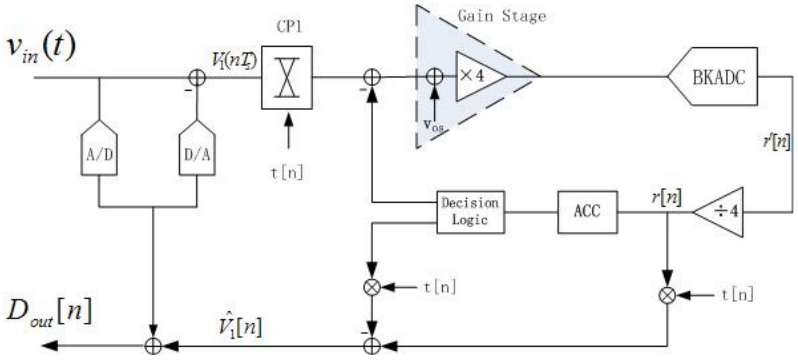

Fig.2: Block diagram of RAMP offset calibration.

III. RANDOM CHOPPER BASED OFFSET EXTRACTION

In the calibration algorithm the offset is extracted by applying a random chopper in front of the residue amplifier similar to [3], but with different calibration actuator. Fig.2 shows a block diagram of the pipelined ADC with the proposed background calibration scheme. The pipelined ADC model is simplified and only the first stage is shown in detail, the succeeding stages are represented by a backend ADC. CP1 represents the analog chopper which is implemented by cross-coupled switches. The switches are driven by a pseudo random number which is statistically independent from the signal. The digital output from the backend ADC r[n] can be considered as the digital representation of the opamp's output,

$$r[n]+Q=V_1(nT_s)t[n]+V_{os} \tag{1}$$

where Q is the quantization noise of the backend ADC. Once the signal dependent term V_1 is chopped it becomes a white noise type of signal. The expected value of r[n] is the input referred offset of the opamp given by,

$$E(r[n])\approx V_{os} \tag{2}$$

In practice, it must be considered that the residue amplifier has a linear gain error and distortion. Supposing that it has a transfer function of $f(\cdot)$ the offset can be theoretically represented by,

$$V_{os}=f^{-1}(E(r'[n])) \tag{3}$$

From above, equation (2) holds only when the gain error and distortion have little effect. The imprecise estimation of the offset will introduce an additional term related to the pn signal at the output of the ADC. This effect will increase the noise level. Simulation results show that when the ADC has a resolution of 12-bit or more this effect must be taken into account. Some techniques from [4],[5] can be used to estimate the gain error or even the distortion. With these parameters the accuracy of the offset estimation can be enhanced by some additional digital manipulations. For example, the offset extracted by E(r'[n]) can be calculated by (3) to improve its accuracy.

IV. COARSE CORRECTION PHASE

The proposed calibration comprises two correction phases. Most of the error is compensated in the coarse analog correction phase. It releases the over-range margin. The rest of the error is adjusted in the digital domain. The analog correction is realized by injecting a DC signal at the input of the residue amplifier. The MDAC with the compensation capacitor is shown in Fig.3.

It is a traditional folded architecture. The compensation capacitors C_c are relatively small comparing with C_1 and C_2. During the sampling phase the top plate is connected to V_{cm}, while in the amplification phase it is connected to a reference voltage depending on how large the offset is. The reference ladder is designed to have a small step size near the V_{cm}. The matching of the resistors in the reference ladder and the process variation of the compensation capacitors are not serious problems because for the coarse correction phase the objective is to release the over-range rather than correcting the error to a specific accuracy. Considering charge conservation the working principle can be presented as follows:

$$\frac{1}{2}V_{in}(C_1+C_2)=(\frac{1}{2}V_o+\frac{1}{2}V_{os})C_2+\frac{1}{2}V_{os}C_1+(V_{r+}+\frac{1}{2}V_{os})C_c \tag{4}$$

$$V_{in}\frac{C_1+C_2}{C_2}=V_o+V_{os,fine} \tag{5}$$

where $V_{os,fine}=V_{os}(C_1+C_2)+(V_{r+}+V_{r-}+V_{os})C_c$ is the remaining offset after applying the analog correction. Obviously, when both V_{r+} and V_{r-} are equal to $-1/2V_{os}(C_1+C_2+C_c)/C_c$, the remaining offset is zero. However, due to the limitation of the step size in the reference ladder the offset cannot be eliminated completely. The correction step size is given by,

$$\Delta_c=\frac{\Delta_r C_c}{C_1+C_2+C_c} \tag{6}$$

where Δ_r is the step size of the reference ladder. To minimize the correction step size both the unit resistor in the reference ladder and the compensation capacitor can be minimized.

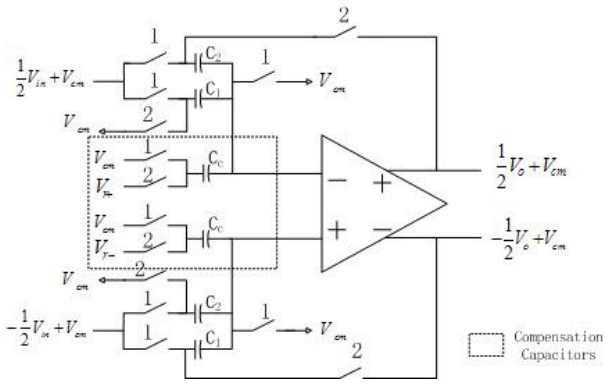

Fig.3: MDAC with compensation capacitors.

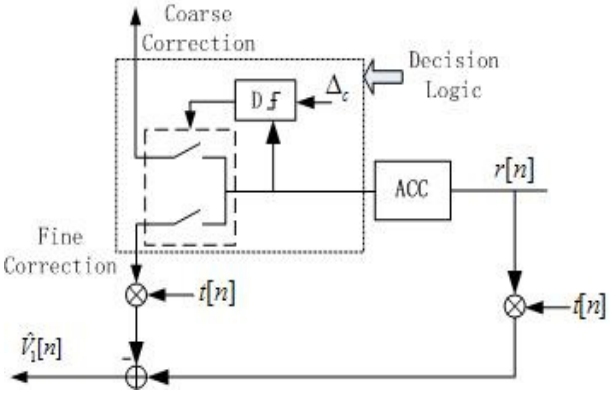

Fig.4: Block diagram of digital correction logic.

V. Fine Correction Phase

For an ADC with low or medium resolution the coarse correction would be sufficient. On the other hand, for high resolution applications the remaining offset will degrade the performance significantly and a fine correction phase must be applied to eliminate the error. The fine correction phase is applied in the digital domain, with the extraction being the same as before. Then, equation (1) becomes

$$r[n]+Q=V_1(nT_s)t[n]+V_{os,fine} \quad (7)$$

The digital correction logic is shown in Fig.4. In equation (7) V_1 is the residue from the previous stage, which is a signal dependent term. To recover it from a chopped output of the backend ADC the estimated offset is subtracted from r[n]t[n],

$$V_1(nT_s)\approx \widehat{V}_1[n]=r[n]t[n]-\hat{V}_{os,fine}t[n] \quad (8)$$

Supposing that from Fig.4 Δ_c is one analog correction step size, a digital comparator compares the extracted offset to Δ_c. If the extracted offset is larger than Δ_c the reference voltage of the compensation capacitor is selected again and the fine offset is extracted once more. If the extracted offset is smaller than Δ_c it would be directly considered to obtain the fine correction. In practice, offset variations may arise from temperature drift and device aging. Decision logic will be used to track the variation of the offset by applying the closest compensation under different conditions.

VI. Simulation Results

The behavior model of the pipelined ADC from Fig.1 was developed. The opamp open loop DC gain was set to 65dB. A $10nV^2$rms white noise signal was added at the input of the residue amplifier to model thermal noise. As mentioned before, the over-range margin is halved when the stage index is increased by 1. So the worst case happens at the output of the 3rd stage, where the over-range margin is only 30mV. Fig.5 shows the residue of the 3rd stage when a 5mV input referred offset was added in the opamp. There is only 10mV over-range margin to accommodate the flash ADC error which is not enough. Fig.6 shows the residue of the 3rd stage when the coarse correction is enabled. Most of the offset was corrected and the over-range margin has been released. Fig.7 shows the convergence of the estimated offset when 2^20 samples were averaged. Fig.8 exhibits the FFT plot. When the fine correction phase was added the SNDR was mainly dominated by the thermal noise.

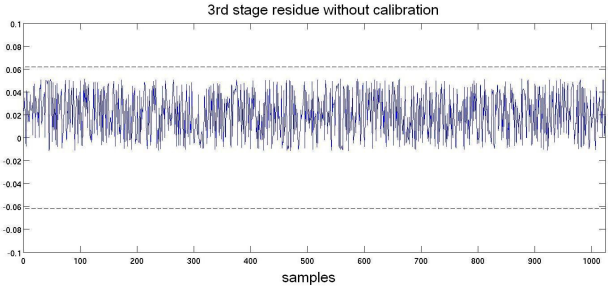

Fig.5: Residue of the 3rd stage without calibration.

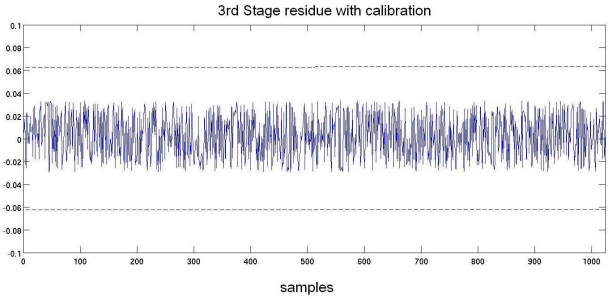

Fig.6: Residue of the 3rd stage with calibration.

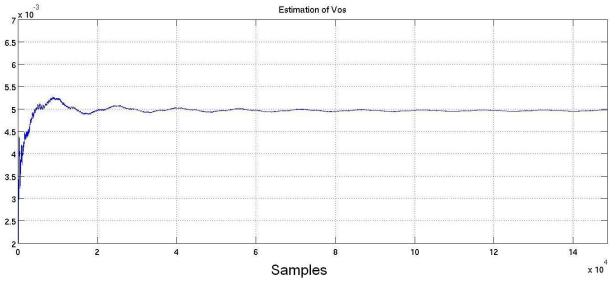

Fig.7: Offset extraction transient response.

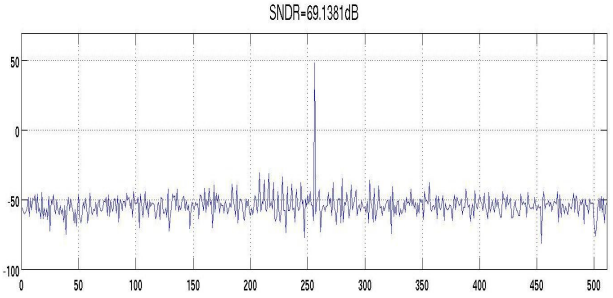

Fig.8: FFT plot of the pipelined ADC.

VII. CONCLUSIONS

In this paper a new background offset calibration technique was presented. It comprises two phases. The coarse correction phase compensates most of the offset in the residue amplifier and releases the over-range margin. The fine correction phase eliminates the remaining offset and allows the calibration technique to be more robust. The simulation result shows that the proposed calibration technique is well-fitted for pipelined ADCs. Additionally, it permits another potential application. Recently, different techniques have been devoted to the correction of the gain error or even the distortion arising from the gain stage, but, they need one or more pseudo random numbers injected at the sub-DAC [4],[5]. The larger the pn amplitude is, the faster the convergence would be [6]. With the proposed calibration technique since the over-range margin is relaxed the amplitude of the injected pn signal can be increased, thus achieving a faster convergence.

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