A 430frms 2.4GHz Ring-Oscillator PLL with Backend Discrete-Time Phase Noise Cancellation Achieving 240.5dB Jitter-FoM

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Research Background

PLL based on Ring-VCO:

- Low phase noise/jitter phase-locked loops (PLLs) are critical building blocks in various systems.
- The LC oscillators have a good phase noise but suffer from large area, magnetic coupling and a small tuning range.
- Ring-VCO PLL suffers from large phase noise and requires a wide-band and high-order filtering.

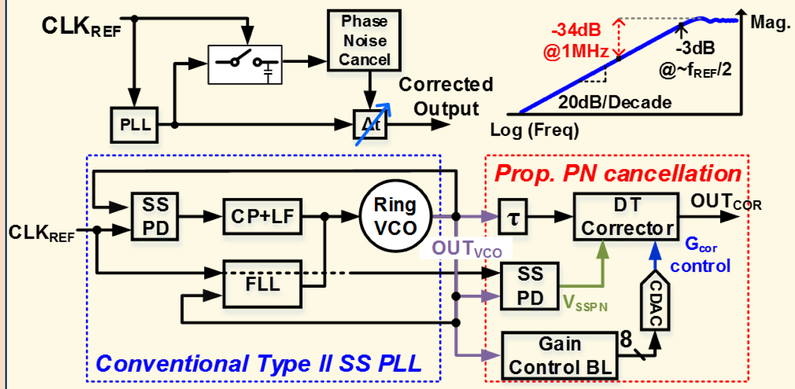
Limitations of state-of-art PLL architectures:

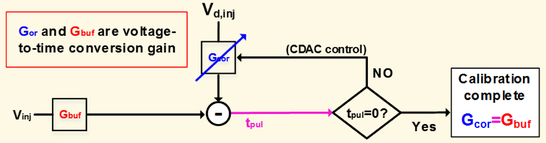
- Wide-band and high-order filtering for Ring-VCO is limited by the loop stability and reference spur.
- The proposed open loop phase noise cancellation is free from both stability and reference spur issues.

Key proposed techniques

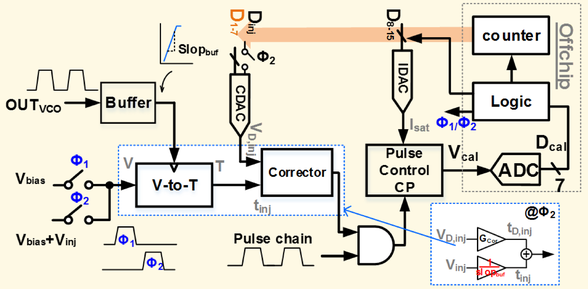
- An open-loop discrete-time phase noise cancellation block.
- Domino-based sampling for good isolation
- A backend gain control algorithm

Proposed Techniques





Algorithm ensure: $G_{cor}=G_{buf}=G_{sampler}$



Architecture:

A conventional Type II sub-sampling PLL followed by a phase noise cancellation block, which provides an extra one order wide-band high-pass filtering.

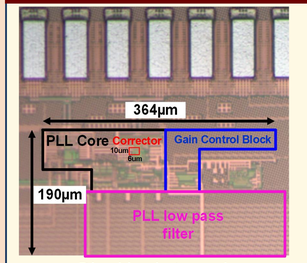
Open-loop phase noise cancellation operation:

- Sampling the noise information from the VCO's output.
- Adjusting the timing Δt of a delay cell in real time.
- Controlling the gain by CDAC.

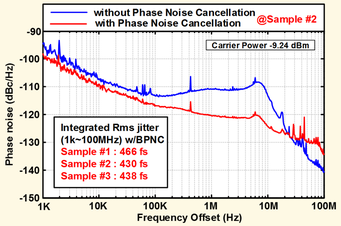
Gain control algorithm:

- A replica corrector with matched gain of main corrector.
- An predefined voltages are connected to calibration circuit
- An off-chip ADC and algorithm converging to correct bias code for CDAC of the corrector to control the corrector gain.
- The algorithm is working in the background, and controlling the gain in real time.
- Negligible error is caused by the mismatch between replica corrector and the main corrector.

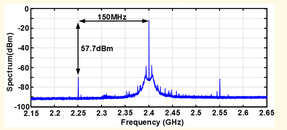
Measurement Results



Die chip photograph



Measured phase noise with and without BPNC



Measured reference spur

	With BPNC	Without BPNC
Phase noise@1MHz dBc/Hz	-120.4	110.9
Integrated jitter (1KHz~100MHz)	430 fs	1.02 ps

Summary and Comparison

	ISSCC15 [1]	ISSCC16 [2]	ISSCC17 [3]	This work
Oscillator Topology	Ring	Ring	Ring	Ring
Reference Freq. (MHz)	22.6	67.74	192	150
Output Freq. (GHz)	2.4	2.1	2.3	2.4
Phase noise @ 1MHz offset(dBc/Hz)	-113.8	-113	-114.4	-120.4
RMS jitter (ps) Integ. range (MHz)	0.97 (0.001~100)	1.05 (0.001~50)	0.72 (0.01~100)	0.43 (0.001~100)
Ref. Spur (dBc)	-65	-45	-37	-58
Power(mW)	4	3.84	4.59	4.8
Area(mm^2)	0.015	0.043	0.0049	0.056
Technology (nm)	45	65	65	28
FOM_1 (dB)	-234.1	-234	-236.2	-240.5
FOM_2 (dB)	175.4	173.6	174.9	181.2

[1] L. Kong, ISSCC2015 [2] Z. Huang,ISSCC2016 [3] J. Chuang, ISSCC2017

★ Introduced least phase noise and no reference spur penalty.
★ The proposed architecture achieves the best both FOM1&FOM2.