Clock-Jitter Sensitivity Reduction in CT ΣΔ Modulators Using Voltage-Crossing Detection DAC

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***Abstract*—A fixed-pulse shape current steering feedback DAC for reducing the clock-jitter sensitivity in CT ΣΔ modulators is presented. Comparing with traditional solutions for clock-jitter effect reduction, the proposed technique uses fixed-pulse shape feedback to achieve higher feedback precision. By applying voltage-crossing detection, fixed-shape feedback pulse with immunity to clock-jitter influence can be generated. A self-reset zero-crossing detector was also designed to reduce the power consumption. The proposed feedback DAC was verified in the design of a 2nd order, 1-bit CT ΣΔ modulator. Full transistor level simulation results show that a 62.5dB SNDR can be achieved with a clock-jitter not larger than 5%T_S. In contrast with the utilization of a general RZ feedback DAC, the proposed technique improves the SNDR by 35dB under 5%T_S of clock-jitter effect.**

I. INTRODUCTION

In recent years Continuous-Time (CT) ΣΔ modulators are extensively utilized in wideband telecommunication systems for their preferable advantages over the Discrete-Time (DT) configuration, namely, high speed, low power and implicit anti-alias filtering [1] [2]. State-of-the-art CT ΣΔ modulators' bandwidth is potentially turning to the hundreds of MHz range [3]; on the other hand, the consumed power can be reduced to less than 5mW [4]. In practice, some non-idealities still limit the performance of CT ΣΔ modulators imposing difficulties in achieving higher speed and resolution. The clock-jitter effect in feedback DACs represents one of the most serious issues preventing the reduction of modulator's In-Band Noise (IBN).

Most of the existing methods to reduce the clock-jitter effect are based on the Shaped-Feedback Waveform (SFBW) technique. It reduces the influence of clock-jitter-induced feedback Pulse-Width (PW) variation by minimizing the amplitude of the tail feedback pulse. However, the common disadvantage of using SFBW DACs is related with the fact that the generated feedback charge amount is inexact due to the jittered feedback PW. Hence the IBN power rises as the clock-jitter increases. To reduce this effect higher feedback peak current is ineluctable. Thus, normally there is a trade-off between clock-jitter tolerance and power consumption.

Another type of technique designated as Fixed-Pulse Shape (FPS) feedback, for jitter sensitivity reduction, was proposed in [5] and it can establish a certain time length through a clock irrelevant operation in the time domain. Since the feedback pulse is generated based on a certain time interval it is immune to clock-jitter. In contrast with the SFBW DAC, the FPS feedback can achieve higher feedback precision within the jitter tolerance. The IBN will not be increased by PW variation induced by uncertain feedback charge amount. Hence the SNR of the system can be maintained stably.

This paper proposes a FPS feedback DAC, where a clock irrelevant fixed time interval is defined based on Voltage-Crossing Detection (VCD). A low power Zero-Crossing Detector (ZCD) is also utilized. The effectiveness of the proposed DAC was verified in a design example of a 2nd order 1-bit CT ΣΔ modulator.

II. VOLTAGE-CROSSING DETECTION (VCD) DAC

A design of a SFBW DAC proposed in [6] is shown in Fig. 1, which can generate an exponential decreasing pulse tail with appropriate feedback peak current. It can effectively reduce the jitter effect without increasing the GBW and SR requirement of the op-amp. However, to create an exponential decreasing shape, additional circuit components are normally required. In Fig. 1(b), the circuit marked by the gray rectangle was applied to create the exponential decreasing current as shown in Fig. 1(a) [6]. This part of the circuit will not be needed in the FPS DAC implementation. In addition, as mentioned previously, using the SFBW method to reduce the jitter sensitivity has less precision than using the FPS feedback.

A. Proposed VCD DAC

By applying FPS feedback the exponential decreasing part in Fig. 1(a) can be removed; the rectangular part will be the generated pulse shape. The configuration of the proposed feedback DAC is shown in Fig. 2. Similar to the structure shown in Fig. 1(b), the VCD DAC also employs a comparator-based circuit. In contrast, the exponential pulse generation circuit is unnecessary anymore. Besides, the feedback DAC implementation marked by the blue dash-line

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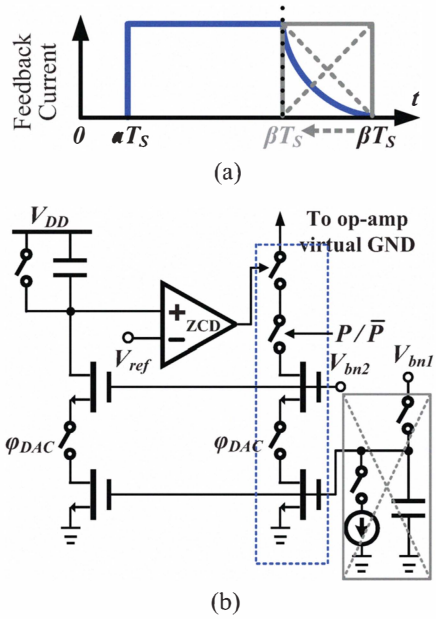

Fig. 1 (a) Feedback pulse generated by (b) the clock-jitter insensitive feedback DAC proposed in [6].

in Fig. 1(b) requires five cascaded transistors, which is not quite suitable for low voltage design. By moving the DAC control switch to the input of the ZCD as shown in Fig. 2, the number of the cascaded transistors can be reduced. Moreover, the V_{ref} connected to the ZCD input prevents the transistors in the current source from entering into the triode region [7].

As illustrated in Fig. 3(a), two non-overlapped clocks are required to trigger and reset the VCD network. In phase φ_1, capacitor C_d is separated from the ZCD and charged to the supply voltage V_{DD}. The positive input of the ZCD is connected to V_{ref} which is lower than V_{CM}, thus the output V_C is kept being "0". DAC feedback starts from φ_2. The constant current I_d discharges C_d during this phase. At the beginning of closing the discharge switch, voltage v_a goes to V_{DD} rapidly as shown in Fig. 3(b), so the ZCD's output will turn to "1". The feedback current is switched on simultaneously. Due to the constant discharge current, the charge amount on the capacitor C_d is decreasing linearly. After v_a dropping down below V_{CM}, V_C turns to "0" again and the feedback current is switched off. Comparing with the waveform on a discharged RC network (proposed in [5]), the voltage shown in Fig. 3(b) is more linear, hence it is easier to be detected. This benefit can reduce the noise effect in the voltage-crossing detection; hence the requirement of the ZCD can be lower.

B. *Clock-jitter Insensitive Function*

Clock-jitter influences the feedback pulse in two sides: feedback PW and feedback pulse position [5]. In the proposed jitter insensitive feedback, the feedback PW is related to the position of voltage-crossing threshold which depends on the speed of capacitor discharge. The feedback PW can be determined by

$$T_{FB} = \frac{C_d\left(V_{DD} - V_{CM}\right)}{I_d} \tag{1}$$

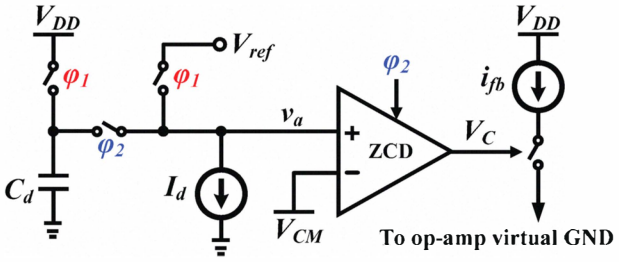

Fig. 2 The structure of the proposed voltage-crossing detection DAC.

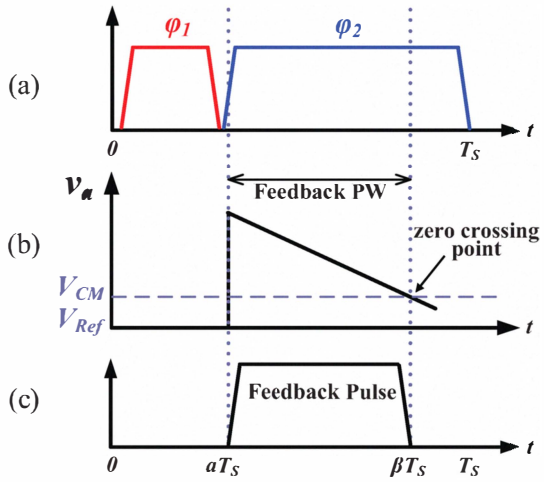

Fig. 3 (a) Control clocks of the proposed VCD DAC. (b) The detected voltage on the ZCD input. (c) The generated feedback pulse.

From (1), the feedback PW is independent of the clock signal. In Fig. 3(c), the clock edge jitter will not affect the feedback PW as long as the total jitter range is less than $(1\text{-}\beta)T_S$ in a clock cycle, which is the clock-jitter tolerance of the DAC.

The feedback pulse position is determined by the value of α as shown in Fig. 3(c). In this design, αT_S is defined by the moment of φ_2 starting. Via using the delayed rising edge of the system clock to trigger φ_1 and φ_2, their relative position to the system clock can be fixed. Thus the value of α is unrelated to clock-jitter.

C. *Feedback Accuracy Analysis*

As analyzed previously, the feedback precision can be immune to the clock-jitter effect by using the FPS DAC. In a clock period, the feedback charges are integrated by the integrating capacitor of the loop filter. This amount of charge will produce a voltage drop on the output of the integrator which describes the feedback result. Based on (1), in current steering feedback loop, the feedback result is expressed as

$$V_{\text{int}} = -\frac{C_d\left(V_{DD} - V_{CM}\right)}{I_d} \cdot \frac{I_{fb}}{C_i} \tag{2}$$

From (2), the output voltage of the loop-filter is related to the capacitor ratio and the current ratio. Thus, it is insensitive to the process variation of capacitors and the transistors in the current source.

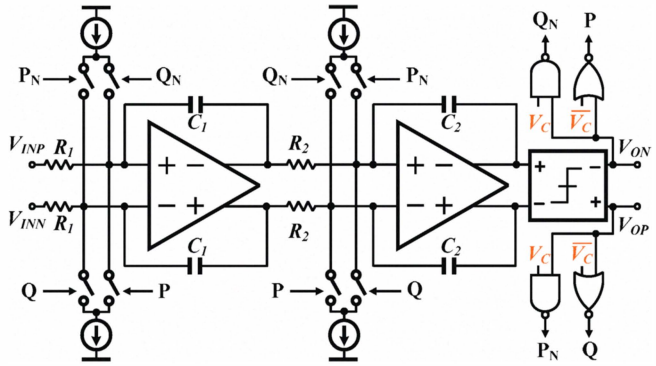

Fig. 4 The circuit schematic of the proposed CT sigma-delta modulator.

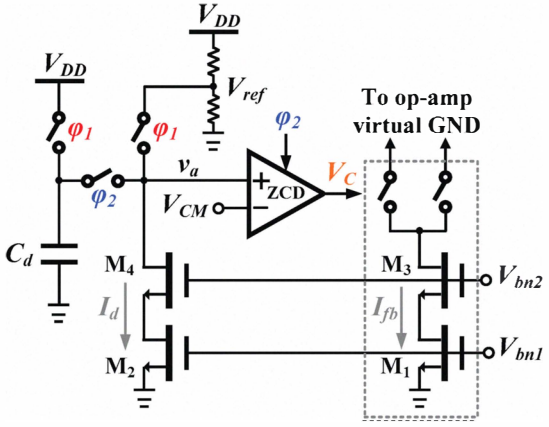

Fig. 5 The circuit implementation of the proposed VCD feedback DAC.

The noises in the VCD network can influence the DAC feedback precision. The noise generated by the ZCD induces the inaccurate voltage-crossing threshold; this error will be injected in the feedback control voltage V_C and transferred into equivalent timing jitter error. The inherent noise of ZCD is inevitable and there is a trade-off between noise and power dissipation. Comparing with inherent noise, the ZCD offset has little influence to the system's performance, and it only causes a little variation of the feedback coefficient.

The input referred noise of the ZCD is due to the shot noise of the constant current I_d that has been discussed in [6]. Referring to [6], this input referred noise can be minimized by reducing I_d. To achieve it, and based on (1), in order to guarantee the defined PW unaltered, the capacitance of C_d should also be reduced. According to the derived noise equation from [6], if the loading capacitor of the current source is reduced, the input referred noise due to the shot noise will increase quadratically. Based on this, if the input referred noise is suppressed by reducing the current, the feedback PW should be decreased simultaneously which will increase the feedback amplitude. Hence there is a trade-off between the input referred noise and the feedback amplitude.

The noise in the reference voltage can also reduce DAC's accuracy. By using the common mode voltage as the reference in voltage-crossing detection, the input referred noise by the on-chip reference ladder can be avoided. V_{ref} is connected to the VCD circuit after the feedback pulse being generated. Thus, the noise on it has no influence to the DAC accuracy.

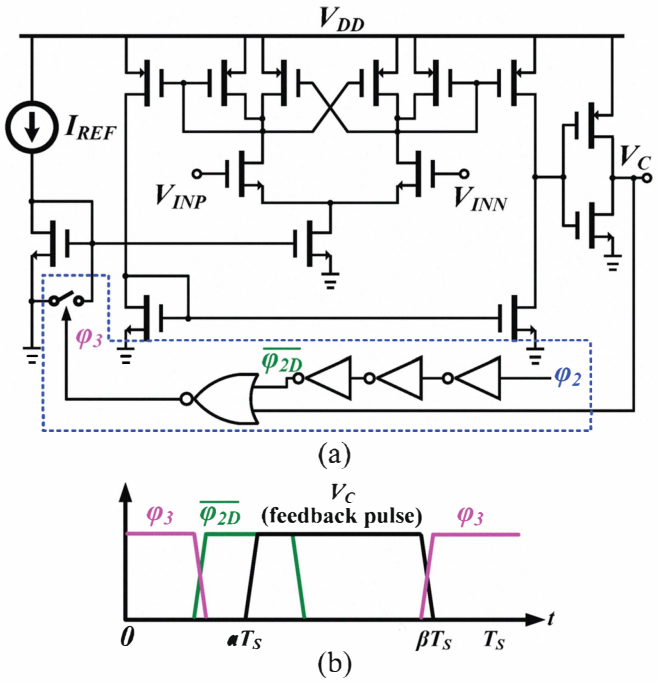

Fig. 6 (a) The proposed self-reset zero-crossing detector. (b) Its control clock.

III. Design and Implementation

A. System Overview

A 2nd order, 1-bit CT ΣΔ modulator was designed and implemented to verify the effectiveness of the VCD DAC in 65nm CMOS technology with 1V supply voltage. Fig. 4 shows the schematic of the designed modulator. Its application is for WCDMA receivers with 2MHz input bandwidth. The sampling rate is 250MS/s according to the OSR of 64. Based on impulse invariant transform, the corresponding DT coefficients can be translated to the CT counterpart. The translated coefficients were scaled down to meet the output swing saturation requirement of the integrators. RZ feedback mode was chosen and the values of α and β are selected to be 0.2 and 0.7. Current steering feedback DACs were employed to match the consideration in (2). The logic gates connected to the modulator's output is for feedback polarity judgment.

B. DAC Implementation

The transistor-level implementation of the proposed VCD DAC is given in Fig. 5. Three transistors are cascaded in the DAC part as marked in the figure to meet the requirements of low voltage design. In practice, to maintain I_d as a constant is difficult, because the voltage on the drain of the current source is going down during the capacitor discharge. Using a cascade structure, the current variation effect can be deduced to negligible. Since the zero-crossing threshold is V_{CM} which is 0.5V in this design, M_2 will not enter into the triode region before the voltage-crossing threshold being detected. Thus, by choosing large transistor channel lengths for M_2 and M_4, I_d can be kept as constant. Since I_d and I_{fb} can be mirrored from a same reference current branch an integer ratio between them can be ensured. As mentioned before, V_{ref} needs not be very

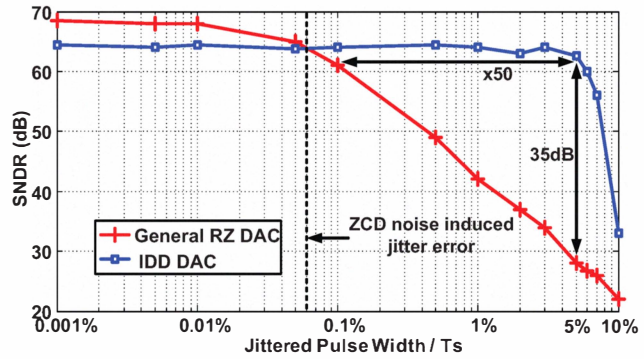

Fig. 7 Simulation results of the clock-jitter tolerance using the proposed and the general RZ feedback DAC.

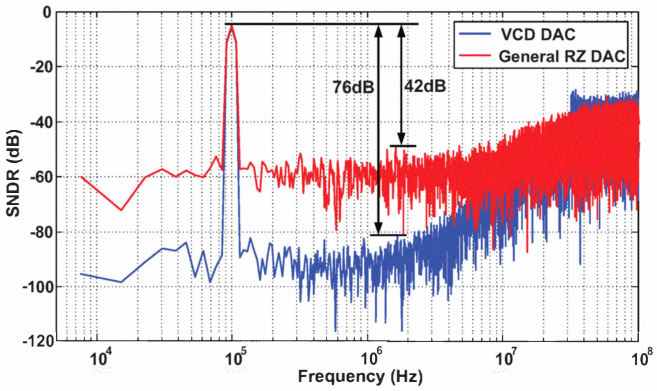

Fig. 8 Simulated output's PSDs of the modulators using VCD and general RZ DAC with 5%T_S jitter effect.

accurate, then, a simple resister voltage divider can be applied to generate it.

C. *Self-Reset Zero-Crossing Detector*

Based on the structure proposed in [8], a ZCD with self-rest function was designed as shown in Fig. 6. To enhance the settling speed, a regenerative latch was employed as the loading of the NMOS input pair. Since an appropriate branch current is required to suppress the inherent noise of the ZCD, a self-reset circuit was designed to reduce the unnecessary power dissipation as circled by the dash-line shown in Fig. 6(a). It will shut the tail current of the ZCD after the feedback pulse being generated and will start it before φ_2 rises. The waveform of its control clock is shown in Fig. 6(b). In practice, ZCD introduces an output offset because of its inherent delay; due to the excess loop delay tolerance of RZ feedback, it will only induce a coefficient offset rather than saturate the loop.

IV. Simulation Results

The clock-jitter insensitive function of the proposed VCD feedback DAC was verified by full transistor-level simulation. The test input signal is in 100kHz with amplitude of -3dBFS. Synchronous jitter was injected into the system clock. All the noises were included in the transient simulation.

The simulation results of clock-jitter tolerance obtained by using VCD DAC and the general RZ DAC are compared in Fig. 7. For 10-bit resolution (62dB SNDR) requirement, the jitter tolerance of using VCD DAC is up to 5%T_S which is at least 50 times larger than using general RZ DAC. The maximum SNDR difference is 35dB. Within the jitter tolerance, a stable SNDR over 62.5dB can be achieved by using VCD DAC. As marked in the figure, the maximum timing jitter error induced by ZCD noise is equivalent to 0.06%T_S clock-jitter. This is the reason why, with a jitter effect of less than 0.06%T_S, the SNDR is higher when using general RZ DAC. With 5%T_S jitter injected, the simulated Power Spectra Densities (PSDs) of the modulators' outputs are shown in Fig. 8. The SFDR difference is around 34dB. From the simulation results it is observed that the proposed DAC can reduce the clock-jitter effect in CT ΣΔ modulators significantly. The additional power consumed by the ZCD is 450μW. By using the proposed self-reset ZCD the power dissipation is reduced by 20%.

V. Conclusions

A current steering feedback technique with reduced clock-jitter sensitivity in CT ΣΔ modulators has been proposed. Comparing it with the shaped-feedback waveform technique, the proposed fixed-pulse shape feedback DAC can achieve higher feedback precision, resulting from the voltage-crossing detection technique. A self-reset zero-crossing detector was designed to reduce its power consumption. The proposed DAC was verified in a 2nd order CT ΣΔ modulator. Simulation results show that it can effectively reduce the DAC clock-jitter sensitivity. The SNDR dropping by clock-jitter effect can be decreased significantly.

Acknowledgment

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