3.5 A 0.6V 13b 20MS/s Two-Step TDC-Assisted SAR ADC with PVT Tracking and Speed-Enhanced Techniques

Minglei Zhang[1], Chi-Hang Chan[1], Yan Zhu[1], Rui P. Martins[1,2]

[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

The two-step SAR ADC is an energy-efficient architecture for high-resolution applications, which faces headroom challenges from the voltage-domain residue amplification under a low power supply. A TDC-assisted SAR ADC [1] uses a voltage-to-time converter (VTC) and a TDC as the back-end to quantize the residue voltage of the SAR ADC, which is attractive to the low power supply scenarios by moving the voltage domain quantization of a two-step SAR ADC into the time domain. However, the TDC-assisted SAR ADC encounters several design challenges. For example, it is sensitive to PVT variations due to partial time-domain operation, and its conversion speed is limited significantly by the long VTC latency when there is a small residue input voltage. This paper presents both PVT tracking and speed enhancement techniques for a 13b two-step TDC-assisted SAR ADC with 0.6V supply. The VTC and the back-end TDC are designed to have a common operation characteristic; thereby, their variations over PVT are inherently tracked without the need of any extra power or circuit overheads. The prototype ADC achieves less than 0.8dB SNDR drop across –50°C to 90°C and ±5% power supply variation at 20MS/s. The Walden FoM is 1.4fJ/conversion-step.

Figure 3.5.1 shows the block and timing diagram of the presented hybrid ADC. A 7b subranging SAR ADC adopts a detect-and-skip switching scheme modified from [2] for voltage-domain quantization. The switching scheme replaces the floated operation in [2] with a solid-connected V_{CM} to keep the common-mode voltage constant during the SAR conversion, while retaining the energy-efficient and high linearity features. A fully dynamic VTC incorporating discharging branches and threshold-crossing detectors (TCDs) converts the residue voltage of the SAR ADC into a time difference (T_P and T_N). Following this, a single-ended time generator produces the input (STA and STO) for the single-ended TDC and gives one sign bit result simultaneously. It also moves the reset instant of STA and STO to the end of the upcoming sampling period for more time margin to the TDC. Unlike conventional two-step TDCs that utilize the PVT-unfriendly time amplifier, the time difference is quantized directly by a 4b flash TDC cascaded with a 3.5b Vernier TDC herein. A 30MS/s maximum conversion rate (with >71dB@LF SNDR) is achieved under a power supply as low as 0.6V, which benefits from 3 design strategies in the time domain: 1) reconfigurable latency VTC; 2) two-step TDC for finer time resolution; 3) pushing part of the TDC conversion into the next sampling period.

The PVT-stabilized technique for the voltage-domain dynamic amplifier in [3] involves a static amplifier and complicated timing control logic. The developed PVT tracking technique eliminates such auxiliaries by tracking the VTC variations with the inherent back-end TDC. Figure 3.5.2 shows the circuit implementation and operation principle of the presented technique. The current source I_D of the VTC consists of one branch of 10 serial unit NMOS and 6 configurable branches of 20 serial unit NMOS. The delay cells in the flash TDC and Vernier TDC have the same topology but with different loading capacitance C_C. Moreover, the current drawn by the rising-edge-related PMOS βI_U is intentionally designed >4× larger than the NMOS counterpart I_U to alleviate the influence from the PMOS-related delay. Based on simulations, the factor β only changes ±3% across –50°C to 90°C and ±5% power supply variation, while the process influence is covered by the configurable I_D of the VTC. The unit NMOS of the current source I_D in the VTC has the same size as the rising-edge-related unit NMOS in the delay cell, and all biased by V_{DD} ($=V_B=V_{OS}=V_T$). Therefore, I_D and I_U share the same PVT response, which results in a PVT-insensitive full-scale (FS) code of the TDC. A low-noise TCD is designed to meet the 13b noise requirement with a dynamic pre-amp and C_1, C_2, while the latency of the VTC can be configured through V_{REF} to achieve a fast V-T conversion. The charge held on the fine SAR CDAC starts to be discharged through I_D at the rising edge of CK_T, and the time outputs T_P and T_N are generated once the residue voltages V_P and V_N cross V_{REF}, respectively. The TCD and the current source I_D are powered down after the time difference T_{RES} is generated for better energy efficiency.

The time residue generator (TRG) in Fig. 3.5.3 connects the flash TDC and Vernier TDC with inherent PVT robustness by removing a time amplifier. To shield the metastability from the time comparator in the flash TDC, the time residue (t_r+t_d) is generated in a complementary manner with a fixed offset t_d. Extra time offset t_d is also added to both STA and STO signal paths for more timing margins under low power supply. Figure 3.5.3 presents a time residue generated example with $1.38t_d$ input to the total TDC. The output code of the Vernier TDC should be inverted to match the residue-generated manner. Different from the TRG in [4] that consumes static power and suffers from non-linearity, a fully dynamic TRG with offset bit shifter is presented, as shown in Fig. 3.5.3. Nodes X and Y are pre-charged before the activation of the delay line in the flash TDC, and then the relevant discharging branches are enabled to generate the rising edges of the residue time difference (S and F). There are 12 delay stages in the 3.5b Vernier TDC, where 4 of them are used for time quantization and the remaining 8 for the offset measurement to the TRG. The offset caused by the TRG is inherently measured and suppressed at the digital back-end through counting the average output code of the Vernier TDC, and then subtracting the TDC output with the measured offset codes. The above operations do not require a known input signal property and have no external intervention, while no further linearity calibration to the TDC delay cells is applied.

The prototype ADC is fabricated in a 1P9M 65nm CMOS process with a core size of 0.053mm^2 as shown in Fig. 3.5.7. Only one-time foreground calibration to the VTC FS time difference and offset is processed, while all the other error sources are covered by the redundancies between stages and the intrinsic matching. A custom designed MOM capacitor array with a single-ended capacitance of 4pF is used to achieve a 13b-level INL of –1.03/+1.31 LSB in Fig. 3.5.4. From the measured 66536-point FFT spectrum in Fig. 3.5.4, the SNDR and SFDR at 20MS/s with a 0.49MHz input signal are 71.5dB and 91.9dB, respectively. The SNDR with Nyquist input is 71.0dB, and stays above 69.5dB with an 18MHz input (Fig. 3.5.4). The presented hybrid ADC exhibits a fully dynamic feature with a similar FoM across different conversion rates. The maximum conversion rate of the design is 30MS/s, while a large design room is reversed to guarantee that the ADC performance is not significantly affected by the sampling network and other non-idealities under PVT variations. The output data of the ADC is decimated by 5 to mitigate the ripple coupled inside the PAD ring. Figure 3.5.5 shows the measured SNDR variation versus temperature and power supply variations of three randomly selected chips, the maximum SNDR drop is less than 0.8dB and 0.5dB across –50°C to 90°C and ±5% power supply variations, respectively. The total power consumption at 20MS/s is 82µW. Figure 3.5.6 summarizes the performance of the ADC and compares it with other state-of-the-art hybrid ADCs. The prototype ADC is not only the only PVT-robust TDC-assisted SAR ADC to date, but it also achieves the best reported FoM of an ADC with both more than 70dB SNDR and 20MS/s conversion rate.

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[5] M. Ding, et al., "A 5.5fJ/conv-step 6.4MS/s 13b SAR ADC utilizing a redundancy-facilitated background error-detection-and-correction scheme," *ISSCC*, pp. 460-461, Feb. 2015.
[6] A. Sanyal, N. Sun, "A 18.5-fJ/step VCO-based 0-1 MASH ΣΔ ADC with digital background calibration," *IEEE Symp. VLSI Circuits*, pp. 26-27, June 2016.

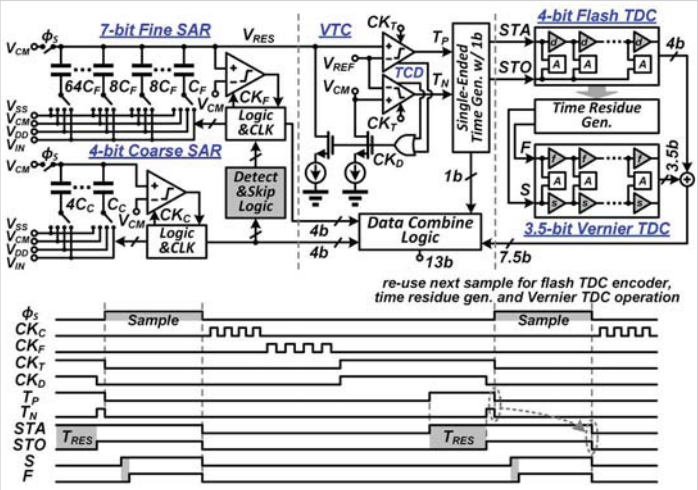

Figure 3.5.1: Block and timing diagram of the prototype 13b two-stage TDC-assisted SAR ADC with speed enhancement techniques (single-ended SAR ADC for simplicity).

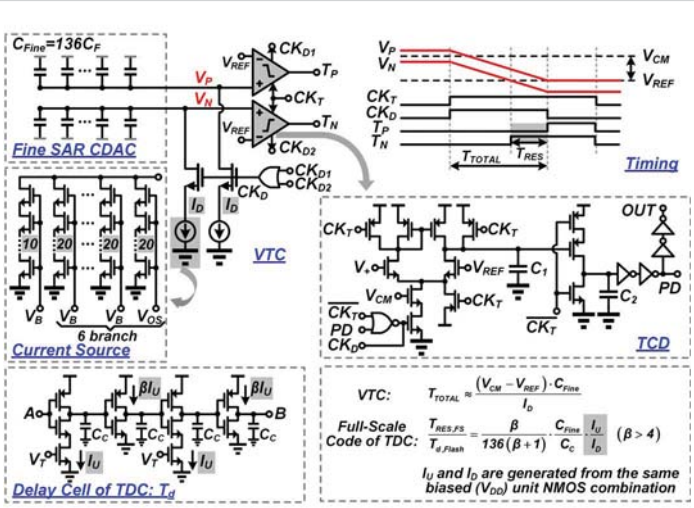

Figure 3.5.2: Circuit implementation and principle of the PVT tracking technique.

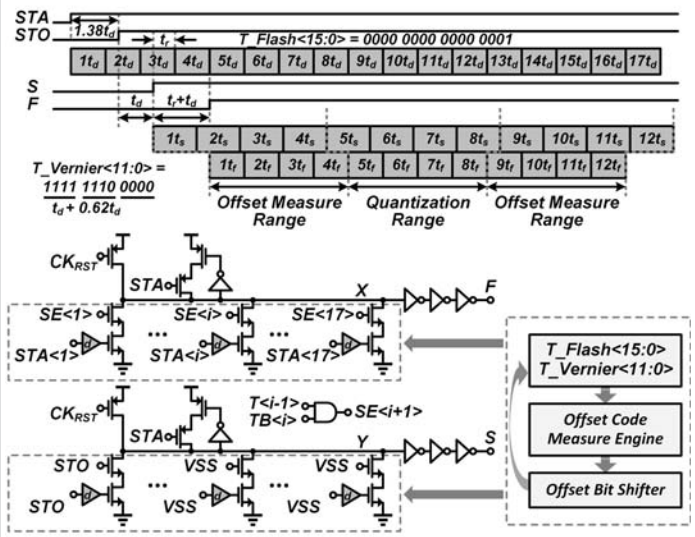

Figure 3.5.3: Fully dynamic time residue generation between the two stage TDC with offset bit shifter.

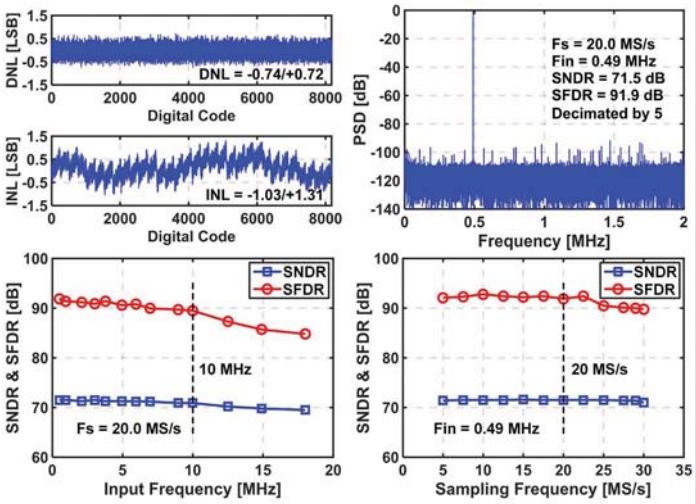

Figure 3.5.4: Measurement results (decimated by 5).

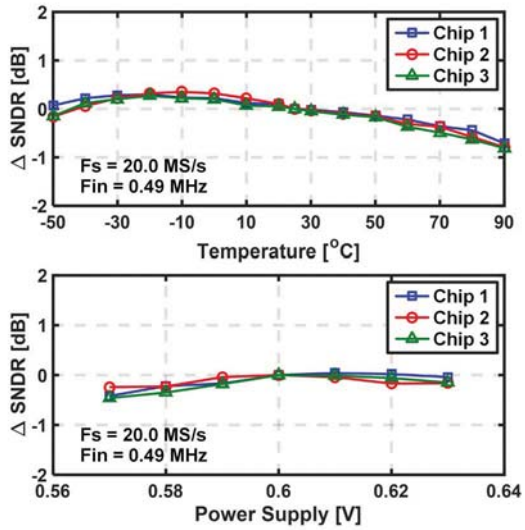

Figure 3.5.5: Measured SNDR variation versus temperature (–50°C to 90°C) and ±5% power supply variation with 20MS/s sampling frequency.

	This Work	[1] JSSC16	[2] ISSCC15	[5] ISSCC15	[6] VLSI16
Architecture	**SAR-TDC**	SAR-TDC	Pipe-SAR	SAR	SAR-VCO
Technology	**65nm**	90nm	65nm	40nm	40nm
Resolution [bits]	**13**	10	13	13	-
Active Area [mm²]	**0.053**	0.041	0.054	0.068	0.030
Power Supply [V]	**0.6**	0.6	1.2	1.0	1.1
Sample Rate (or 2×BW) [MS/s]	**20**	2	50	6.4	6
SNDR @ Nyq. [dB]	**71.0**	54.5	70.9	64.1	71.4
SFDR @ Nyq. [dB]	**89.5**	82.3	84.6	81.9	-
Total Power [μW]	**82**	4.6	1000	46	350
FoM_W @ Nyq. [fJ/conv.step]	**1.4**	4.0	7.0	5.5	18.5
FoM_S @ Nyq. [dB]	**181.9**	167.9	174.9	172.5	170.7

Figure 3.5.6: Performance summary and comparison with other hybrid ADCs.

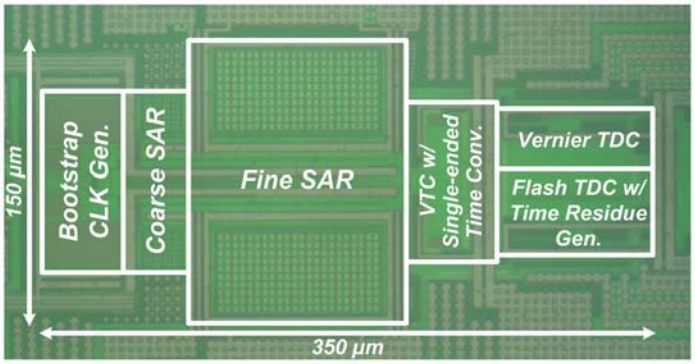

Figure 3.5.7: Die microphotograph.

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