SWITCHED-CAPACITOR FINITE IMPULSE RESPONSE INTERPOLATORS WITHOUT THE INPUT SAMPLE-AND-HOLD FILTERING EFFECT

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Abstract

This paper presents new Switched-Capacitor (SC) Finite Impulse Response (FIR) interpolators whose frequency responses are no longer affected by the input sample-and-hold filtering effect that occurred in previous circuits. Two different types of polyphase architectures are discussed, one based on the Direct-Form (DF) and another employing Active-Delayed Blocks (ADB). The DF polyphase structure is analysed either with input sampled-and-held signals or with arbitrary input signal formats, while the ADB structure will be presented only with arbitrary input signal formats. Examples are given to illustrate both types of SC FIR interpolator circuits.

1. INTRODUCTION

SC interpolators are employed to increase the sampling rate from f_s to Lf_s, with the corresponding rejection of the unwanted frequency-translated image components associated with the signals sampled at lower rate, and hence allowing more relaxed continuous-time post-filtering in SC filtering and digital-to-analogue interface systems. In order to save silicon area and power dissipation, specialised multirate SC circuits were developed based on polyphase structures that could take advantage of the sampling rate increase inherent to interpolation process [1,2,3]. Such SC interpolators, however, have only implemented the interpolation of sampled-and-held (S/H) signals requiring that the original digital interpolating filter $H(z)$ is modified according to [1]

$$H'(z) = H(z) \cdot \sum_{l=0}^{L-1} z^{-l} \qquad (1)$$

Such modification introduces L additional zeros at f_s, $2f_s$...$(L-1)f_s$, as well as their replicas at integer multiples of Lf_s, and therefore yields increased distortion in the overall frequency response of interpolators besides demanding a more complex design procedure and circuit architecture.

This paper presents new SC FIR interpolators which no longer require such modification of original interpolating filter and hence operate in a similar way as their digital counterparts due to the inherent impulse sampled operation at the input. One type of architecture using a direct-form (DF) polyphase structure is presented operating either with an input sample-and-hold signal format (in a simplified form) or arbitrary input signal formats. Another architecture using an Active-Delayed Blocks (ADB) polyphase structures [4], more adequate for higher order applications (due to the simplified circuit architecture) is also presented. Examples of both types of architectures are given and their performance is verified by computer simulations.

2. IMPULSE SAMPLED DIRECT-FORM POLYPHASE SC INTERPOLATORS

2.1 Input S/H Signal Format : For simplicity of explanation, we begin by considering the example of a digital interpolating function where the sampling rate increase is $L=4$ and the interpolating filter with length $N=7$ possesses the impulse response coefficients given in Fig.1(a). Such interpolating function can be implemented by using the DF polyphase structure of Fig.1(b) with one output time-shared accumulator, where, despite the input sampled-and-held signal format, the prototype transfer function of the digital interpolation filters has not been modified, as was previously required [1]. The corresponding SC circuit is derived in Fig.1(c), here, we can see that all SC branches sample the input signal in time slots 8 and 7 but, because of the input S/H signal format, this is equivalent to sampling only once per period $1/f_s$. The interpolated output samples are produced by the $L=4$ DF polyphase filters in time slots 0, 1, 2 and 3. SC branches with normalised capacitance values h_0 and h_4 correspond to the first polyphase filter delivering an output sample in time slot 0. Similarly, SC branches with normalised capacitance values h_1 (or h_2) and h_5 (or h_6) constitute the second (or third) polyphase filter producing an output sample in time slot 1 (slot 2); SC branch with normalised capacitance value h_3 constitutes the fourth

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polyphase filter whose output sample is produced in time slot 3. The computer simulated amplitude response shown in curve I of Fig.1(d) demonstrates that the amplitude response of the SC interpolator is free from the S/H shaping effect at the lower sampling frequency and hence rendering this interpolation process exactly the same as in digital interpolation. For comparison, the amplitude response of the SC interpolator previously available for implementing the same interpolating function by employing a modified transfer function is also plotted in Curve II, clearly showing that the response is affected by the input sample-and-hold format due to the additional zeros at f_s, $2f_s$ and $3f_s$ [1]. Considering the output sample-and-hold effect at higher sampling rate Lf_s, the resulting amplitude response of this SC interpolator is also given in curve III of Fig.1(d).

2.2 Arbitrary Input Signal Formats : Although the input signals of SC interpolators are usually sampled-and-held at f_s, as required in the above SC interpolator, they must be strictly synchronised with the operation of the interpolator in order to guarantee that only one input sample is taken during the interpolation period. Such requirement is overcome by an alternative DF polyphase SC interpolator with more switching waveforms, which are employed for ensuring that all SC branches sample the input signals only once per period $1/f_s$ (lower input sampling period), regardless the input signal format [5]. This is accomplished by using in each of the polyphase filters (except the last one) two paralleled branches clocked at half the input sampling rate and with the same normalised capacitance values. The computer simulated amplitude response of such an SC interpolator, obtained with arbitrary input signal format, is exactly the same as in Fig.1(d) [5].

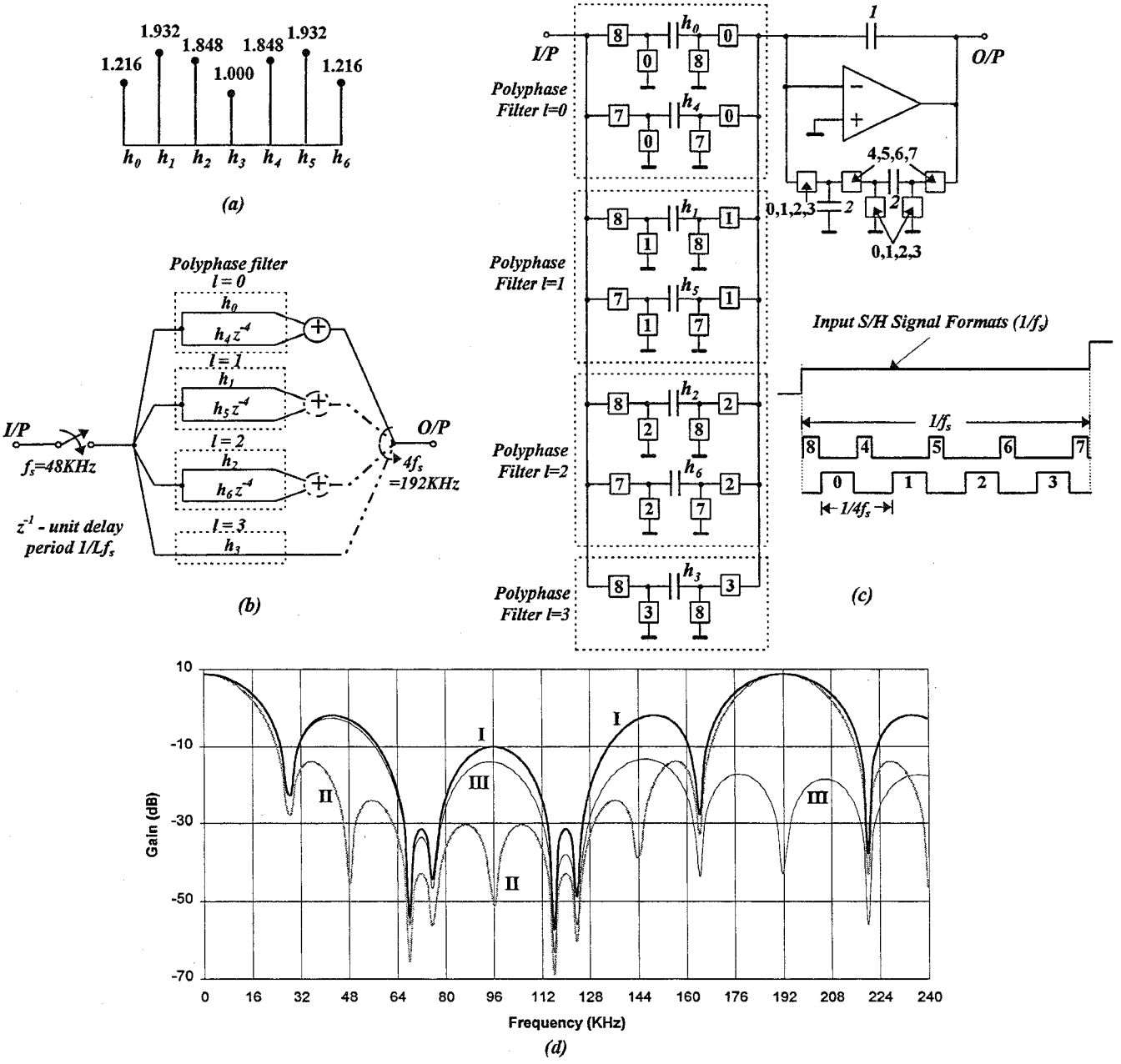
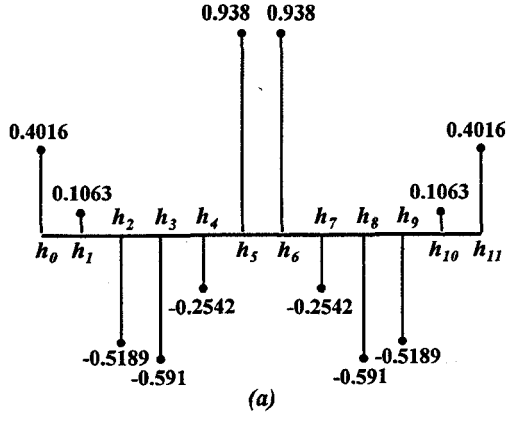


Fig.1 Impulse Sampled Direct-Form Polyphase SC Interpolator for Input Sample-and-Hold Signal Format
(a) Impulse Response of Original "Digital" Prototype Filter (b) Direct-Form (DF) Polyphase Structure
(c) SC Circuit and Switch Timing (d) Computer Simulated Results of SC interpolator

3. IMPULSE SAMPLED ADB POLYPHASE SC INTERPOLATORS WITH ARBITRARY INPUT SIGNAL FORMATS

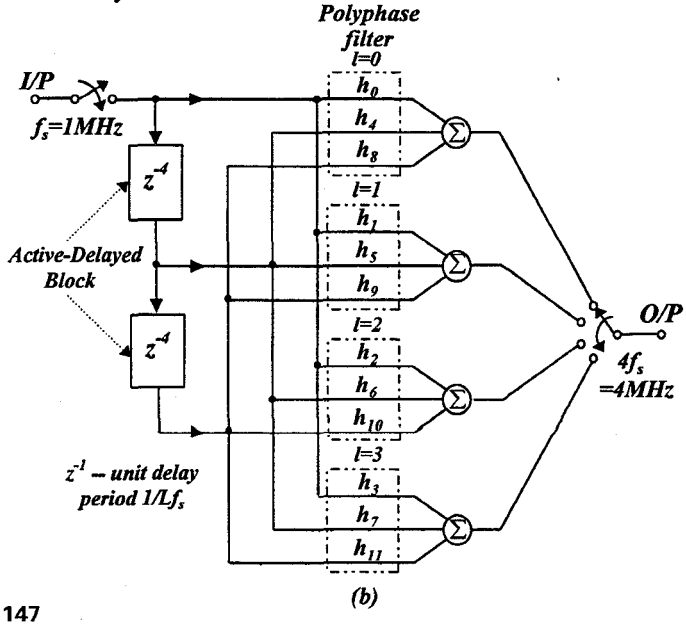
The previous DF polyphase SC implementation may be appropriate when the length of the impulse response N is not much higher than the interpolating factor L, i.e. $N \leq 2L$, due to the requirement of a rather large number of SC branches and complex switching waveforms. Such disadvantage can be overcome by the alternative ADB polyphase SC interpolator constructed by combining the parallel processing DF polyphase structures together with a serial processing delay line for filter length $N>2L$. Such interpolation can be illustrated by means of a design example of a bandpass SC interpolator whose impulse response coefficients are shown in Fig.2(a) with length $N=12$ and an interpolating factor $L=4$ with output sampling rate $4f_s=4MHz$. The resulting ADB polyphase structure and its corresponding SC circuit with the respective switching phases ① are presented in Fig.2(b) and Fig.2(c) respectively. As we can see in Fig.2(c), the upper two OA's with Toggle-Switch-Inverter (TSI) and feedback/reset SC branches constitute two cascaded active-delayed blocks for producing the delay terms $z^{-7/2}$ and $z^{-15/2}$; the rest of the circuit is constituted by 4 DF polyphase filters formed by SC accumulators with input SC branches for realising the correlative delay terms which include the complementary delay $z^{-1/2}$. For relaxing the settling time requirements of OA's, instead of one time-shared accumulator, each polyphase filter has an individual accumulator (1 OA). All SC branches transfer charges to their corresponding OA's only in phase 5 which has a maximum pulse width $\geq 7/8f_s$, so that the settling of the OA's can be close to $7/8f_s$ whereas it is about $1/8f_s$ in the former two circuits, thus relaxing the settling time requirements of OA's both in ADB's and accumulators. Since the output of the OA Ac0 in the accumulator of polyphase filter 0 is sampled in phase 0 with pulse width $1/4f_s$, the settling of Ac0 must be about $1/4f_s$ only. The output of the OA Ac1 is sampled in phase 1 which is the same width of phase 0, but the settling of Ac1 is about $1/2f_s$ because phase 1 has an additional delay $1/4f_s$ of phase 5 whereas there is no delay between phase 0 and 5. Based on this analogy, the settling of OA Ac2 and Ac3 are about $6/8f_s$ and $7/8f_s$ respectively. Another enhancement for relaxing all the settling requirements of OA's in the accumulators is also proposed with switching phases ②. If the circuit block marked by dotted line is employed instead of one output switch of phase 0 in polyphase filter 0 as shown in Fig.2(c), and likewise, if the output switches in polyphase filter 1, 2 and 3 are also replaced by their corresponding counterparts, the output of OA's in accumulators will not be sampled in phase 0, 1, 2 and 3 directly, but will be sampled to charge the capacitors in phase 4 of next period. Then the output will be taken after unity gain buffers in phase 0, 1, 2 and 3 in the next period, causing a linear phase delay in the overall response only. Thus, the settling time of all OA's is relaxed to $7/8f_s$. In addition, the total capacitance area will also decrease relatively, since the capacitors associated with each OA in L output accumulators can be scaled separately, while in the former architecture all the capacitors are connected to the same input node of the OA of one output accumulator. The computer simulated amplitude response of this SC interpolator, obtained with arbitrary input signal formats, is shown in curve I of Fig.3(d). The amplitude response of SC ADB polyphase interpolator with modified transfer function has been also simulated, as shown in curve II. In curve III we can find the amplitude response of this interpolator when the output S/H effect at higher sampling rate Lf_s is considered.



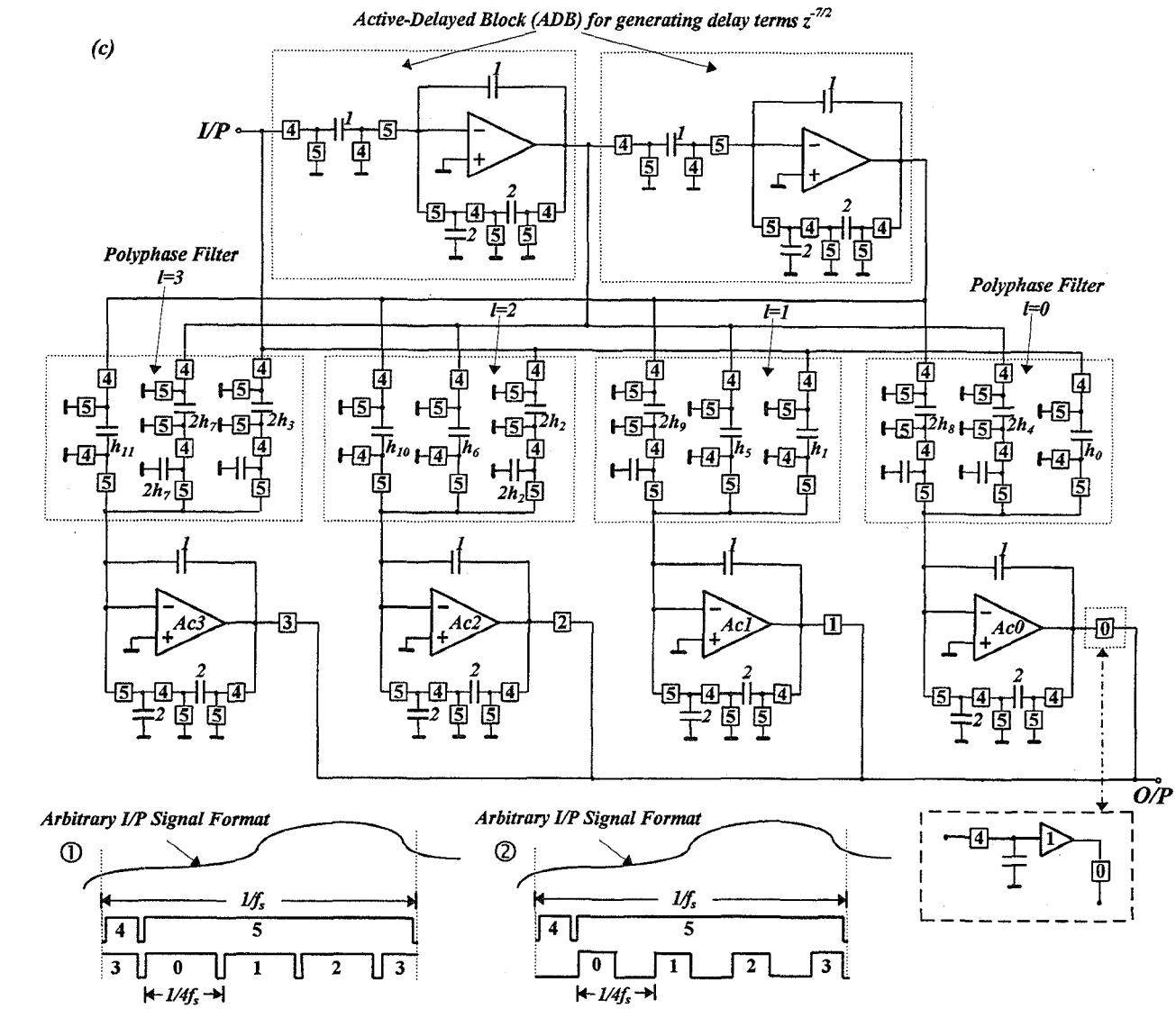
(a)

4. CONCLUSIONS

New impulse sampled SC FIR interpolator circuits were presented, which are no longer affected by the sample-and-hold shaping effect at the lower input sampling frequency. These, are based on DF polyphase or ADB polyphase structures that implement the same digital interpolating function but which require different constraints for the interpolated input signal. The first solution of the polyphase structure can only operate with a properly synchronised sample-and-hold input signal while the second, more elaborated solution accepts input signals with arbitrary formats. Finally, an ADB polyphase structure is presented, appropriate for higher order applications, that will also accepts input signals with arbitrary formats.



(b)



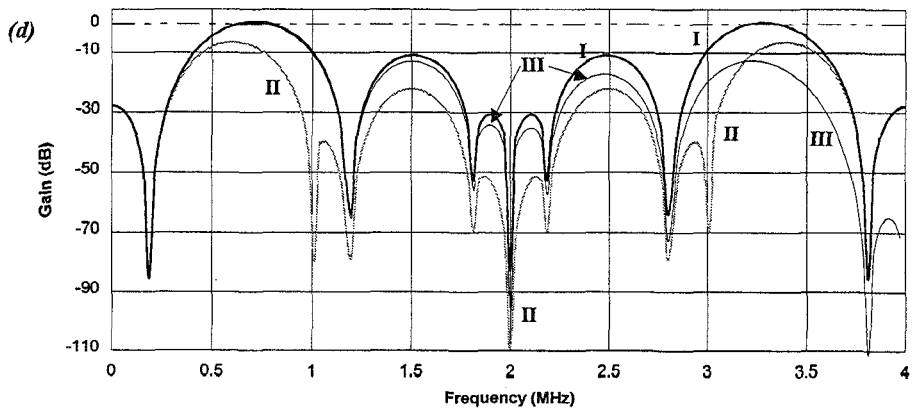


Fig.2
Impulse Sampled SC ADB Polyphase Interpolator With Arbitrary Input Signal Formats

(a) Impulse Response of Original "Digital" Prototype Filter
(b) Active-Delayed Block (ADB) Polyphase Architecture
(c) SC Circuit and Switch Timing
(d) Computer Simulated Results of the SC Bandpass Interpolator

References

[1] J.E.Franca, "Non-recursive Polyphase Switched-Capacitor Decimators and Interpolators", *IEEE Trans. on Circuits and Systems*, Vol. CAS-32, pp. 877-887, 1985.

[2] R.P.Martins, J.E.Franca, "Infinite Impulse Response Switched-Capacitor Interpolators with Optimum Implementation", in Proc. *IEEE International Symposium on Circuits and Systems*, Louisiana, USA, May 1990.

[3] R.P.Martins, J.E.Franca, "Novel Second-Order Switched-Capacitor Interpolator", *Electronics Letters*, Vol.28 No.2, pp.348-350, 13th February 1992.

[4] J.E.Franca, S.Santos, "FIR Switched-Capacitor Decimators with Active-Delayed Block Polyphase Structures", *IEEE Trans. on Circuits and Systems*, Vol.CAS-35, No.8, pp1033-1037, Aug. 1988.

[5] U Seng Pan, R.P.Martins, J.E.Franca, "Switched-Capacitor Interpolators Without the Input Sample-and-Hold Filtering Effect", *Electronics Letters*, in press, 1996.