A Digital Background Nonlinearity Calibration Algorithm for Pipelined ADCs

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***Abstract*—This paper presents a new digital background calibration algorithm for pipelined analog-to-digital converters (ADCs). Background calibration can extract calibration data without interrupting ADCs normal conversion operation. Digital calibration can relax the design difficulty of analog circuits of ADCs, and gains the improvement of technology scaled down. This algorithm provides a method to effectively estimate the nonlinearity of opamp, and calibrates it in digital domain without any additional analog circuit. Simulation results show that the ENOB can be improved from 6.3b to 10.67b by the proposed algorithm.**

I. INTRODUCTION

Digital background calibration techniques haves been applied to pipelined analog-to-digital converters (ADCs) to improve resolution and/or reduce power dissipation. A pipelined ADC comprises some cascaded stages. For example, a 12bits pipelined ADC with 1.5bits per-stage [4]. It comprises 10 1.5bits stages and a 2bits flash ADC. The 10 stages have 0.5 bit overlap to obtain a 10bits digital output with digital error correction. And for each 1.5bits stage, it comprises a sub-ADC which quantizes the stage's analog input, and a sub DAC which generates a corresponding analog signal with digital output of sub-ADC. Analog input subtract corresponding analog signal of sub-DAC to obtain the residue signal. This residue signal multiply a gain factor ("2" for 1.5 bit per stage), and output signal pass to next stage to do the same process until the final 2 bits flash ADC. Digital calibration corrects the digital output of pipelined ADC, and yielding a linear analog-to-digital (A/D) conversion characteristic.

There are some different background calibration schemes. In some schemes, an extra signal is injected into the signal path, and an additional signal range is required [3]. It needs a long time to converge. In other schemes, an additional ADC channel is required. This channel is used to be a reference to calibrate the main ADC channel [4]. But all of them only extract a gain error factor for each stage. Because they assume the finite gain of opamp is much dominate the nonlinearity of itself. They didn't consider the nonlinearity of opamp, so in real design of pipelined ADC, although the gain of opamp is relaxed by digital background calibration, the design a linear low gain opamp is also a difficult issue.

To calibrate the nonlinear issue of opamp and further relax the design of opamp, it needs at least two gain error factors for each stage. With these two gain error factors, the nonlinearity of gain error factor array of opamp can be estimated with a second order polynomial. Using this nonlinear model, the nonlinear gain error of each stage can be calibrated with corresponding output levels.

II. NONLINEARITY OF PIPELINED ADCS

For general pipeline stage, the *j*th stage analog input V_j, is quantized by a sub-ADC. Its digital output D_j, drives a sub-DAC to obtain an analog signal $V_j^{da}(D_j)$. Analog input V_j subtract $V_j^{da}(D_j)$ to obtain a residue signal, and this residue signal multiply gain factor G_j to generate the output signal of *j*th stage V_{j+1}. This is an ideal operation of a pipeline stage. It can be expressed as (1). Generally, switched capacitor circuit is applied to achieve the function of analog input subtract DAC output and multiply gain factor. So the ideal gain factor G_j can be expressed as (2)

$$V_{j+1} = G_j \times \left[V_j - V_j^{da}(D_j)\right] \tag{1}$$

$$G_j = \frac{C_s + C_f}{C_f} \tag{2}$$

C_s , C_f are sampling capacitors of sample and hold circuit. $D_j \in \{-1, 0, +1\}$ is determined with comparison of V_j with the $+0.25V_r$ and $-0.25V_r$. But in reality, the nonlinear finite DC gain A_{0j} and parasitic capacitance of negative input node of opamp C_p also should be considered in gain factor calculation. So the gain factor also can be expressed as (3). And output of DAC $V_j^{da}(D_j)$ can be written as (4).

$$G_j' = \frac{C_s + C_f}{C_f} \times \frac{1}{1 + \frac{1}{A_{0j}} \frac{C_s + C_f + C_p}{C_f}} \tag{3}$$

$$V_j^{da}(D_j) = V_r \cdot \frac{C_s}{C_s + C_f} \times D_j \quad (4)$$

The offset effect due to the input-referred offset voltage of the opamp, the charge injection from the analog switches, and the offset of sub-DAC can be summarized as an offset voltage. This offset voltage can be corrected by digital error correction algorithm. So it is not considered in this transfer function. The output of jth stage can be expressed as (5). For 1.5 bit stage, assume that $C_s = C_f$. (5) can be rewritten as (6). In (6), the analog input of jth stage just multiply a constant factor G_j. If the gain error G_e can be measured, and the transfer function of jth stage can be calibrated to ideal transfer function (1). This is the concept of calibration.

$$V_{j+1} = G_j' \times \left[V_j - V_j^{da}(D_j)\right] \quad (5)$$

$$V_{j+1} = G_e \times \left[G_j \cdot V_j - V_r \cdot D_j\right] \quad (6)$$

with

$$G_e = \frac{1}{1 + \frac{1}{A_{0j}} \frac{C_s + C_f + C_p}{C_f}} \quad (7)$$

In (7), [1], [2] assume A_{0j} is a constant. So the gain error $G_e$also can be written as a constant. But in real opamp design A_{0j} is even function of jth stage output V_{j+1}, which can be expressed as,

$$A_{0j} = A_{dc} + \sum_{i=1}^{\infty} a_i \cdot V_{j+1}^{2i} \quad (8)$$

A_{dc} represents DC gain of opamp. a_i are gain coefficients of polynomial of A_{0j}(Figure 1). If this output dependent gain is considered as a constant for linear calibration algorithm. The output signal which is close to reference voltage after calibration has more Inaccurate than the signal around common-mode level, so nonlinear calibration is applied to achieve higher accuracy of pipelined ADCs.

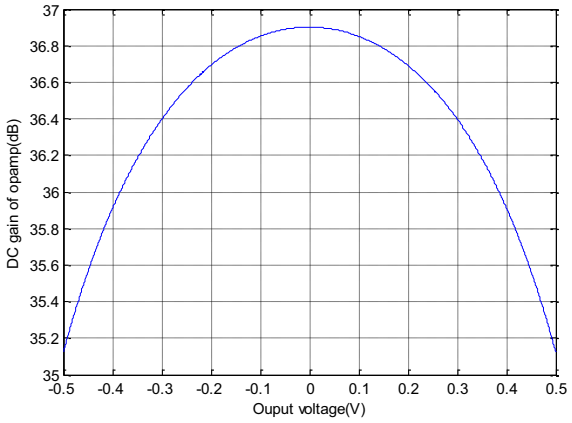

Figure 1. Example of nonlinear DC gain of opamp v.s. output voltage

III. Proposed Gain error extraction Method

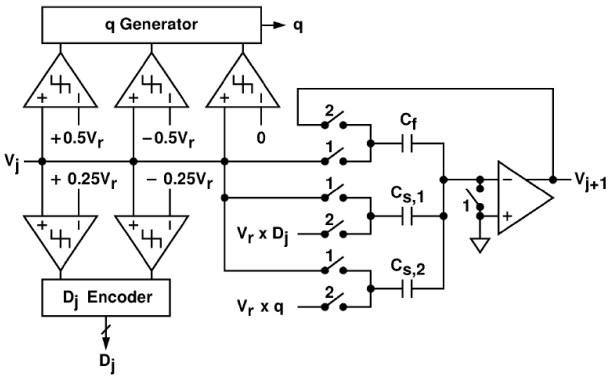

Figure 2. Split-capacitor SC pipeline stage with redundant comparators

In [2], there is a split-capacitor structure applied in 1.5 bit pipeline stage. Two comparators are quantized input signal as typical 1.5bit pipeline stage, and three more comparators are added to control pseudorandom number generator for injecting pseudorandom number into signal path. The structure can solve the over-range issue when pseudorandom number is injected to signal path. As shown in Figure 3, the three comparators divide input signal into four regions A1, A2, B1 and B2, with boundaries at 0 and $\pm 0.5V_r$. When V_j appears in the A1 region, pseudorandom number q can be a random signal +1 and 0. When V_j appears in A2, the injected pseudorandom number q is always +1. When V_j appears in B1 region, q can be alternate randomly between 0 and -1. When V_j appears in B2, q is always -1. This signal dependent pseudorandom number can avoid signal over-range at A2 and B2. If all output signals are collected and be calibrated, then one gain error factor can be extracted after calibration. In the proposed work, one more extracted gain factor is needed. The output signals are collected by region one group comprises A1 and B1, another comprises all four regions signal, and then there are two gain error factors can be extracted. One is gain error factor of mid-region A1 and B1 of opamp's output, another is gain error factor of full-range of opamp's output. This range can be set to different values for each stage. With these two gain error factors, the nonlinearity of opamp can be estimated and calibrated.

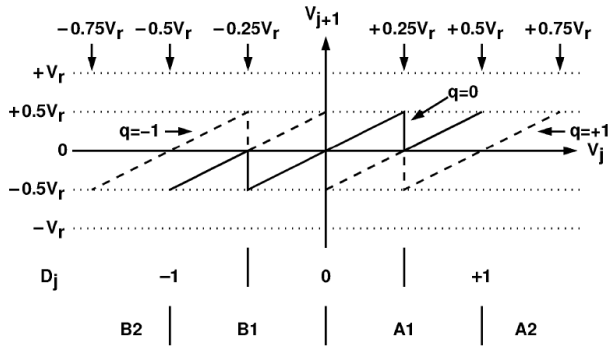

Figure 3. Transfer characteristcis of Figure 2's pipeline stage

IV. NONLINEARITY CALIBRATION ALGRITHM

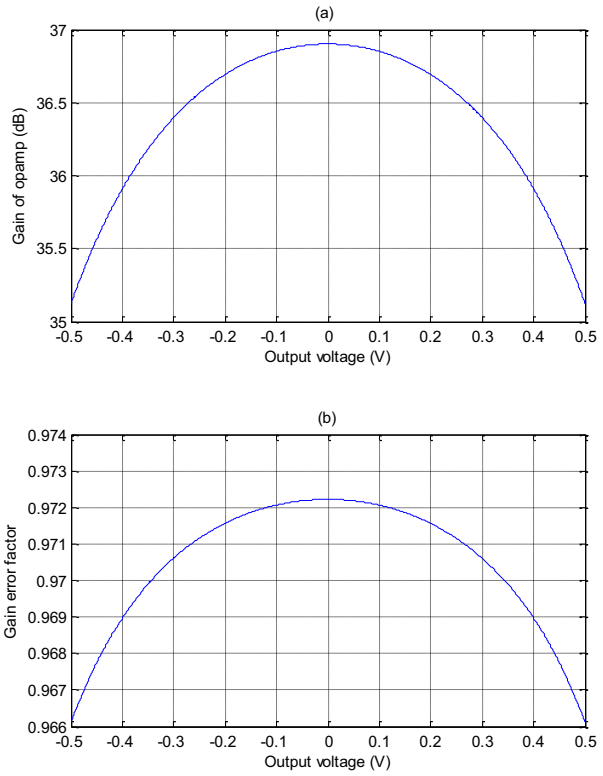

Figure 4. (a) Nonlinear gain of opamp (b)Correponding gain error factor for 1.5bit stage without parasitic capacitance

As (7) shown, all capacitance values are constant for pipeline stage. The only variable in (7) is A_{0j}. It's not difficult to proof if A_{0j} is a even function, that gain error factor G_e has the same characteristic. So the same model can be used to estimate gain error factor G_e.

$$G_{ej} = G_{e0} + \sum_{i=1}^{\infty} b_i \cdot V_{j+1}^{2i} \tag{9}$$

In [1], the digital background calibration extracts gain error factors with correlation-based. This algorithm needs a large number of input samples. For *N*-bit ADC, the order of samples is on the order of 2^{2N}. So the final convergence gain error factor can be considered as the average of these samples. The two gain factors is extracted in Section III also can be considered as the gain average of different output range. Ordinary, the gain error factors of A1 and B1 is larger than that of four regions. (Figure 5)

The two extracted gain error factors can be considered the average of these nonlinear gain error factors at different output range. So, in Figure 5, the area below the green lines (extracted gain error factor) should be equals the area below the blue lines (nonlinear gain error factor curve). With (9), if second order polynomial estimation is taken to approximate the gain error factor curve, the following equations can be written,

$$\begin{cases} \int_{-Vr/2}^{Vr/2} G_{e0} + b_1 \cdot V_{j+1}^2 dV_{j+1} = G_{e1} \cdot 2 \cdot (Vr/2) \\ \int_{-Vr}^{Vr} G_{e0} + b_1 \cdot V_{j+1}^2 dV_{j+1} = G_{e2} \cdot 2Vr \end{cases} \tag{10}$$

In (10), G_{e1}, G_{e2} are extracted gain error factors for A1,B1 region and full region, respectively. There two unknown values G_{e0} and b_1 and two equations, so the values of this two coefficients can be obtain by solving equations. And put these two coefficients back to second polynomial estimation of G_e, the rebuild approximation curve can be drawn as Figure 6.

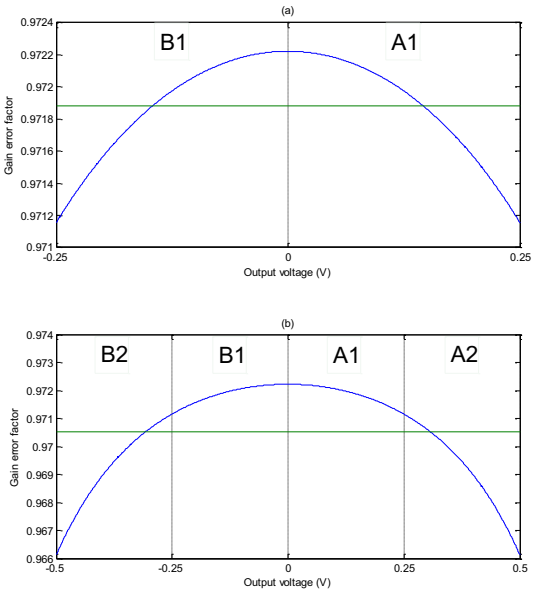

Figure 5. (a) Extarced gain error factor and gain error factor on A1 and B1 (b) Extarced gain error factor and gain error factor on A1, A2, B1 and B2.

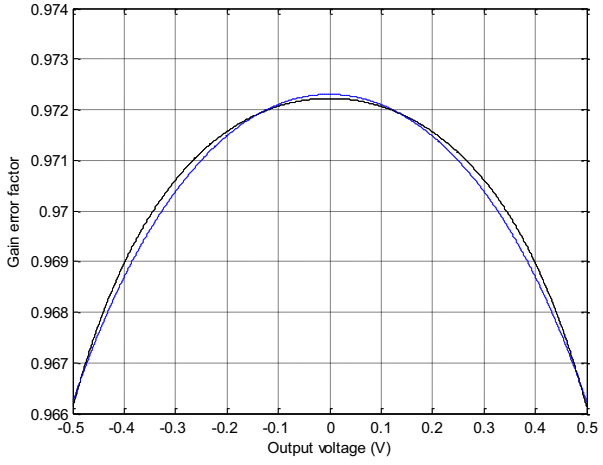

Figure 6. Second order polynomial rebuild G_e,(blue line), and higher order model of G_e pipeline stage simulation (before calibration)

With this second order polynomial gain error factor model, each stage is calibrated with a certain array which instead of a single gain error factor value in linear gain calibration. This second order model is divided to 2^{N+1-j} identical intervals and

calculated an average value for each interval in *j*th stage. So for *j*th stage, there are 2^{N+1-j} elements in gain error factors array, and with digital binary output, the corresponding gain error factors can be identified. With these nonlinear gain error factors and output signals, the rest part of digital calibration is identical with conventional linear digital calibration works.

V. SIMULATION RESULTS

The Matlab model of 12bit 200MHz pipelined ADC is applied to test the performance of proposed digital background nonlinearity calibration with first 6 stages of pipelined ADCs. In pipeline model, the higher order polynomial is applied to build nonlinearity of opamp' open-loop gain. The common-mode DC gain in opamp model is only 37dB. Input frequency is 99.8MHz. I n table I, it shows that the original signal with 37dB open loop gain nonlinear opamp, then SNDR is only 39.82dB. With linear calibration, finite open loop gain issue can be improved so much and achieve a higher SNDR 57.35dB. But harmonic distortion is still a dominate issue of output. With proposed nonlinear gain calibration, the harmonic distortion issue also can be suppressed with 65.98 dB SNDR.

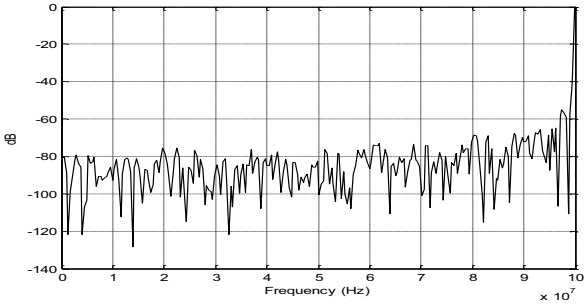

Figure 7. The FFT of output without calibration

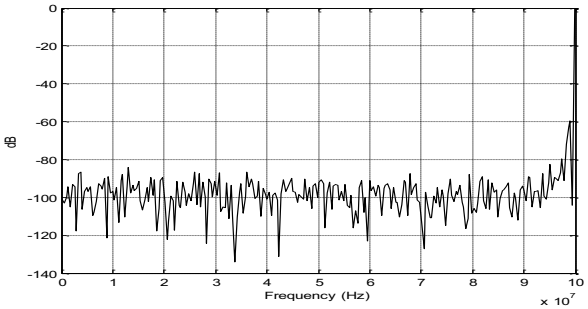

Figure 8. The FFt of output with digital background linear calibration

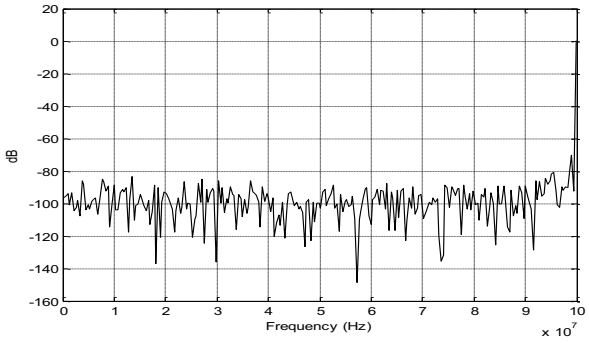

Figure 9. The FFT of output with digital background nonlinear calibration

TABLE I. SIMULATION RESULTS OF DIFFERENT ALGORITHM

	Comparison of different Algorithm		
	Original output without calibration	***Digital background linear calibration***	***Digital background nonlinear calibration***
SNDR(dB)	39.82	57.35	65.98
SFDR(dB)	40.45	59.45	70.34
ENOB(bit)	6.32	9.23	10.67

VI. CONCLUSIONS

This paper describes an algorithm of nonlinear gain digital background calibration for high resolution pipelined ADC. Comparing with linear digital background calibration, this algorithm can further relax the design difficulty of opamp in pipeline stage or achieve a lower common-mode DC gain and/or higher speed. But this algorithm still has some limitation. For example, two gain error factors are extracted which need more samples to converge, and output range for integration in (10) is different for each stages which need set them respectively.

VII. ACKNOWLEDGMENT

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VIII. REFERENCES

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