9.4 A 0.5V 1.15mW 0.2mm² Sub-GHz ZigBee Receiver Supporting 433/860/915/960MHz ISM Bands with Zero External Components

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The rapid proliferation of Internet of Things has urged the development of ultra-low-power (ULP) radios at the lowest possible cost, while being universal for worldwide markets. Both current-reuse [1,2] and ultra-low-voltage [3] receivers are promising solutions. [1] unifies most RF-to-BB functions in one cell for current-mode signal processing, resulting in a high IIP3 (–6dBm) at small power (2.7mW) and area (0.3mm²). However, outside the current-reuse cell, another supply is required for other circuits, complicating the power management [1,2]. [3] facilitates single-0.3V operation of the entire receiver at 1.6mW for energy harvesting, but the limited voltage headroom and transistor f_T call for bulky inductors/transformers to assist the biasing and to tune out the parasitics, penalizing the IIP3 (–21.5dBm) and area (2.5mm²). In both cases, a fixed LC network was adopted for input matching and pre-gain to lower the NF, which is costly and inflexible for multi-band designs.

Aiming for a single-0.5V ULP receiver for sub-GHz ZigBee (IEEE 802.15.4c/d) products (e.g., [4]), three circuit techniques are proposed: 1) An RF-to-BB-recycled front-end concurrently amplifies the RF (in common mode) and BB (in differential mode) signals under the same set of gain stages, squeezing the power by *frequency separation* and *signal orthogonality*. 2) An N-path (N=4) tunable LNA, embedded into the front-end, realizes low-noise input impedance matching while offering area-efficient blocker filtering to enhance the out-of-band linearity. 3) A VCO with extensively-distributed negative-gain cells for current-reuse with the BB complex low-IF filters is employed. With 1.15mW of power and 0.2mm² of area, the receiver shows 8.1dB NF and –20.5dBm IIP3 over the 433/860/915/960MHz ISM bands APT for China, Europe, North America and Japan, respectively, with zero external components.

The RF-to-BB-recycled front-end (Fig. 9.4.1) is described using the I channel. With C_i and C_o considered as short circuits at RF and ignoring their memory effects (detailed later), *Path A* amplifies the common-mode RF signal (and blockers) from V_i to V_o, where the two G_m stages are in parallel. *Path B* routes V_o to the two passive mixers for single-to-differential downconversion. *Path C* returns the differential BB-signals $V_{B1,I\pm}$ to the two G_m stages individually, recycling their gain orthogonally for BB amplification. Elegantly, BB filtering is inherent with C_i and C_o, as the differential BB signals and blockers see V_i and V_o as virtual grounds. Together with the Q channel, a functional view of the front-end (Fig. 9.4.2) is a single-ended $4G_m$ inverter-based LNA self-biased by $R_F/4$, followed by four I/Q passive mixers loaded by C_i, and finally by four *virtual* $1G_m$ BB amplifiers loaded by C_o. This topology not only nullifies the BB power, but also avoids the RF balun and balances the NF ($4G_m$ at RF) with linearity ($1G_m$ at BB).

When the memory effects of C_i and C_o are taken into account, the passive mixers become a 4-path switched-capacitor (SC) network, advancing the LNA into an *equivalent 4-path tunable LNA* (Fig. 9.4.3). For simplicity, we assume C_o is a short circuit at RF, but keep C_i since it dominates the frequency-translated filtering effect. After one LO cycle ($1/f_{LO}$), V_i is sampled and held by C_i building the 4-phase voltages (V_{ci}, $-V_{ci}$, jV_{ci}, $-jV_{ci}$). For the in-band RF signal, those voltages are in-phase-summed at V_o in the steady state. For the out-of-band RF blockers, those voltages are out of phase and cancelled when appearing at V_o. This bandpass effect can be modeled as an R_p-L_p-C_p resonator in series with the mixer's on-resistance (R_{sw}), and the center frequency is tunable by f_{LO} via L_p. It can be proven that such a resonator can be equivalently placed as the feedback network of the $4G_m$ stage (Fig. 9.4.3), rendering three benefits when comparing it with the passive N-path filter [5]: i) a closed-loop gain ($A_{v,LNA}$) much greater than 1 is feasible and bandpass filtering occurs twice at both V_i and V_o, enhancing the out-of-band linearity. ii) The $4G_m$ weakens the effect of R_{sw} to stopband rejection (i.e., β at V_i and $A_{v,LNA}/\gamma$ at V_o), given that R_{sw} is divided by $(1+(V_o/V_i))$ when reflecting back to V_i at the blocker frequencies, where L_p or C_p is considered as a short (Fig. 9.4.3). This feature saves the LO power for a given R_{sw}. The filtering effect at V_i is, to the first order, irrelevant to R_{sw}, and goes up with G_m that should be high for low NF. iii) Given an LNA's BW_{-3dB}, a smaller C_p is allowed due to the boosting factor $1+2A_{v,LNA}$, when referring to V_i. For instance, $A_{v,LNA}$=10 V/V can boost the effective C_p by ~20x.

The LNA's in-band input impedance (R_{in}) is $\sim[(R_F/4)//R_p]/4G_mR_L$ at L_pC_p resonance. Unlike the traditional R_F-feedback-only inverter-based LNA [6] that suffers from a tight tradeoff between S_{11} and NF, here R_p offers a freedom for input matching while contributing negligible noise (R_p is the equivalent resistance of the 4-path SC network).

A VCO filter is tailored for current reuse even at 0.5V (Fig. 9.4.4). The loss in the LC-tank of the VCO is compensated by a negative transconductor ($-G_{mT}$) pieced together from T number of M_v cells, i.e., $G_{mT}=T(4g_{mv})$, where g_{mv} is from M_v. The aim is to distribute the bias current of the VCO to all BB gain stages (A_1, A_2… A_{18}) that implement the filter. For the VCO, M_v operates at $2f_{LO}$ or $4f_{LO}$ for dividing out a 4-phase LO at f_{LO}. Thus, the VCO signal leaked to the source nodes of M_v ($V_{F1,I+}$, $V_{F1,I-}$) is pushed to very high frequencies ($4f_{LO}$ or $8f_{LO}$) and can be easily filtered by BB capacitors. For the filter's gain stages such as A_1, M_b (g_{mb}) is loaded by an impedance of $\sim 1/2g_{mv}$ when L_p is considered as a short at BB. Thus, A_1 has a ratio-based voltage gain of roughly g_{mb}/g_{mv}, or as given by $4Tg_{mb}/G_{mT}$. The latter shows how the distribution factor T can enlarge the BB gain, but is a tradeoff with its input-referred noise and can add more layout parasitics to $V_{VCOp,n}$ (i.e., narrower VCO's tuning range). The –R cell added at $V_{F1,I+}$ and $V_{F1,I-}$ boosts the BB gain without loss of voltage headroom. For the BB complex poles, $A_{2,5}$ and C_{f1} determine the real part while $A_{3,6}$ and C_{f1} yield the imaginary part. There are 3 similar stages cascaded for higher channel selectivity and image rejection ratio (IRR). R_{blk} and C_{blk} were added to avoid the large input capacitance of $A_{1,4}$ from degrading the gain of the front-end.

The receiver was fabricated in 65nm CMOS. Measurements (Fig. 9.4.5) showed that the gain (50±2dB), NF (8.1±0.6dB) and IRR (20.5±0.5dB) are stable over the four ISM bands. A two-tone test at [f_{LO}+12MHz, f_{LO}+22MHz] shows an $IIP3_{out\text{-}of\text{-}band}$ of –20.5±1.5dBm. All S_{11} are <–8dB and the VCO phase noise is –117.4±1.7dBc/Hz at 3.5MHz offset. Owing to the merged VCO filter, the BB signal should be <50mV_{pp} for not degrading the phase noise by 1dB. The 2MHz-IF gain response shows 18/38dB rejection at the adjacent/alternate channel. Other results (not shown) are the out-of-band P_{1dB} (–20dBm), and blocker-NF (13.7dB) for a single-tone blocker of –20dBm applied at 50MHz offset from the 860MHz RF. This blocker resilience is reasonably high for 1.15mW receiver power at 0.5V.

Benchmarking with the recent art [1,3,7] in Fig. 9.4.6, this work succeeds in covering multi-ISM bands with LO-defined input matching and RF filtering, while advancing the power and area efficiencies with zero external components. Figure 9.4.7 shows the die micrograph of the receiver.

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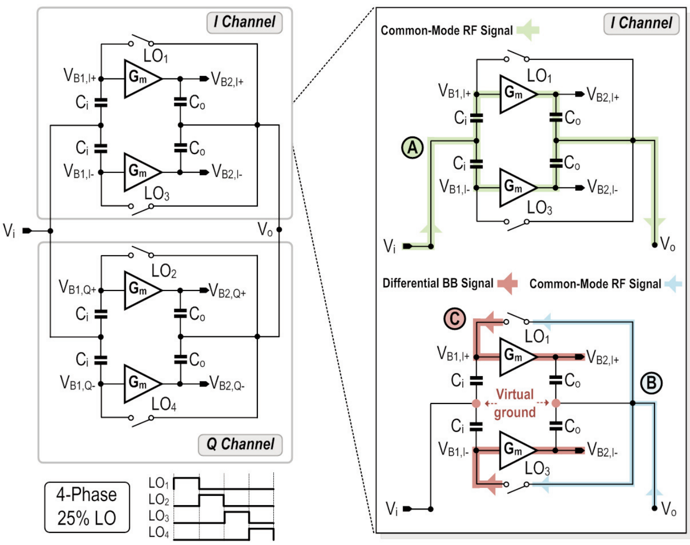

Figure 9.4.1: Proposed RF-to-BB-recycled front-end.

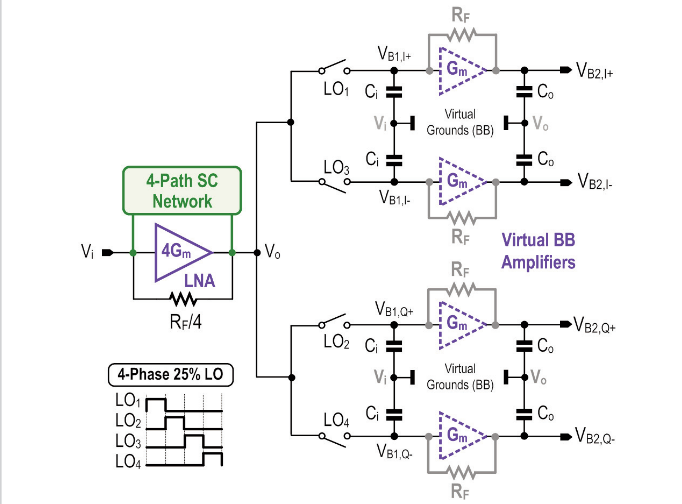

Figure 9.4.2: Functional view of the RF-to-BB-recycled front-end. The memory effects of C_i and C_o associated with the 4-path SC network are detailed in Fig. 9.4.3.

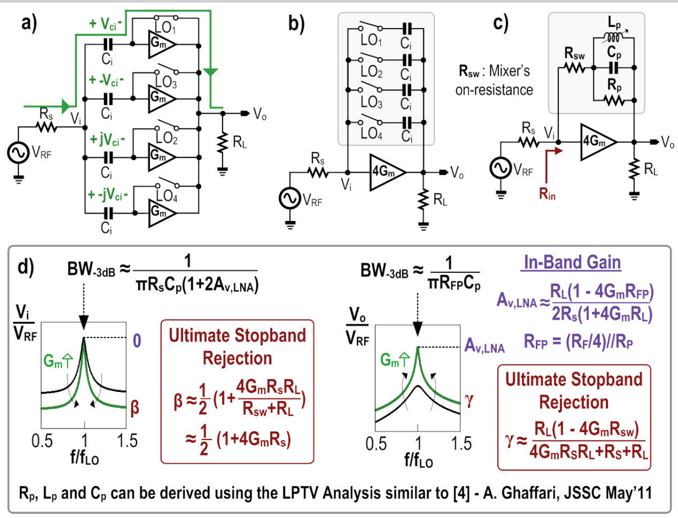

Figure 9.4.3: a) An equivalent 4-path tunable LNA embedded inside the front-end. a) and b) are mathematically equivalent and modeled as c). d) The filtering profiles of c).

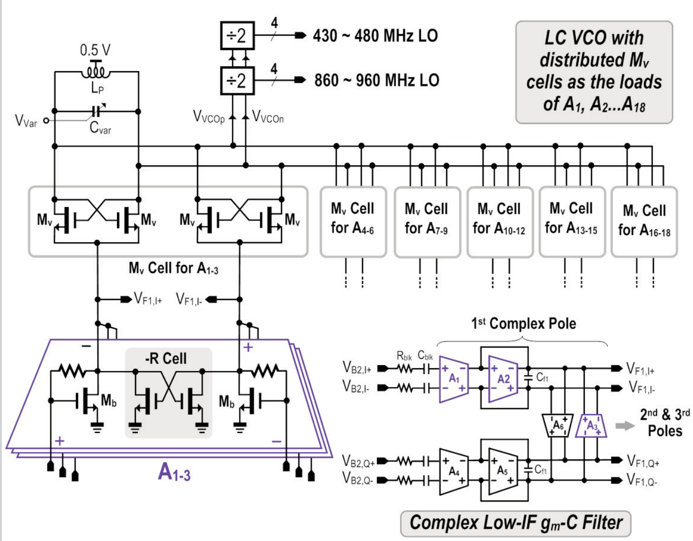

Figure 9.4.4: 0.5V current-reuse VCO filter and LO generation.

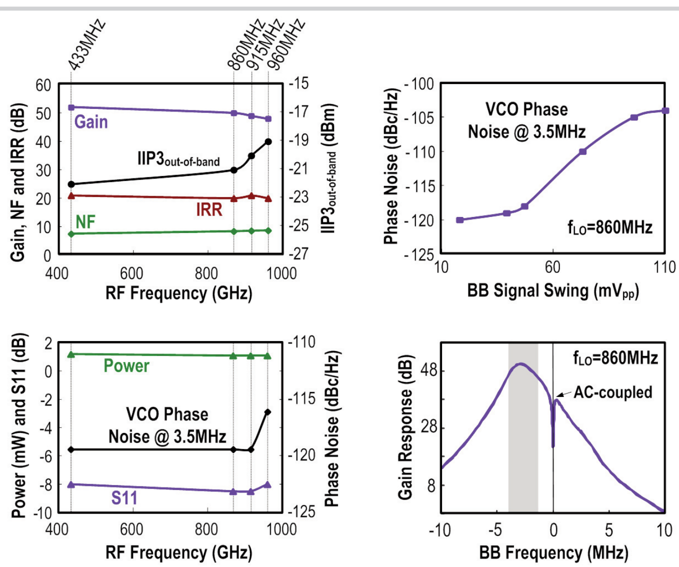

Figure 9.4.5: Measured key performance metrics.

	This Work	ISSCC'13 [1] (w/ VCO)	ISSCC'13 [3]	JSSC'10 [7]
Application	433/860/915/960 MHz (ZigBee/IEEE802.15.4c/d)	2.4 GHz (ZigBee/ IEEE 802.15.4)	2.4 GHz (Energy Harvesting)	2.4 GHz (ZigBee/ IEEE 802.15.4)
Architecture	RF-to-BB-Recycled Front-End + N-path Tunable LNA + Current-Reuse VCO-Filter	Blixer + Hybrid Filter + Passive RC-CR Filter + LC VCO	CG LNA + Passive Mixers + N-Path SC IF Filter + LC VCO	LNA-Mixer-VCO Merged Cell + Complex Filter
BB Filter	3 complex poles	1 Biquad, 4 complex poles	2 real poles	3 complex poles
Input Matching Technique	On-chip N-path SC (tunable by LO, high Q)	On-chip LC (fixed, low Q)	Off-chip LC (fixed, low Q)	Off-chip LC (fixed, high Q)
External Components	zero	zero	2 caps, 1 inductor	1 caps, 1 inductor
Input Matching BW and Tunability	433 to 960 MHz (tunable by LO)	2.25 to 3.55 GHz (fixed)	~ 2 to 2.6 GHz (fixed)	2.3 to 2.6 GHz (fixed)
Active Area (mm²)	0.2	0.3	2.5	0.35
Power (mW) @V_{DD}	1.15 ± 0.05 @ 0.5 V	2.7 @ 0.6/1.2 V	1.6 @ 0.3 V	3.6 @ 1.2 V
Gain (dB)	50 ± 2	55	83	75
NF (dB)	8.1 ± 0.6	9 [spec.: 15.5]	6.1	9
$IIP3_{out\text{-}of\text{-}band}$ (dBm)	−20.5 ±1.5	−6 [spec.: −32]	−21.5	−12.5
IRR (dB)	20.5 ± 0.5	28 [spec.: 4]	N/A	35
VCO Phase Noise (dBc/Hz)	−117.4 ± 1.7 @ 3.5 MHz	−115 @ 3.5 MHz [spec.: −102]	−112 @ 1 MHz	−116 @ 3.5 MHz
Technology	65 nm CMOS	65 nm CMOS	65 nm CMOS	90 nm CMOS

Figure 9.4.6: Chip summary and benchmark with the state-of-the-art.

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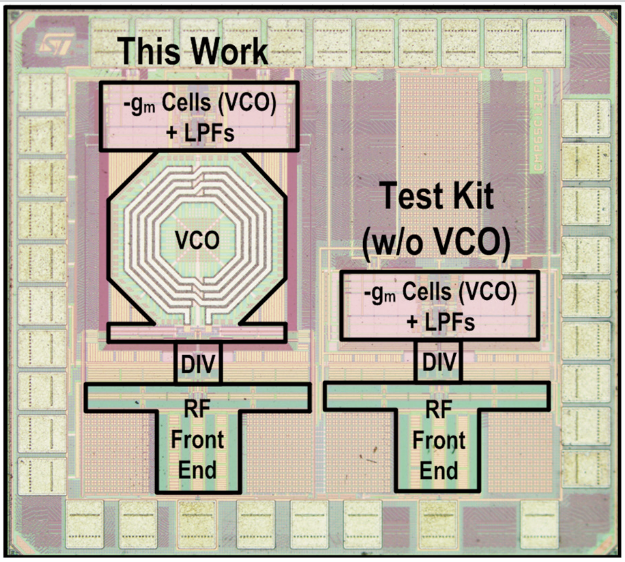

Figure 9.4.7: Die micrograph of the fabricated receiver.