MULTISTANDARD-COMPLIANT RECEIVER ARCHITECTURE WITH LOW-VOLTAGE IMPLEMENTATION

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ABSTRACT

Multistandard-compliant wireless transceivers with low-voltage low-power implementation are in great demand to match the proliferation of multiple WLANs and the continuous scaling of CMOS technologies. This paper proposes both the architecture and the corresponding circuit techniques to implement a low-IF/zero-IF reconfigurable receiver IF-to-baseband chip for IEEE 802.11a/b/g WLAN. Optimum low-voltage circuit techniques enabled a successful operation at 1 V in 0.35-µm CMOS.

1. INTRODUCTION

IEEE 802.11a, b and g are the three prominent WLAN standards currently under exploitation. Dissimilarity in their physical layer (PHY), regrettably, obstructs the systems from reaching the sought features of high-level of integration, multistandard compliance, low voltage and low power. This paper describes an unprecedented 1-V receiver design for 802.11a/b/g WLAN. Implemented in 0.35-µm CMOS, the cost is only 14% of the 90-nm CMOS, but with a significant loss in voltage headroom [Fig. 1(a)]. Also, such a design simulates well the situation that will happen when the technologies are scaled down to 22nm-18nm CMOS [Fig. 1(b)]. Thus, the developed low-voltage technique will be continuing useful. Such a target, in conjunction with the scope of multistandard compliance, makes the design and implementation techniques very different from the other WLAN solutions using standard supply [1]-[3].

2. DESIGN CONSIDERATIONS AND ARCHITECTURE

Briefly, 802.11b is a wideband and spread-spectrum standard, direct conversion (or namely, zero-IF) is the most efficient way once the low-frequency disturbance (DC offset and flicker noise) is eliminated, for instance, by AC-coupling. Conversely, although 802.11a and g are wideband also, the OFDM technique will turn the removal of the low-frequency disturbance by notch filtering very problematic, since a slight frequency deviation in the frequency synthesizer will place the notch on the channel sub-carriers rather than

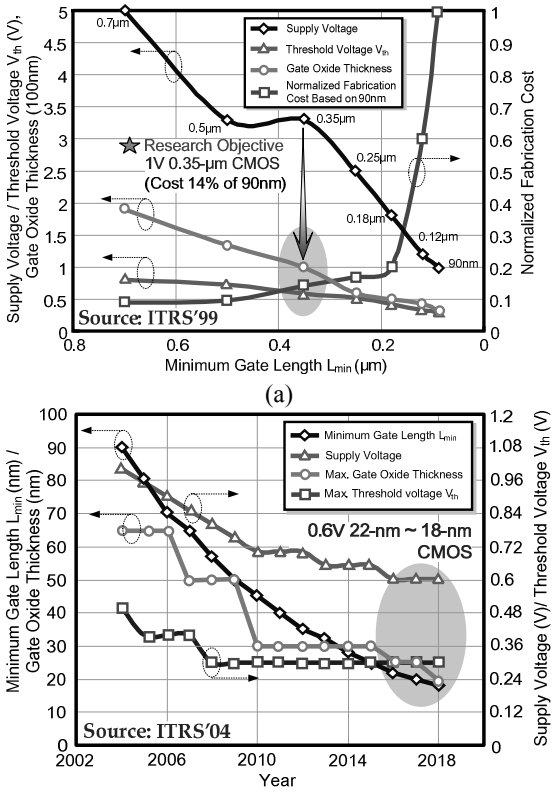

Fig. 1: Scaling of CMOS - (a) From microscale to 90 nm, (b) From 90 nm to 18 nm.

eliminating the unwanted low-frequency disturbance [4]. To alleviate the problem, a low-IF architecture with a half-channel-spacing IF can be used for both 802.11a and g, since the image is now the first adjacent channel that is only at the maximum 16 dB larger than the desired channel. Such an architectural consideration motivates the investigation of a low-IF/zero-IF reconfigurable receiver [5]-[6], as depicted in Fig. 2. One more channel selection is added in the IF to cooperate with the frequency synthesizer, such that low-IF/zero-IF reconfiguration becomes simple, and at the same time relaxes the frequency synthesizer design specifications.

The two frequency bands, 2.4 GHz and 5 GHz, require two sets of low-noise amplifiers (LNAs) and

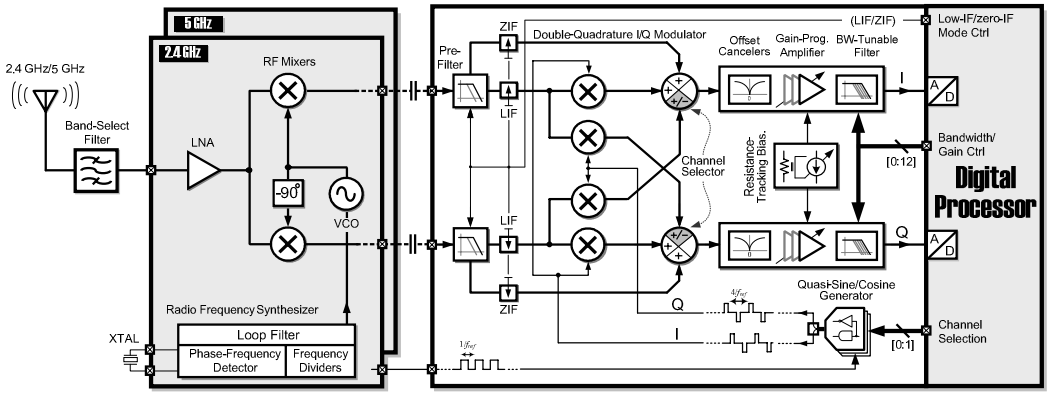

Fig. 2: Proposed low-IF/zero-IF reconfigurable receiver architecture.

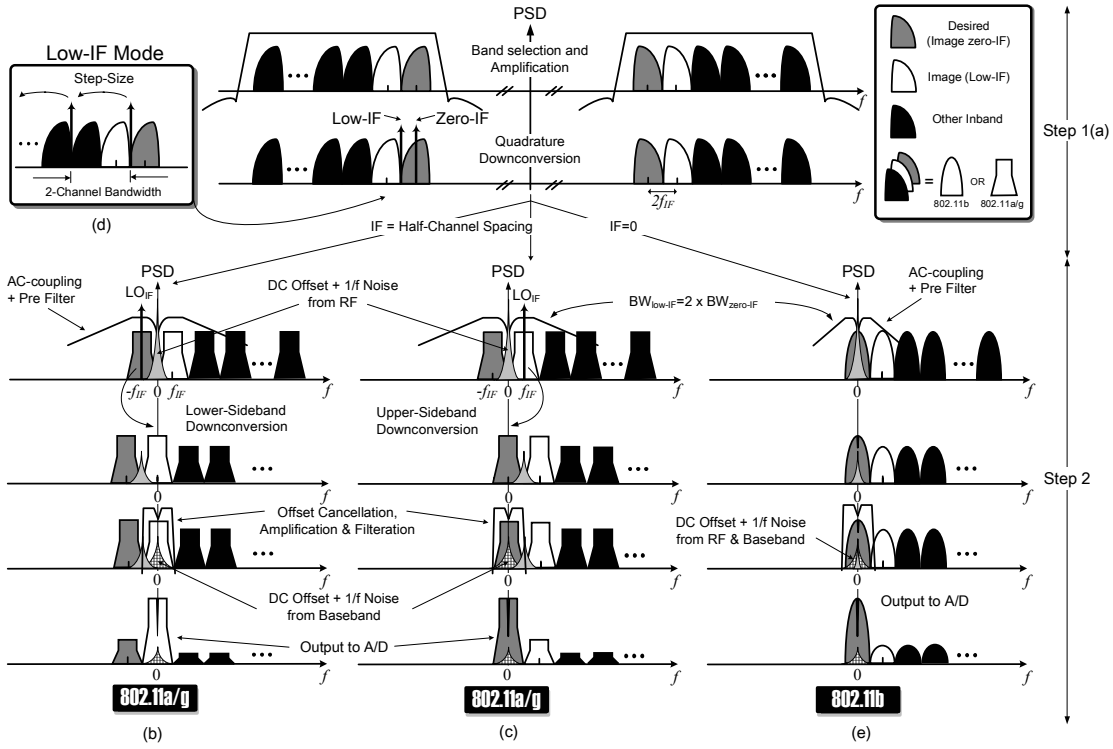

Fig. 3: Spectra-flow illustrations - (a) Step-1: RF-to-IF downconversion for 802.11a/b/g. (b) Step-2: IF-to-baseband lower-sideband downconversion. (c) Step-2: IF-to-baseband upper-sideband downconversion. (d) Low-IF channel-selection scenario at RF. (e) Step-2: zero-IF mode.

RF mixers for amplification and RF-to-IF downconversion, respectively. The pre-filter and double-quadrature *I/Q* modulator offer two modes: filtering and downconversion in low-IF mode, or simply filtering with a halved bandwidth in zero-IF mode. The modulator not only performs IF-to-baseband downconversion and image rejection, but also serves as an IF channel selector. The IF modulation signals are generated by a quasi-sine/cosine generator, which alters the phase of the sine's one between 0° or 180° for transparent selection of the channel in the control path. The bandwidth (BW)-tunable filter purifies the channels of 802.11a/b/g with different cutoff frequencies, and the programmable-gain amplifier (PGA) optimizes the signal swing to full-scale for the A/D conversion. DC-offset cancelers are embedded in the filter and PGA to suppress the 1/*f* noise and DC offset. The digital processor controls the operating modes, the channel selection, the gain and the BW.

3. Operating Principles

3.1 Low-IF Mode

Figure 3(a)-(c) describes the operation in low-IF mode pictorially [6]. For the 5-GHz 802.11a or the 2.4-GHz 802.11g, after amplification by the LNA, the

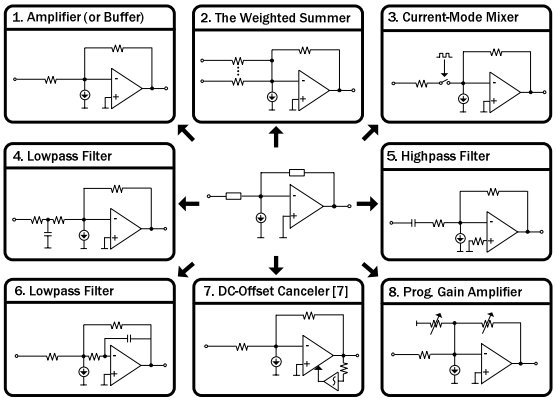

Fig. 4: Opamp-based functions in inverting configuration.

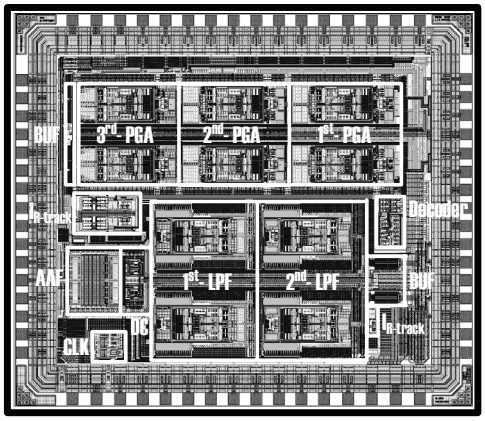

Fig. 5: Chip Layout.

desired channel and its image will be downconverted together to an identical IF (which is half-channel spacing) but with a complex-conjugate representation [Fig. 3(a)]. The low-frequency disturbance, located in between the desired signal and its image can be comfortably cancelled by using AC-coupling, while the high-side injected image can be suppressed by the pre-filter. The double-quadrature I/Q modulator can flexibly select either of them from IF to baseband without the need of a frequency synthesizer. Thus, a channel selection is accomplished between the desired channel and its image at IF, without any prerequisite in the radio-frequency range [Fig. 3(a)-(c)]. In the following BW-tunable filter and PGA, the DC-offset cancellation is possible because the OFDM channel has no sub-carrier at DC and the IF-to-baseband down-conversion imposes very small frequency error. In addition, this coarse-at-radio fine-at-baseband channel selection method provides many advantageous features to the frequency synthesizer that can be described as follows:

First, the step-size of the frequency synthesizer can be doubled [Fig. 3(d)], which implies that the division ratio in the phase locked-loop (PLL) will be halved since the finally selection is done at the IF. For an integer-*N* frequency synthesizer, a larger step-size implies a higher reference frequency can be utilized. Thus, the loop bandwidth of the PLL is also enlarged by the same factor to shorten the PLL settling time and reduce the phase noise from the local oscillator, without the stability and overshoot penalties. Moreover, a higher reference frequency reduces the division ratio in the modulus, so as the phase noise contributed by the reference frequency. Furthermore, fewer locking positions also simplify the modulus anatomy, thereby enhancing the channel selection speed.

3.2 Zero-IF Mode

For the 802.11b, direct downconversion is preferred [Fig. 3(e)] [6] since DC-offset cancellation with a cutoff-frequency less than 10 kHz generates an insignificant intersymbol interference (ISI). The bandwidth of the pre-filter is correspondingly reduced by a factor of 2, and the double-quadrature I/Q modulator would be bypassed. The following operations that include DC-offset cancellation, filtering and amplification are all analogous to those presented in the low-IF mode.

4. Low-Voltage Circuit Techniques

Several baseband functions, such as amplification, filtering and IF mixing, can be built by using low-voltage OpAmps in inverting configuration. Fig. 4 shows 8 of these functions that can be super-positioned all together to form a multifunctional block with a single OpAmp. No input swing is required from the OpAmp while rail-to-rail output swing is deliverable. The DC level of the virtual ground is biased to 0.1 V for a simple NMOS switch to function, while keeping a value of overdrive voltage that would be enough for the current source to function. Such a series of low-voltage circuitry has been extensively utilized in the implemented system. Also, detailed descriptions of the techniques adopted in the design of the PGA and the DC-offset canceler are addressed in [7].

5. Simulation Results

The layout of the chip that was fabricated in 0.35-μm CMOS is shown in Fig. 5. Figures 6(a)-(d) depict its post-layout simulation results. The output passband noise density is ~10 μV/Hz, while the flicker noise is suppressed by more than 32 dB by the DC-offset canceler [Fig. 6(a)]. Because of the constant-feedback-factor characteristic of the programmable-gain amplifiers [7], the lower and upper -3dB points remain practically constant at all gain levels [Fig. 6(b)]. The robustness of the chip is demonstrated in a 100-time AC Monte-Carlo simulation [Fig. 6(c)], and no dangerous yield is observed. The spurious free dynamic range (SFDR) is 46 dB with an output swing of 0.98-V_{pp} [Fig. 6(d)]. The power consumption is ~30 mW.

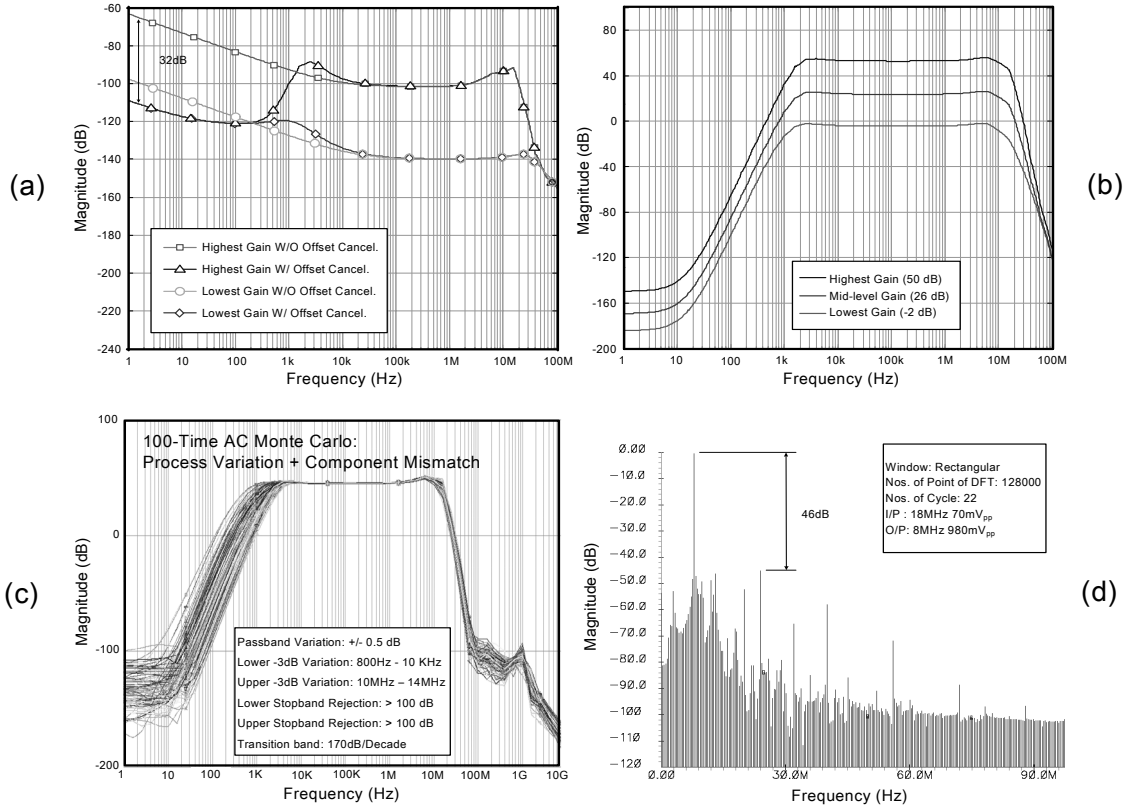

Fig. 6: Post-layout simulation results - (a) Output noise (zero-IF). (b) AC response (zero-IF). (c) Monte-Carlo AC responses (zero-IF). (d) FFT response (low-IF).

6. CONCLUSIONS

This paper presented innovative design techniques to realize an IEEE 802.11a/b/g-compliant receiver with reconfiguration only necessary in the IF-to-baseband part. The multistandard compliance was enabled by the two-step channel-selection technique, which helped to synthesize the low-IF and zero-IF modes in a single path, while simultaneously providing an extra benefit in terms of relaxation of the frequency synthesizer design specifications. Low-voltage operation is achieved with the contribution of different OpAmp-based inverting configuration circuits that implement the baseband functions, which include the filtering, frequency down-conversion, DC-offset cancellation and gain-controllable amplification.

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