A 10b 1.6GS/s 12.2mW 7/8-way Split Time-interleaved SAR ADC with Digital Background Mismatch Calibration

Mingqiang Guo, Jiaji Mao, Sai-Weng Sin, Hegong Wei[1], R. P. Martins[2]
State-Key Laboratory of Analog and Mixed Signal VLSI, Dept. of ECE, FST, University of Macau, Macao
[1]University of Texas at Austin, Austin
[2]On leave from Instituto Superior Técnico, Universidade de Lisboa, Portugal

***Abstract*—This paper presents a split time-interleaved (TI) successive-approximation register (SAR) analog-to-digital converter (ADC) with digital background mismatch calibration. Benefitting from the proposed split TI topology, the mismatch calibration convergence speed is fast without any extra analog circuits. A prototype 10-b 1.6-GS/s 7/8- way split TI-SAR ADC in 28-nm CMOS achieves 54.2dB SNDR at Nyquist rate with a 2.5-GHz 3-dB bandwidth, while the power consumption is 12.2mW leading to a Walden FOM of 18.2 fJ per conversion step.**

Keywords— SAR analog-to-digital converter (ADC), time-interleaved (TI) ADC, timing-skew calibration, split ADC, background mismatch calibration.

I. Introduction

The time-interleaved (TI) ADC architecture is the popular choice for wide-band applications, but it suffers from the offset, gain, and timing mismatches between each sub-converters. The use of reference channel is one of the efficient way to calibrate the mismatch error in the background. However, additional reference ADC replicas [1] can substantially increase power and hardware overhead, or alternating the reference ADC with a single comparator [2] makes the convergence speed quite slow. Moreover, the alternatingly reference channel will produce extra spurs by changing the overall TI ADC's input impedance periodically [3-4].

This paper describes a split time-interleaved ADC architecture with digital background mismatch calibration. First, each sub-converter of the split part can be considered as the reference by the other part. Therefore, a fast mismatch convergence can be achieved without the use of an extra reference converter [1][4] or a comparator [2][3]. Second, the ADC's input impedance remains constant because there are two sub-converter sampling in every sample, simultaneously, and no spurs arise from impedance variations. All the offset, gain and timing mismatches can be calibrated in the background using the proposed method. To verify the proposed architecture, we implemented a prototype 10-b 1.6-GS/s 7/8-way TI a ADC in 28-nm CMOS.

Section II introduces the proposed time-interleaved architecture and the digital background mismatch calibration based on this topology. Section III presents the ADC implementation, including the architecture and the phase generator circuitry. Section IV summarizes the experimental results of the prototype split TI-SAR ADC.

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II. Split Time-interleaved ADC

A. The proposed Split TI ADC Architecture

Fig. 1 shows the proposed TI ADC split into two parts, part A and B, with the same overall sampling rate (f_s) but different number of channels M and N, respectively. Similar to the split non-interleaved ADCs, we obtained the final output by the average of the two split parts, to reduce the requirements of SNR for each split part by half when compared with the regular TI-ADC. To keep one of the sub-converter ADC_A as the reference of the ADC_B, the M and N must be mutual prime numbers. Also, M and N=M+1 are an excellent choice to simplify the implementation of the sub-converter (In this work, ADCA and ADCB are identical but with different sampling rate).

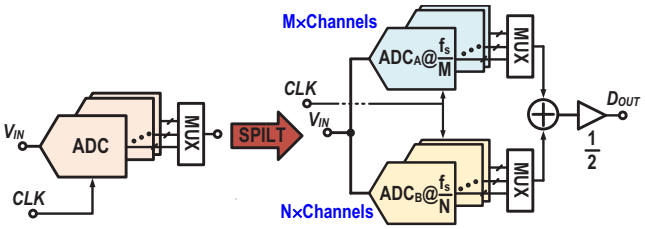

Fig. 1. The conceptual idea of the proposed split TI ADC architecture.

Fig. 2 shows an illustrative example of 3/4-way split TI-SAR with the proposed architecture; it consists of 4 SAR ADC_A working at $f_s/4$ and 3 SAR ADC_B working at $f_s/3$, respectively. Each of the 4 ADC_A and the 3 ADC_B samples the input signal V_{in} at the falling edge of its sampling clock (ϕ_{A1}~ϕ_{A4}, ϕ_{B1}~ϕ_{B3}).

As the timing diagram of Fig. 2 illustrates, the sampling clock of ADC_{A1} and ADC_{B1} will meet with each other after every 12 clock cycles and it can serve as the implicit timing reference for the mismatch calibration. Similarly, every sub-converter of ADC_A can periodically compare the sampling instant with that of the ADC_B (like ADC_{B1}). It enables the background calibration based on a least mean square (LMS) algorithm, viewing the output of the ADC_{B1} as the reference signal to calibrate the mismatch error of ADC_A. We apply the same principle simultaneously applied to ADC_B to calibrate its

mismatch error. There are always two sub-converters (one in ADC_A and another in ADC_B) sampling in every cycle simultaneously, imposing a constant ADC input impedance.

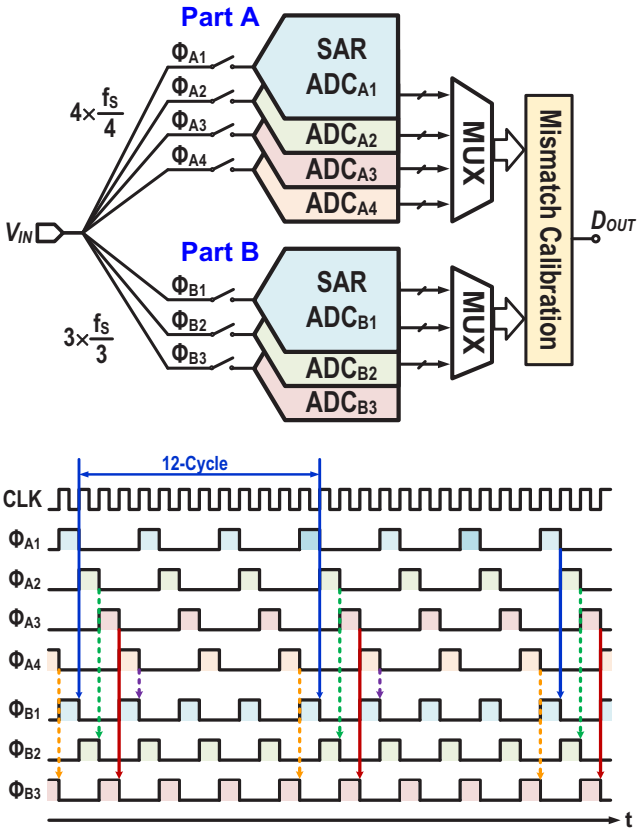

Fig. 2. Architecture and timing diagram of the proposed 3/4-way TI-Split-ADC.

B. *Digital Background Mismatch Calibration*

Fig. 3 shows the principles of the digital background mismatch calibration, with the operation of the mismatch calibration for both ADC_A and ADC_B is done synchronously and independently. Fig. 3(a) exhibits the ADC_{B1} (one of the unit converters of ADC_B) chosen as the reference to calibrate all the sub-channels in ADC_A. The goal of the calibration algorithm is to determine the mismatch factors of all interleaved channels of ADC_A equal to those of the reference channel ADC_{B1}. The $D_{A,out,raw}$ ($4\times f_s/4$) and $D_{B,out,raw}$ ($3\times f_s/3$) represent the raw outputs from ADC_A and ADC_B. ADC_{B1} will meet each sub-channels of ADC_A every 12 cycles (Fig. 2). Therefore, we use a multiplexer ($4\times f_s/12$) to choose the output $D_{A,out}$ ($f_s/3$) which corresponds to the output of ADC_A after mismatch correction. Then, it obtains the current conversion error *e* defined as the difference of the outputs between the unit converter of ADC_A ($D_{A,out}$) and the corresponding one from ADC_{B1} ($D_{B1,out,raw}$). The LMS search block updates the coefficient of mismatch factors effectively minimizing the difference *e* [1]. Fig. 3(b) shows the calibration case in part B, which is similar to part A in Fig. 3(a), with factors "3" and "4" interchanged as shown.

All kinds of mismatches including offset, gain, and timing-skew among every sub-converter can be calibrated, as well, by the principles of Fig. 3. Since timing calibration is much more complex than offset and gain, here we briefly discuss the case of timing-mismatch calibration algorithm.

The new data $D_{A,out}$ and $D_{B,out}$ after mismatch calibration is,:

$$D_{out} = D_{out,raw} - \frac{dV_{in}(t)}{dt} \cdot \Delta t \qquad (1)$$

where the $dV_{in}(t)/dt$ is the derivative of the input, and the Δt is the timing skew error. With the help of a Hilbert transform filter and a scaling factor, it can compute the derivative of the input in any Nyquist Band (NB) [5] by the digital FIR filter in Fig. 4.

Since Δt is not known in advance, it has to be estimated with the LMS algorithm by the digital accumulators (Acc) with update the equation [6],

$$\Delta t^{(new)} = \Delta t^{(old)} + \mu \cdot \frac{dV_{in}(t)}{dt} \cdot e \qquad (2)$$

where the step size μ controls the convergence speed and accuracy of the LMS search.

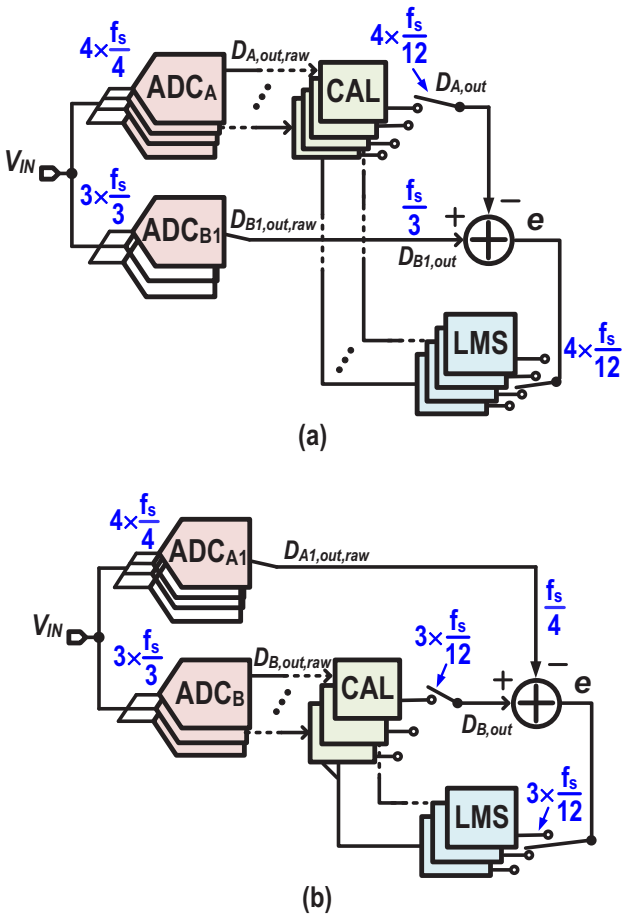

Fig. 3. Principles of the digital background mismatch calibration: (a) Part A; (b) Part B.

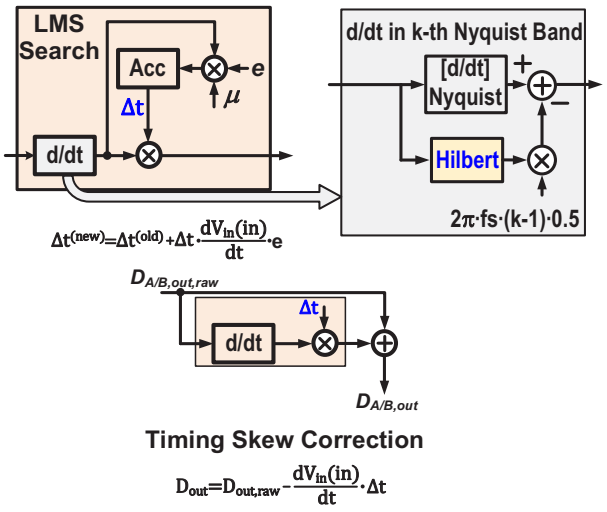

Fig. 4. Timing mismatch calibration.

III. ADC Implementation

A. 7/8 Way Split TI-SAR ADC

Fig. 5 illustrates how we implemented the overall 7/8-way 10-bit TI-SAR ADC to verify the proposed split-TI-ADC. It consists of 2 parts A and B, with TI sub-channels A1-A8 (8×200MS/s SAR) and B1-B7 (7×228MS/s SAR), respectively. The master clock $CLK_{1.6G}$ (ground-shielded from the signal) routed in a tree structure adjacent to the signal trace reduces the clock skews between ADCs.

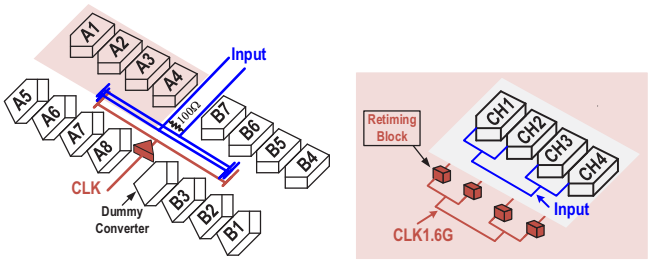

Fig. 5. Block diagram of the 7/8-way split TI-SAR ADC.

B. Phase Generator

A low jitter and skew multi-phase clock is key to achieve high SNDR at high frequencies. Fig. 6 presents the phase generator where a 1.6 GHz master clock, divided by 8-cycle or 7-cycle ring counters, generates the outputs Q_{A1}-Q_{A8} and Q_{B1}-Q_{B7} with duty cycles with of 12.5% or 14.3%, respectively. The clock chain contributes with a substantial number of phase jitters and mismatches. We can suppress these effects through the use of a retiming technique [7]. The falling edge of the master clock of $CLK_{1.6G}$ now defines the sampling points created by Φ_{A1}-Φ_{A8} and Φ_{B1}-Φ_{B7}, suppressing the above jitter and mismatch components. From the post-layout simulation, the total extracted jitter of each sampling edge (Φ_{A1}-Φ_{A8} and Φ_{B1}-Φ_{B7}) is close to 70fs rms, dominated by the global clock buffer, and the total power consumption of the phase generator is only 2.3-mW.

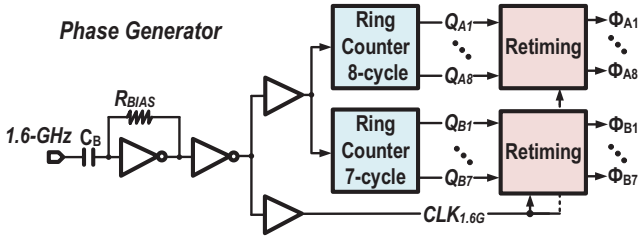

Fig. 6. Phase Generation.

IV. Measurement Results

The prototype 7/8 way split TI-SAR ADC fabricated in 28nm CMOS and occupies a core area of 370×210μm^2, with the chip microphotograph exhibited in Fig. 7 and the digital background mismatch calibrations off-chip. The digital supply of the SAR logic is 0.8V while the analog supply of the clock generator, comparator, and DAC switches are 0.9V to obtain sufficient linearity and low-jitter of the input sampling. The single-ended input capacitance is 180fF.

Fig. 8 plots the measured DNL and INL at 1.6GS/s with a 760MHz input, indicating a maximum of 0.22 LSB for the former and 0.51 LSB for the latter. Fig. 9 shows the measured SNDR with a 2.52GHz input at 1.6GS/s during convergence of skew calibration. The proposed calibration method improves the SNDR from 47 to 51.3dB. Fig. 10 presents the measured dynamic performance at 1.6GS/s indicating an SNDR of 54.2dB and an SFDR of 67.1dB with a 760-MHz input signal, and the SNDR of 51.3 dB and the SFDR of 63.5dB at a 2.52GHz input.

Fig. 11(a) shows the dynamic performance versus sampling rate with a 760-MHz input signal. The SNDR exhibits a 3dB variation from 0.7 to 2.5GHz input frequency with a sampling rate of 1.6GS/s (Fig. 10(b)). Table I shows the performance summary and a comparison with similar state-of-the-art TI-ADCs. The ADC consumes 12.2mW at 1.6GS/s reaching a Walden FOM of 18.2fJ/conv-step and Schreier FOM of 162.4dB at Nyquist.

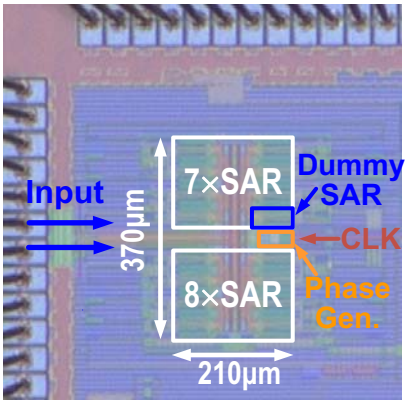

Fig. 7. Chip microphotograph.

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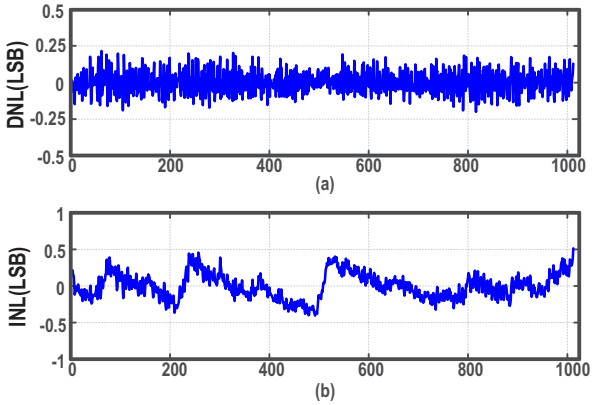

Fig. 8. Measured DNL and INL at 1.6GS/s with a 760MHz input.

TABLE I. PERFORMANCE SUMMARY

	ISSCC-15 H. K. Hong	ISSCC-15 B. Sung	ISSCC-16 C.Y. Lin	VLSI-16 Y.C. Lien	VLSI-17 Lei Luo	This Work
Technology	45nm	45nm	40nm	16nm	16nm	28nm
Architecture	TI-SAR	TI-FATI	TI-SAR	TI-SAR	TI-SAR	TI-SAR
Resolution(bit)	10	10	10	10	10	10
Speed(GS/s)	1.7	1.6	2.6	1.6	2.0	1.6
Supply(V)	1.2	1.1	0.95	1.1	0.85/1.5	0.9/0.8
Power(mw)	15.4	17.3	18.4	9.8	10.4	12.2
Area(mm^2)	0.057	0.36	0.825	0.023	0.014	0.073
SFDR@Nyq.(dB)	62.0	61.2	57.8	61	56	67.1
SNDR@Nyq.(dB)	51.2	56.1	50.6	50.3	50.1	54.2
SNDR@>Nyq.(dB)	NA	NA	NA	NA	NA	51.3@2.52GHz
FOM@Nyq.(fJ)	30.4	21	25.6	19.2	19.9	18.2
FOMS@Nyq.(dB)	158.6	162.8	159.1	160.2	159.9	162.4

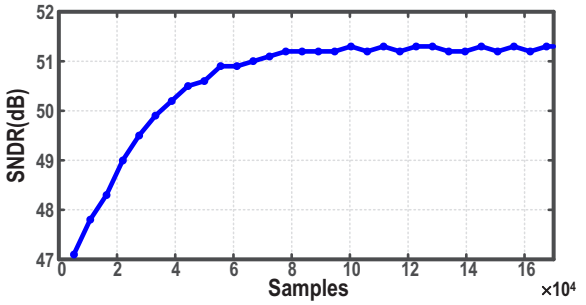

Fig. 9. Measured SNDR with a 2.52GHz input at 1.6GS/s during convergence of timing calibration.

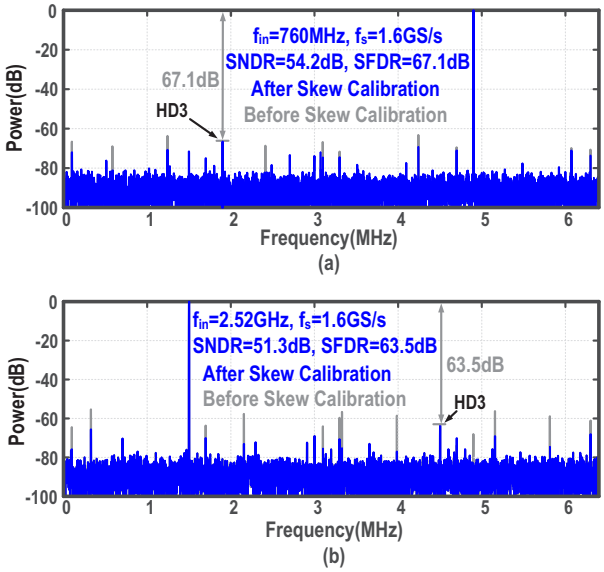

Fig. 10. Measured output spectrum before and after mismatch calibration (decimated by a factor of 125).

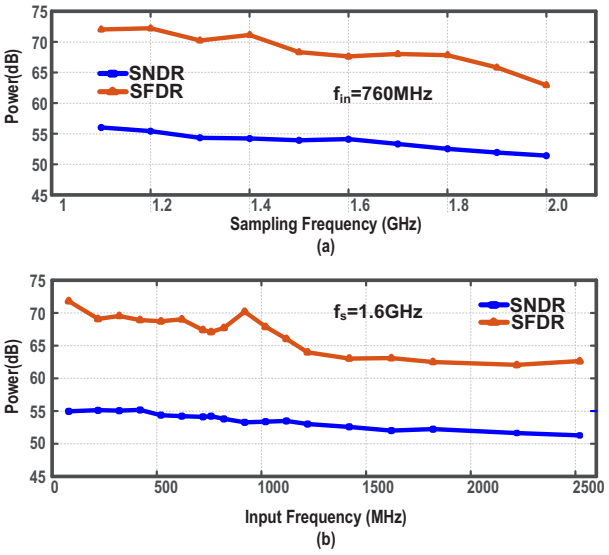

Fig. 11. Measured dynamic performance versus (a) sampling rate and (b) input frequency.