A 22.4μW 80dB SNDR ΣΔ Modulator with Passive Analog adder and SAR Quantizer for EMG Application

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***Abstract*—A Feed-Forward (FF) multi-bit ΣΔ modulator with passive analog adder and 4-bit Successive Approximation (SA) quantizer is presented. The modulator covers the 10KHz bandwidth according to electromyography application. The design utilizes the same DAC array of the SAR quantizer to realize analog summation for the FF signal, which significantly reduces the power dissipation and the silicon area. The modulator operates at 1MS/s with 1V supply. The prototype chip implemented in 65nm CMOS achieves 80dB SNDR and 81dB DR with 22.4μW power consumption. The Figure of Merit (FoM) is 0.13 pJ/conv.-step.**

***Keywords*—ΣΔ modulator, SAR quantizer, passive analog adder**

I. Introduction

In recent years, research in biomedical electronic engineering is becoming more attractive. Yet, the Analog-to-Digital Converter (ADC), as a bridge connecting the analog and the digital domain, is a requisite component for biomedical signal processing. The specifications of the ADCs adopted in main biomedical applications are shown in Fig. 1. Thereinto, electromyography (EMG) has the strictest requirement to the ADC's performance, i.e. relative wide bandwidth and high resolution. The bandwidth for the EMG signal is 10KHz; the A-D conversion precision should be at least 13-bit. Meanwhile, low power and small area are also significant considerations. ΣΔ ADC achieves high resolution with appropriate bandwidth which is a preferred candidate to satisfy the A-D conversion requirements of EMG applications.

In order to achieve a low power design in the ΣΔ ADC, the output signal swing of the op-amps in the ΣΔ modulator should be reduced, to allow the op-amp to be implemented by a single-stage structure. The Feed-Forward (FF) loop topology for the ΣΔ modulator can cancel the signal term at the output of the integrators; and, only quantization noise will be processed in the loop filter path. Hence, this can reduce the output signal amplitude of the integrators. The implementation of the FF loop architecture requires an analog adder in front of the quantizer which is generally implemented using a Switched-Capacitor (SC) amplifier [1]. Passive summation can be adopted to implement it with much less power consumption. However, it will attenuate the summing result;

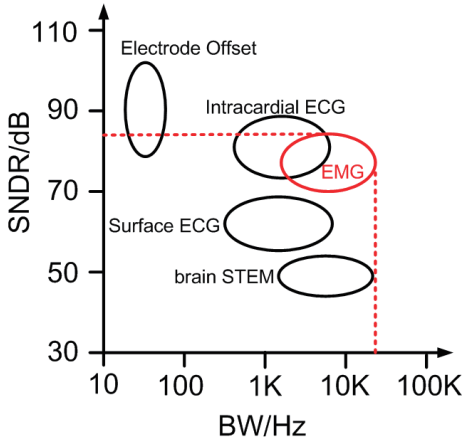

Fig. 1: Specifications of the ADCs in main biomedical applications.

therefore, additional amplification would be needed to restitute the signal swing and to fulfill the quantization range which inevitably consumes extra power [2].

This paper proposes an input FF ΣΔ modulator employing a 4-bit SAR quantizer. The FF summation is realized by a passive analog adder, which is implemented in the DAC array of the SAR quantizer. This design achieves not only ultra-low power, but also minimizes the area and reduces circuit complexity.

II. Input Feed-Forward ΣΔ Modulator with Passive Analog Adder

A. ΣΔ Modulator Architecture

This design employs feed-forward multi-bit topology for low power considerations. Fig. 2 shows the ΣΔ modulator architecture and its timing control diagram. The scheme is composed by two SC integrators and a 4-bit SAR quantizer with feedback Data-Weighted Averaging (DWA). In contrast with the utilization of high order (>3) noise shaping, the system will not suffer from instability with the 2nd order loop filtering. Meanwhile, due to the multi-bit quantization, the ADC's resolution can satisfy the requirements with only 2nd order noise shaping implying that the 2nd order loop filter is

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perfectly adequate for this design. On the other hand, since the multi-bit quantizer is chosen to reduce the quantization error, the feedback D/A Converters (DAC) may suffer from mismatches errors. This fact may degrade the ADC resolution below 80dB. Therefore, the DWA proposed in [3] will be employed to randomize the mismatch error.

Based on the mathematical behavioral modeling of the system, to achieve a SNDR above 80dB, an Oversampling Ratio (OSR) of 50 was chosen. Plus, to guarantee the anticipated resolution, the dc gain of the op-amp must be greater than 30dB, and since the sampling frequency is 1MHz, its GBW was chosen to be at least 5MHz.

B. Passive Analog Adder

Also illustrated in Fig. 2 is the implementation of the input FF that requires an adder in front of the quantizer. To avoid the use of an extra op-amp the summing point can be placed in the digital domain. As a result, extra multi-bit quantizers should be used to convert the signal from analog to digital, thus allowing the FF architecture to relocate its summing point into the digital area [4]. Obviously, this method will impose an additional area to realize the redundant quantizers which will be inappropriate in a small-area design.

Assuming Y as the sum of two signals X_1 and X_2, the relationship between Y and X_i (i=1,2) can also be expressed as:

$$Y = X_1 + X_2 = X_1 - (-X_2) \quad (1)$$

Furthermore, let us assume that the two terminals of the differential output of the 2nd integrator are $V_{int2,n}$ and $V_{int2,p}$, and, $V_{in,n}$ and $V_{in,p}$ symbolize the two input terminals. Besides, $V_{out,n}$ and $V_{out,p}$ exhibit the summation result. Then, the mathematical expression for the summation point before the quantizer is,

$$V_{out,n} = V_{int2,n} + V_{in,n}, V_{out,p} = V_{int2,p} + V_{in,p} \quad (2)$$

Since the differential signals obey the following relationship

$$V_{int2,n} = -V_{int2,p}, V_{in,n} = -V_{in,p} \quad (3)$$

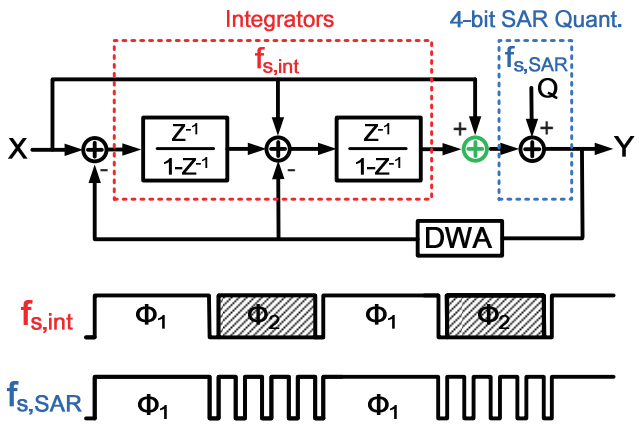

Fig. 2: Overall ΣΔ ADC architecture and its timing diagram.

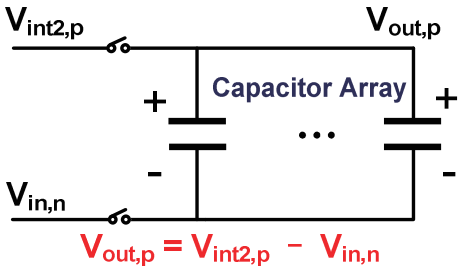

Fig. 3: Passive analog adder based on a capacitor array.

by combining it with (1) and (2) will lead to,

$$V_{out,n} = V_{int2,n} - V_{in,p}, V_{out,p} = V_{int2,p} - V_{in,n} \quad (4)$$

Since in (4) the addition is changed into subtraction, the capacitor can be used to implement it, and this concept is illustrated in Fig. 3. When two signals $V_{int2,p}$ and $V_{in,n}$ charge the capacitor array in each of its sides simultaneously, the residue voltage in the capacitor array is the subtraction of those two signals, leading to an effective signal summation.

The SAR ADC uses the DAC array to sample the input signal, therefore, both sides of the DAC can be utilized to sample the input signals and the integrator output signals, respectively. Applying this method to the SAR quantizer will lead to the summation of the two FF signals. Since this passive analog adder doesn't need extra active circuits it can really save power and area.

C. 4-bit SAR Quantizer - Architecture Considerations

The multi-bit quantizer in the ΣΔ ADC can be realized by a Pipeline [5] or a Two-step [6] ADC. However, these two structures consume more power than a SAR ADC that is a dynamic circuit which consumes relatively lower power when compared with others ADCs. In this work, the 4b SAR quantizer is a self-timed scheme [7] that generates internal higher frequency SAR clocks, using the clock at sampling frequency.

III. Circuit Implementation

A. Op-amp and the loop filter

The op-amp architecture used in this design, presented in Fig. 4 [8], exploits a current starving technique for gain enhancement, and it is chosen based on low-power and matching considerations. However, it does not use feed-forward and multi-bit quantizer topology for the sigma-delta ADC design in [8]. Therefore, the OTA should process large signals, thus needing extra MOS transistors to enhance the slew-rate, which usually results in extra power consumption. But, that will be avoided in the current design. Moreover, the op-amp's gain is larger than 30dB, with a PM > 60^o in each corner simulation, which is fit for the whole system requirements.

Fig. 5 shows the loop filters' topology where DACP<1:15> and DACN<1:15> indicate the feedback DAC control signal. The C1 and C2 represent the unit capacitor in both integrators whose value is 66fF.

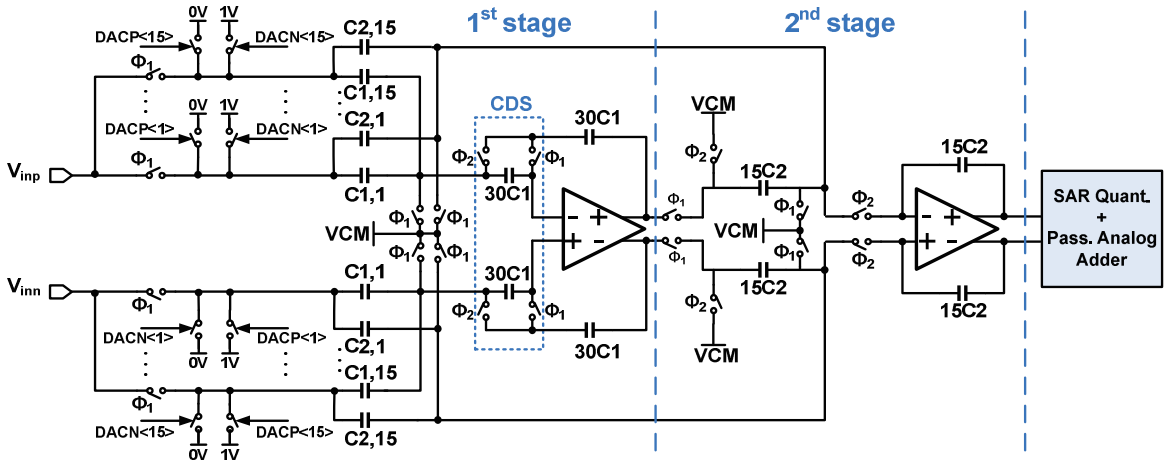

Fig. 5: Loop-filter topology.

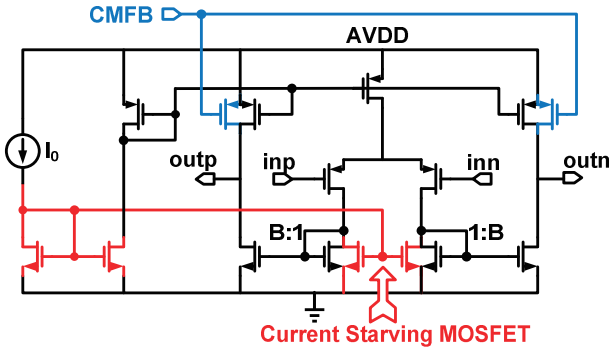

Fig. 4: The architecture of the op-amp.

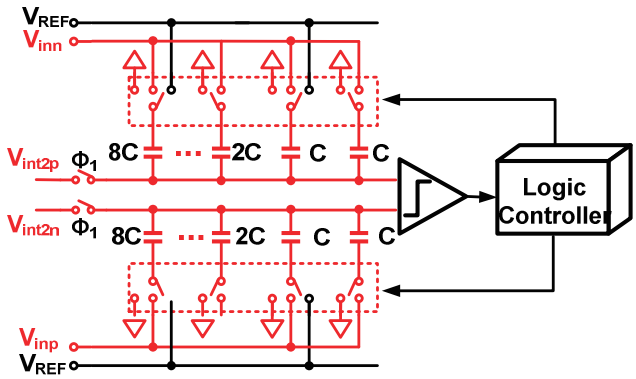

Fig. 6: 4-bit SAR quantizer with the proposed passive analog adder.

B. 4-bit SAR ADC with passive analog adder

As mentioned before, the passive analog adder is built-in together with the DAC of the 4-bit SAR quantizer, as shown in Fig. 6. In the structure, both plates of the DAC capacitor participate in signal sampling. To guarantee the sampling accuracy, the sampling switches are implemented by using a bootstrapped structure to minimize the signal-dependent charge injection errors.

IV. Measurement Results

The proposed biomedical ΣΔ modulator was fabricated in a standard 65nm 1P7M CMOS process with metal-to-metal (MOM) capacitor. Table I summarizes the overall measured performance, with a supply voltage of 1V. The total power consumption is 22.4μW including an analog power of 16.9μW, and a digital power of 5.5μW. The measured peak SNDR achieves around 80dB at 1MHz sampling rate. Table II exhibits a benchmark with related state-of-the-art (similar resolution and bandwidth) of ΣΔ ADCs. The FoM of this work has a relative advantage over other designs.

Fig. 7 shows the measured Power Spectral Density (PSD) of the ΣΔ modulator which indicates a peak SNDR of 79.6dB. The test input signal is at 470Hz which allows containing the in-band harmonics up to the 10th order. Besides, due to the feedback DWA, harmonic distortion does not impose any performance issue in this design. The measured modulator's Dynamic Range (DR) achieves 81dB, as illustrated in Fig. 8. Fig. 9 shows the die photograph, where the active core area is 0.133mm^2.

V. Conclusions

An ultra-low power biomedical ΣΔ modulator for EMG applications employing FF loop topology and multi-bit quantization has been presented. A passive analog adder implemented by utilizing the DAC of the 4-bit SAR quantizer has also been proposed to accomplish the summation of the FF input signal. The high frequency control signal for the 4-bit SA quantizer is generated on-chip based on the modulator's sampling clock. The prototype chip was implemented in 65nm CMOS technology, which achieves 10kHz bandwidth and 80dB SNDR, consuming 22.4μW of power at 1V supply. The FoM of the ΣΔ modulator is as low as 0.13pJ/conv. –step.

Acknowledgment

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TABLE I. MEASURED PERFORMANCE SUMMARY

Process	65nm CMOS
Supply	1V
Signal Bandwidth	10KHz
OSR	50
Sampling Frequency	1MHz
Peak SNDR	80dB
Dynamic Range	81dB
Power Consumption	Analog: 16.9µW Digital: 5.5µW Total: 22.4µW
FoM	0.13pJ/conv. -step
Active Area	0.133mm^2

TABLE II. PERFORMANCE BENCHMARK

	[9] CICC'10	[10] CICC'11	[11] ISSCC'11	This Work
Process[um]	0.13	0.13	0.18	**0.065**
Supply[V]	1.2	0.9	1.5	**1**
Bandwidth[KHz]	8	4000	1000	**10**
Peak SNDR[dB]	56	77	79.3	**80**
Power[µW]	4.8	13800	2900	**22.4**
FoM[pJ/step]	0.14	0.298	0.21	**0.13**

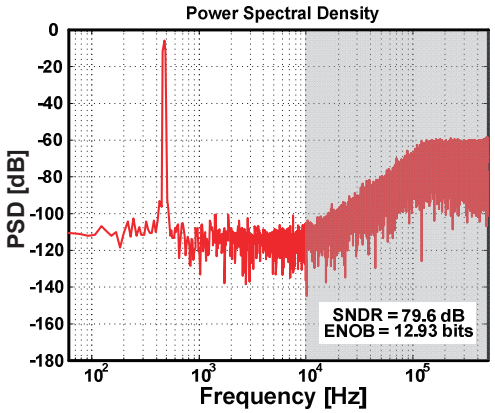

Fig. 7: Measured Power Spectral Density of the ΣΔ modulator.

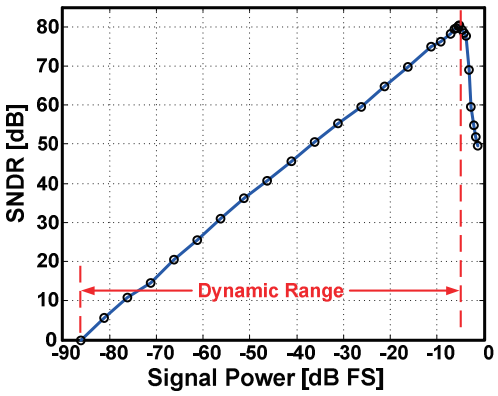

Fig. 8: Measured DR of the ΣΔ modulator.

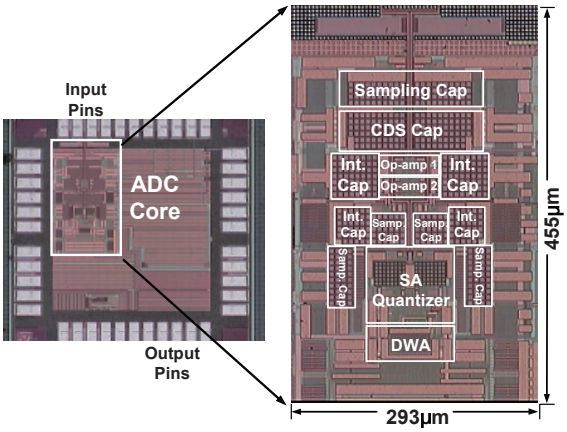

Fig. 9: Chip die photograph.

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