

3.9 An RF-to-BB Current-Reuse Wideband Receiver with Parallel N-Path Active/Passive Mixers and a Single-MOS Pole-Zero LPF

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The latest passive-mixer-first wideband receiver (RX) [1] has managed to squeeze the power (10 to 12mW) via resonant multi-phase LO and current-reuse harmonic rejection BB, but the removals of *RF gain* and *virtual ground* severely penalize its NF (10.5±2.5dB), while devaluing its original IIP3 benefits (+10dBm). The described wideband RX exploits an RF-to-BB current-reuse topology, with parallel N-path active/passive mixers, to leverage such power-performance tradeoffs. Specifically, the RX features: 1) a *current-reuse RF front-end* with an N-path active mixer to realize most RF-to-BB functions in the current domain, resulting in better power efficiency and linearity; 2) a *feedforward N-path passive mixer* to enable LO-defined input matching with zero external components, while offering frequency-translated band-pass filtering and noise cancelling; 3) a *single-MOS pole-zero LPF* to perform current-mode BB filtering while alleviating the tradeoff between the in-/out-of-band linearity, and 4) a *BB-only two-stage harmonic-recombination (HR) amplifier* to boost the 3rd and 5th harmonic rejection ratios (HRR_{3,5}) with low hardware intricacy. Targeting the TV-band (0.15 to 0.85GHz) cognitive radios for IEEE 802.22/802.11af, the RX manifests favorable NF (4.6±0.9dB) and out-of-band IIP2/IIP3 (+61/+17.4dBm) under low power dissipation (10.6 to 16.2mW).

Figure 3.9.1 depicts the RF front-end that unifies most functions. A single-ended RF input (V_{in}) avoids the balun and its insertion loss. The $-g_{m,CS}$ stage (M_{CS}) serves as the LNA, which is stacked by an 8-path active mixer (M_{A1-8}) for down-conversion, and an 8-path current-mode LPF for channel selection before BB I-to-V conversion at R_L ($V_{BB0}, V_{BB45}, \dots, V_{BB315}$). M_{A1-8} driven by an 8-phase 12.5%-duty-cycle LO ($V_{LO0}, V_{LO45}, \dots, V_{LO315}$) allow HR at BB to enhance the critical HRR_{2,6}. A feedforward 8-path passive mixer (M_{P1-8}) driven by the same set of LOs, but anti-phased with M_{A1-8} , is added for three intents:

Input Matching and Out-of-Band Filtering: Owing to the bidirectional transparency of passive mixers [1-4], M_{P1-8} can frequency-translate the low-pass impedance ($Z_{in,LPF}$) of V_x to a band-pass one ($Z_{in,RF}$) at V_{in} , allowing LO-defined input matching and RF filtering. Moreover, the BB signal at V_x is upconverted to V_{in} and downconverted back to V_x by the $-g_{m,CS}$ stage and M_{A1-8} . The resultant positive loop gain is $G_{loop} = g_{m,CS} R_{in,LPF} / 8$, where the factor 8 comes from the number of mixer paths. To ensure stability (i.e., $Z_{in,RF} > 0$), G_{loop} can be set as 0.55 (i.e., $g_{m,CS} = 20\text{mS}$, $R_{in,LPF} = 220\Omega$), resulting in a 2.2x increment of $Z_{in,RF}$. This act permits a smaller R_{SW} (6 Ω) to enhance the ultimate stopband rejection at V_{in} , which is theoretically 13.3dB [$2R_{SW}(R_{SW} + R_S)$]. To vacate more voltage headroom and enhance the linearity, M_{A1-8} were biased in the *triode* region. This approach brings down the swing at V_y (drain node of M_{CS}) and frequency-translates the low-pass $Z_{in,LPF}$ from V_x to a band-pass one at V_y , aiding the out-of-band rejection.

Input Biasing: unlike the TV-band RXs in [5-6] that entail a bulky external inductor for bias and wideband impedance matching, here the gate of M_{CS} is biased via the passive mixers copying the dc voltage from V_x to V_{in} , avoiding any external parts while giving adequate overdrive voltage ($V_{DS} = 420\text{mV}$) on M_{CS} for better linearity. Moreover, owing to no AC-coupling capacitors at V_{in} , the RF bandwidth easily covers the low-frequency range.

Noise Cancelling: the anti-LO-phased active and passive mixers allow *concurrent* noise cancellation of R_{SW} and LPF under $g_{m,CS} R_S = 1$ (Fig. 3.9.2). For the former, R_{SW} induces a noise current to R_S , and is sensed by the $-g_{m,CS}$ stage to produce an anti-phased output nullifying the noise inherently. For the latter, when the RX is operated differentially, the LPF's noise current on R_S will be copied to another path with the same phase, being a cancellable common-mode noise. Hence, the RX NF is dominated by the thermal noise of M_{CS} (i.e., Noise Factor = $1 + \gamma$, where γ is the channel noise factor), which can be upsized (W/L: 120/0.18) to reduce the 1/f noise. M_{A1-8} contribute insignificant noise and are small in size (W/L: 12/0.06) to save the LO power.

The current-mode Biquads in [5,6] only can synthesize two complex poles, while the proposed single-MOS LPF (Fig. 3.9.3) offers stronger pole-zero filtering, being more cost-effective than its real-pole-only counterparts [1-4]. The LPF's transfer function relies on R_B , C_B , and an intentionally large transistor M_{LPF} (W/L: 768/0.5). The latter brings in large parasitics C_{gd} (~0.3pF) and C_{ds} (~0.3pF) under bulk-source connection, introducing two stopband zeros. By tuning the zeros to 150MHz, stopband rejection at 100-to-200MHz offset can be enhanced, suitable for filtering the GSM850/900 bands when the RX is to operate up to 710MHz (IEEE 802.11af). The simulated bandwidth has a mean value of 14.6MHz ($\sigma = 0.48\text{MHz}$). Another useful property of the LPF is the peaking of $Z_{in,LPF}$ around the cutoff, which avoids the fast roll-off shape when it is translated to RF. The grounded C_B essentially suppresses the out-of-band interferers before they see the active device (M_{LPF}). Without affecting most in-band metrics, C_B can be upsized to concurrently narrow the RF and BB bandwidths at the expense of die area. Elegantly, the stopband profile of this LPF is highly insensitive to R_L , easing the tradeoff between the in-/out-of-band linearity. V_{bias} from a replica RF front-end handily aids the biasing.

Single-stage HR shows an uncalibrated HRR_{3,5} of 34 to 45dB [1,3]. The proposed BB-only two-stage HR amplifier (Fig. 3.9.4) boosts the HRR_{3,5} without the gain scaling at RF [4], resulting in simpler layout and lower parasitics. Owing to the embedded BB channel selectivity at the RF front-end, the linearity of such HR amplifiers is highly relaxed, resulting in power savings. The latter also leads to limited BB bandwidth assisting the stopband rejection. The gain weighting is based on a PMOS amplifier {2:3:2} followed by an NMOS amplifier {5:7:5} to approximate the gain ratio {1:√2:1} with <0.1% error [4]. Thus, the total relative gain error becomes insignificant due to the multiplication: $(\epsilon_0 + \epsilon_{1,HR}) \epsilon_{2,HR} / 4$, where ϵ_0 is the relative gain error of the RF front-end, and $\epsilon_{1,HR} / \epsilon_{2,HR}$ is the relative gain error of the 1st/2nd stage HR amplifier. The simulated worst HRR_{3,5} is >53dB (mean=62dB). Thus, the HRR_{3,5} is dominated by the LO phase error.

The RX fabricated in 65nm CMOS occupies a small die area of 0.55mm² that is dominated by the 8-path LPFs with $C_B = 24\text{pF}$. From 0.15 to 0.85GHz, all LO-defined S_{11} are <-12.5dB. The RF-to-IF gain is 51±1dB and NF is 4.6±0.9dB. The power rises with the frequency from 10.6 to 16.2mW, in which 7.5mW due to the static power (RF+BB). At 0.7GHz RF and maximum gain, the IIP2/IIP3 raises from +15/-12dBm (in-band) to +61/+17.4dBm (out-of-band). The BB bandwidth is ~9MHz with 86.3dB stopband rejection at 150MHz offset, thanks to the dual stopband zeros. The out-of-band P_{1dB} is -2.5dBm at 50MHz offset, enhanced by the RF filtering.

The chip summary is given in Fig. 3.9.6. Benchmarking with the passive-mixer-based RXs [1-4], this work succeeds in saving the power without sacrificing the NF, out-of-band linearity and HRR. No external component is entailed and stronger BB filtering is achieved in a small die size. Figure 3.9.7 shows the RX die micrograph.

Acknowledgements:

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References:

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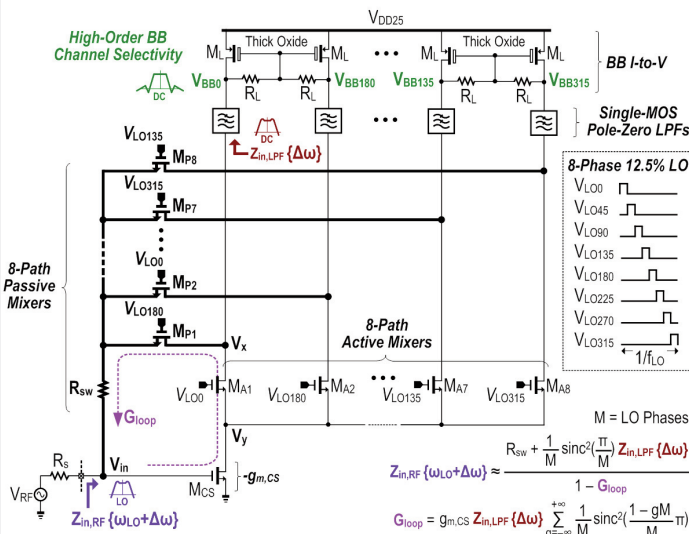


Figure 3.9.1: A current-reuse RF front-end with a single-ended RF input.

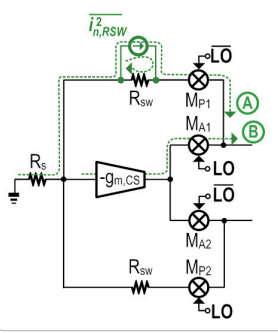
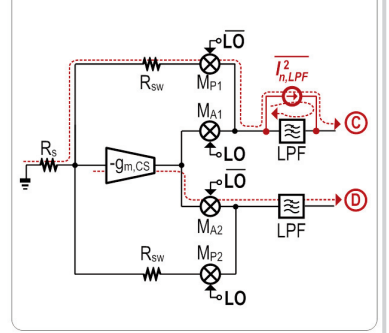
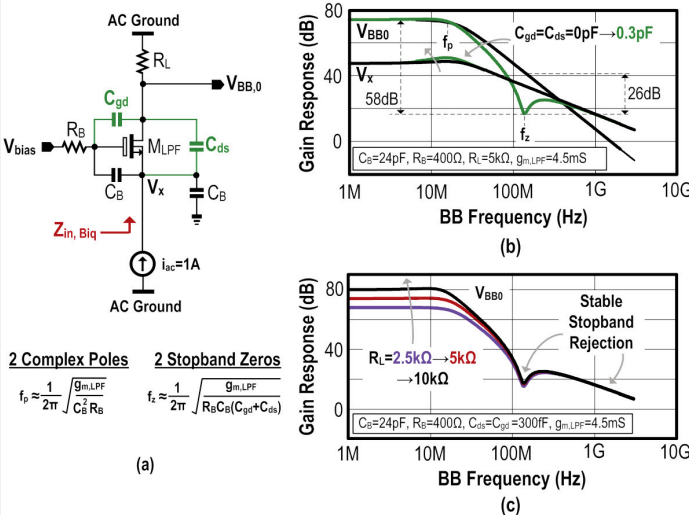
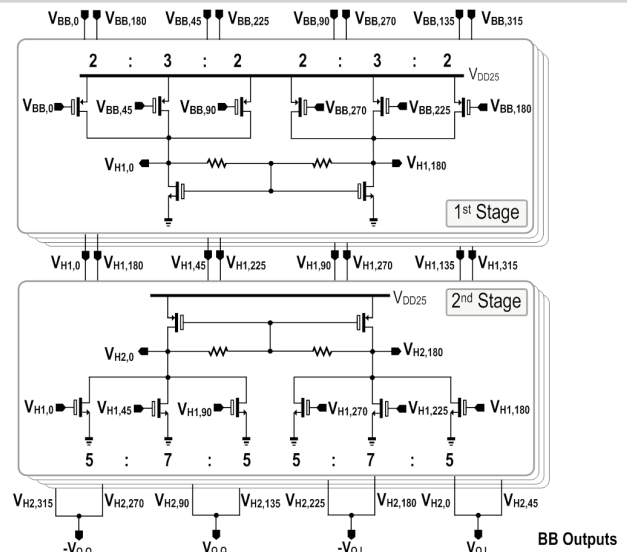
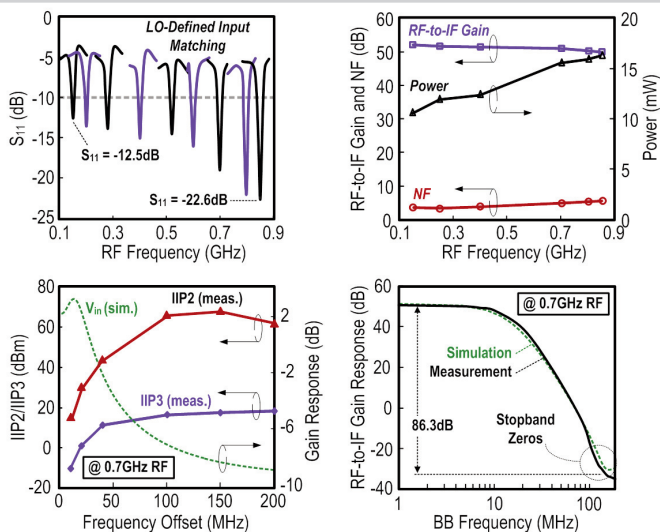
Noise cancellation of passive mixer (R_{sw}) under $R_s g_{m,CS} = 1$ (A) Path: $-k_1 i_{n,RSW}^2$ (B) Path: $k_1 i_{n,RSW}^2 R_s^2 g_{m,CS}^2$ Noise cancellation of LPF under $R_s g_{m,CS} = 1$ (C) Path: $k_2 i_{n,LPF}^2$ (D) Path: $k_2 i_{n,LPF}^2 R_s^2 g_{m,CS}^2$ k_1 and k_2 are constant representing the noise currents leak to R_s Figure 3.9.2: Simplified two-phase noise equivalent circuits of the RF front-end showing the noise cancellation of R_{sw} (left) and LPF (right).Figure 3.9.3: a) Single-MOS pole-zero LPF. b) Simulated V_{BB0} and V_x showing the rejection added by the stopband zeros. c) Sizing R_L for In-band gain.

Figure 3.9.4: BB-only 2-stage harmonic-recombination (HR) amplifier.

Figure 3.9.5: Measured S_{11} , RF-to-IF gain, NF and power; IIP2/IIP3; RF-to-IF gain response.

	This Work	JSSC '13 [1]	VLSI '13 [2]	ISSCC '12 [3]	ISSCC '09 [4]
RX Architecture	Current-Reuse RF Front-End + Feedforward Passive Mixer	Passive Mixer + BB LNA	RF LNA + Passive Mixer + G_m -C + Op-Amp	2-Path Noise-Cancelling + Passive Mixer + Op-Amp	RF LNA + Passive Mixer + Op-Amp
Downconversion	Active / Passive	Passive	Passive	Passive	Passive
RF Input Style	Single-Ended	Single-Ended	Differential	Single-Ended	Differential
RF Range (GHz)	0.15 to 0.85	0.7 to 1.6 (8-phase path)	0.4 to 3 (8-phase path)	0.08 to 2.7	0.4 to 0.9
Power (mW) @ RF	10.6 @ 0.15GHz 16.2 @ 0.85GHz	10-12 @ 0.7GHz 10-12 @ 1.6GHz	20 @ 0.4GHz 40 @ 3GHz	37 @ 0.08GHz 70 @ 2.7GHz	49 @ 0.4GHz 60 @ 0.9GHz
DSB NF (dB)	4.6 ± 0.9	10.5 ± 2.5	1.8 to 2.4	1.9 ± 0.4	4 ± 0.5
Ultimate Out-of-Band IIP3 (dBm)	+17.4	+10	+3	+13.5	+16
Ultimate Out-of-Band IIP2 (dBm)	+61	+26.6	+85 (calibrated)	+54	+56
External Parts	Zero	Zero	Transformer	Zero	2 Inductors and 1 Transformer
Active Area (mm ²)	0.55	2.9 (inc. VCOs)	~0.5 (from Fig.)	1.2	1
BB Filtering Style	2 Complex Poles + 2 Stopband Zeros (Current-Mode)	1 Real Pole (Passive-RC)	2 Real Poles (Active/Passive-RC)	2 Real Poles (Active/Passive-RC)	2 Real Poles (Active-RC)
HRR _{3,5} (dB)	>53, >51	34, 34	70, 55 (calibrated)	42, 45	60, 64
BB Bandwidth (MHz)	9	20	0.5 to 50	2	12
RF-to-IF Gain (dB)	51 ± 1	37	36	72	34.4 ± 0.2
Supply (V)	1.2, 2.5	1.3	0.9	1.3	1.2
CMOS Technology	65 nm	65 nm	28 nm	40 nm	65 nm

Figure 3.9.6: Chip summary and benchmark with recent passive-mixer-based RXs [1-4].

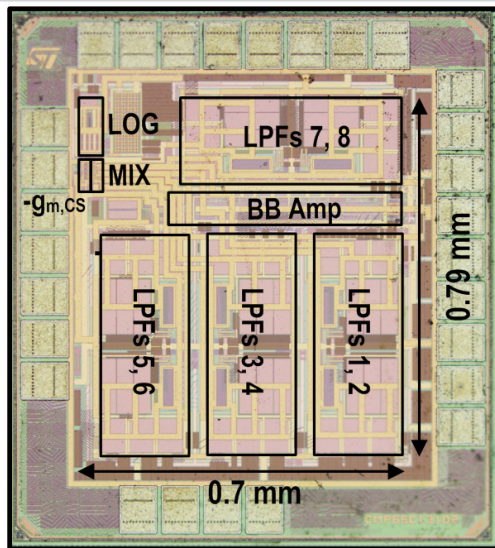


Figure 3.9.7: RX die micrograph.