Parasitic Calibration by Two-Step Ratio Approaching Techinque for Split Capacitor Array SAR ADCs

Si-Seng Wong, Yan Zhu, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, R. P. Martins
Analog and Mixed Signal VLSI Laboratory (http://www.fst.umac.mo/en/lab/ans_vlsi/index.html)
Faculty of Science and Technology, University of Macau, Macao, China
E-mail: ma96552@umac.mo

Abstract—**A calibration technique is proposed to apply for split capacitor array of successive approximation register (SAR) ADC. This technique calibrates the parasitic effects of the split capacitor array by two-step ratio approaching technique, and achieves medium-to-high resolution. The calibration technique is designed and simulated under a 10-bit 100MS/s SAR ADC structure, with 15% to 25% of top plate parasitic capacitance. The simulation results show that the proposed technique can improve the THD from -41 dB to -59 dB at Nyquist input frequency for the worst case. The DNL/INL is improved from 5.02/5.6 LSB to 0.25/0.38 LSB, respectively.**

Keywords--analog-to-digital converter (ADC); split capacitor array; sucessive approximation register (SAR); parasitic calibration; offset calibration

I. INTRODUCTION

SAR ADC is a popular ADC architecture applied for many high-performance digital communication systems and high-quality video systems because SAR ADC can achieve medium-speed, power-efficient, and medium-resolution requirements. Fig. 1 shows the basic architecture of a SAR ADC, which consists of a digital-to-analog converter (DAC) array, successive approximation logic, and a comparator [1]. The SA logic controls the operation of the DAC by performing binary-scaled feedback. The DAC array samples input signal and processes residue from subtraction with the reference voltage during conversion, so it is the core part of the SAR ADC.

The split capacitor array is more attractive than traditional binary-weight capacitor (BWC) array because of smaller input equivalent capacitance and lower power consumption [2]. However, the parasitic capacitance reduces the linearity of the DAC array, which degrades the overall performance of the ADC [3]. Especially in modern nanometer technology, small unit capacitors are widely used due to speed and power consideration, which causes more non-idealities for the split capacitor array because the parasitic effect becomes more critical.

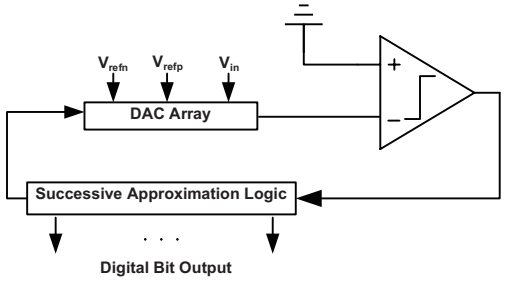

Figure 1. Basic SAR ADC architecture

A split-capacitor array with a larger attenuation capacitor together and a calibration capacitor bank is proposed here after the development from [4] and [5] and enhances the linearity of the implementation. Instead of using C-2C capacitor array as [4] and [5], the proposed calibration capacitor bank reduces the parasitic capacitance limitation. This paper presents a new digital calibration technique which applies two linear voltages to the ADC first, then operates until the specified binary ratio is approached. The calibration algorithm works with the proposed capacitor bank to reduce non-linearity caused by parasitic effect.

II. CAPACITOR ARRAY

A. Conventional Split Capacitor Arrary

The conventional architecture of a split capacitor array is shown in Fig. 2, where the thin lines represent the top plate of the capacitors. The attenuation capacitor is usually calculated as [6]:

$$C_{atten} = \frac{C_{totalLSB}}{C_{totalLSB} - 1} \tag{1}$$

where the total equivalent capacitance of LSB and MSB array are:

$$C_{totalLSB} = \sum_{n=0}^{L-1} 2^n C_0 . \tag{2}$$

$$C_{totalMSB} = \sum_{n=1}^{M-1} 2^n C_0 . \tag{3}$$

Where L and M are the number of bit of LSB and MSB array

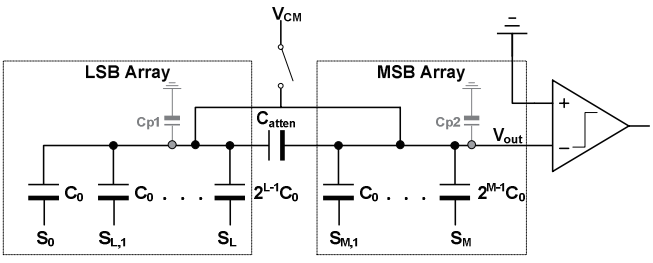

Figure 2. Conventional split capacitor array

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respectively, and C_0 is the unit capacitor of the DAC array. Assume M=L, so that the input capacitance of the DAC array is minimized. Then the equivalent output voltage of the split capacitor array can be expressed as:

$$V_{out}(X) = \frac{C_{atten}[\sum_{n=1}^{L}(2^{n-1}C_0)S_n + \sum_{n=1}^{M}(2^{n-1}C_0)S_n] + (\sum_{n=1}^{M}(2^{n-1}C_0)S_n)(C_{TotalLSB} + C_{p1})}{(C_{TotalLSB} + C_{atten} + C_{p1})(C_{TotalMSB} + C_{atten} + C_{p2}) - C_{atten}^{\ 2}} V_{ref} \quad (4)$$

where S_n represents the switches connected to the DAC array, C_{p1} and C_{p2} are the total top-plate parasitic of LSB array and MSB array respectively. From the equation (4), the parasitic C_{p2} only causes gain error, but C_{p1} brings non-linearity to the DAC array. The parasitic problem can be diminished by reducing the number of bits in the LSB array, and enlarging the MSB array [3]. But the disadvantage is larger equivalent input capacitance and induces lower-speed, larger area, and power usage.

B. Split Capacitor Arrary with calibration capacitor bank

Fig. 3 shows the architecture of the split capacitor array with calibration capacitor bank. The conventional attenuation capacitor C_{atten} shown in equation (1) is replaced by a αC_0 to equalize the nominator between the LSB array and MSB array, and thus enhance the linearity. The value of α can be calculated as:

$$\alpha = \frac{2^{M-1}C_0 + C_{p1}}{(2^{M-1}-1)C_0}. \quad (5)$$

In practical cases, there are some process variations during fabrication, so that C_{p1} varies with processes. Therefore, calibration is required to ensure the circuit always works appropriately.

It is impossible to adjust the value of α during the calibration process because it is extremely sensitive to C_{p1}. Thus, a larger α value must be selected for revising the parasitic range. A capacitor bank is used for digital calibration so that the equation becomes:

$$\alpha = \frac{2^{M-1}C_0 + C_{p1} + C_{bank}}{(2^{M-1}-1)C_0}. \quad (6)$$

Due to the denominator of $(2^{M-1}-1)\,C_0$, it is easier to adjust the switches of C_{bank} to approach the same achievement instead of adjusting α. The calibration circuit applies two linear voltages to the DAC array first. Then it controls the switches of C_{bank} to approach specified binary ratio. The detail information about the calibration algorithm is provided in the implementation session.

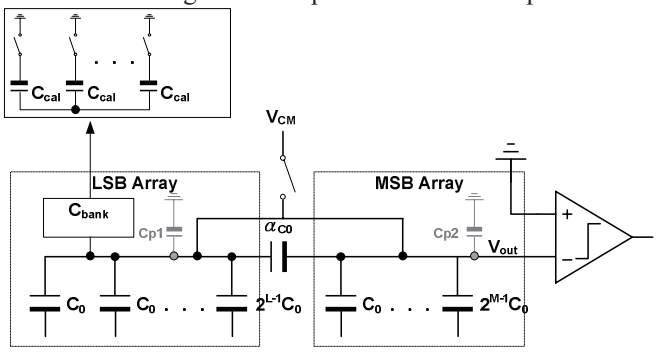

Figure 3. Split capacitor array with calibration capacitor bank

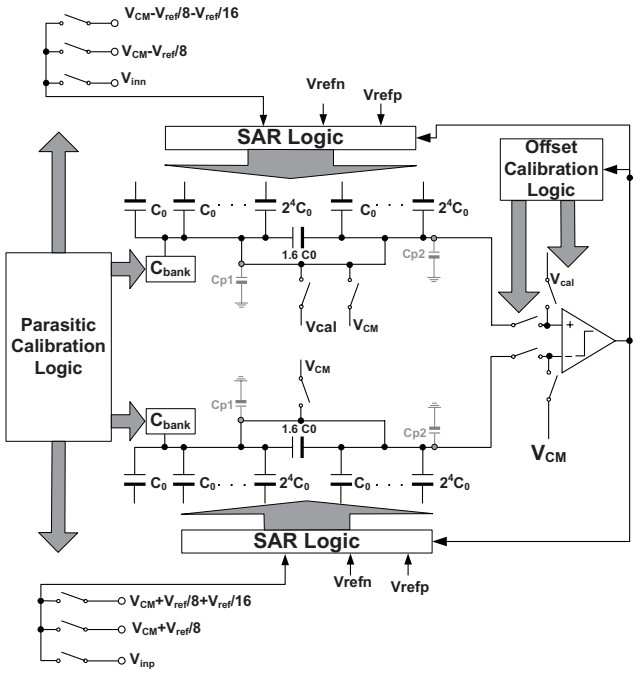

Figure 4. Split capacitor array and calibration block diagram

III. IMPLEMENTATION METHOD

The proposed split capacitor array and the calibration logic are implemented on a 10-bit SAR ADC in 65nm CMOS technology. Fig. 4 shows the block diagram of the implemented circuit. The configuration of the split capacitor array is 5-bit for the LSB array and 5-bit for the MSB array. A unit capacitor (C_0) is about 10fF, which has approximately 20% of top plate parasitic after routing. Assume there is ±5% variation of parasitic. The attenuation capacitor should be around 16fF by equation (5). Then the calibration capacitor bank is estimated to be about 100fF by equation (6). The value of C_{cal} is set to 10fF.

The overall calibration flow chart is shown as in Fig. 5. The first step of calibration is to fixed comparator offset which affects the ADC output codes and therefore obstructs the processing of parasitic calibration. After that, the parasitic calibration logic analyzes the ADC code and determines

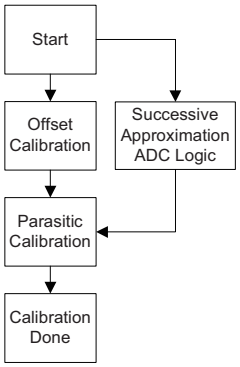

Figure 5. Overall calibration flow chart

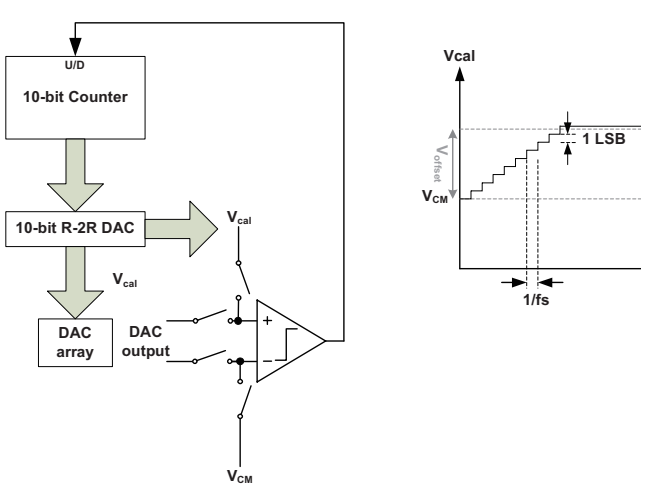

Figure 6. Offset calibration circuit block diagram

whether the calibration progress is done or not. The following sub-sections describe detail of calibration logics.

A. Offset Calibration Logic

Fig. 6 shows the offset calibration circuit block diagram respectively. Assumed the comparator offset is V_{offset}, V_{cal} is fed to the upper DAC array, and the lower DAC array connects with common-mode voltage V_{CM}. The main purpose is to change V_{cal} from V_{CM} to $V_{CM}+V_{offset}$ in order to cancel the comparator offset equivalently, and therefore fully utilize the capacitor array without any modification on the comparator circuit. During the offset calibration process, the differential split capacitor arrays are disconnected from the inputs of the comparator. The calibration voltage V_{cal} is generated from the 10-bit R-2R DAC and compared to V_{CM} by the offset calibration logic (10-bit counter). The R-2R DAC requires 10-bit resolution to achieve 1 LSB step. The calibration logic stops when the output signal of the comparator is flipped.

Compare to conventional offset calibration [4] which adjusts bulk voltage of the comparator input transistor, requiring the extra mask for deep N-well implantation. The proposed offset calibration only employs an R-2R DAC and a counter, which can be utilized in general fabrication process.

B. Parasitic Calibration Logic

The flow chart of the parasitic calibration progress is shown in Fig. 7. The parasitic calibration logic starts after the offset calibration. The non-linearity effect for the split capacitor aray tarts when the code changes from 0000011111 to 0000100000 because the bit shifted from LSB array to MSB array. Therefore, the ADC output code reflects the linearity when applying two linear voltages that can generate codes shifting from LSB array to MSB array. In the implemented 10-bit case, a 10-bit reference ladder is the pre-requirement for the calibration.

The calibration logic compares the ADC output codes to determine the linearity. Refer to Fig. 4, during the parasitic calibration process, V_{inp} and V_{inn} are disconnected from the DAC arrays. $V_{CM}+V_{ref}/8$ and $V_{CM}-V_{ref}/8$ are connected between the DAC arrays to generate $V_{ref}/4$ between the differential

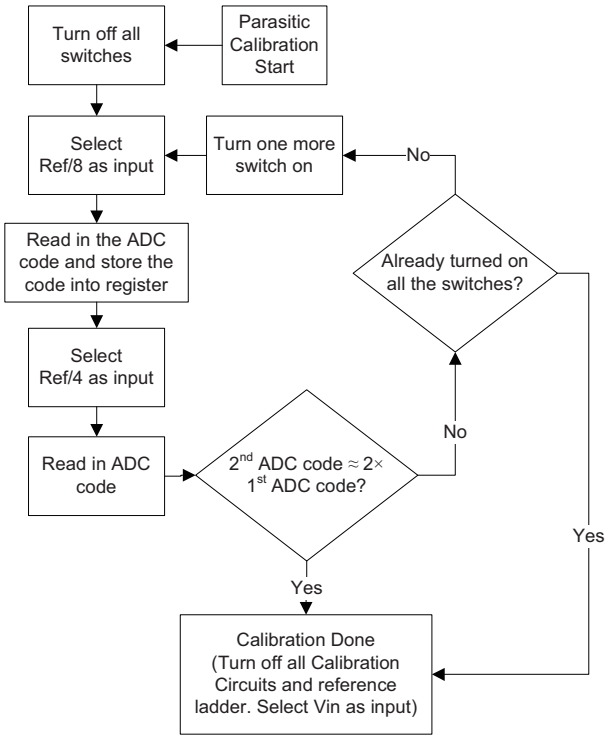

Figure 7. Parasitic calibration flow chart

inputs, where $V_{CM}+V_{ref}/8+V_{ref}/16$ and $V_{CM}-V_{ref}/8-V_{ref}/16$ generate $V_{ref}/8$ between the differential inputs. The calibration logic stops when the ADC codes are in ratio of 2:1. After the calibration process, V_{inp} and V_{inn} are resumed back to the DAC arrays for normal SAR ADC operation.

After all calibrations are done, the last step is turning off all calibration circuits and reference ladder to save power. The R-2R DAC can be power-off by switching all binary-scale R to ground because offset does not affect the SAR ADC structure. The V_{CM} is supposed to resume back to the upper DAC array instead of V_{cal}.

IV. Simulation Results

The 10b SAR ADC utilized the proposed split capacitor array and calibration algorithm has been designed in 65 nm CMOS technology with 1 V supply. All the simulation is simulated under the sampling frequency of 100MS/s at Nyquist input, with 20% of top plate parasitic capacitance. The simulation performance shows that the calibration improved the total harmonic distortion (THD) from -41 dB (6.5 bits) to -59 dB (9.5 bits), as shown in Fig. 8 (a) and (b) respectively. The DNL/INL is improved from 5.02/5.6 LSB to 0.25/0.38 LSB, respectively. Fig. 9 (a) shows the DNL and INL performance before calibration. Fig. 9 (b) shows the DNL and INL performance after calibration. The estimated power consumption for the digital calibration logic is about 30 μW.

V. Conclusion

A calibration technique is proposed for split capacitor array SAR ADC. This technique calibrates the parasitic effects of the split capacitor array, and achieves medium-to-high resolution. The calibration algorithm applies two linear voltages to the

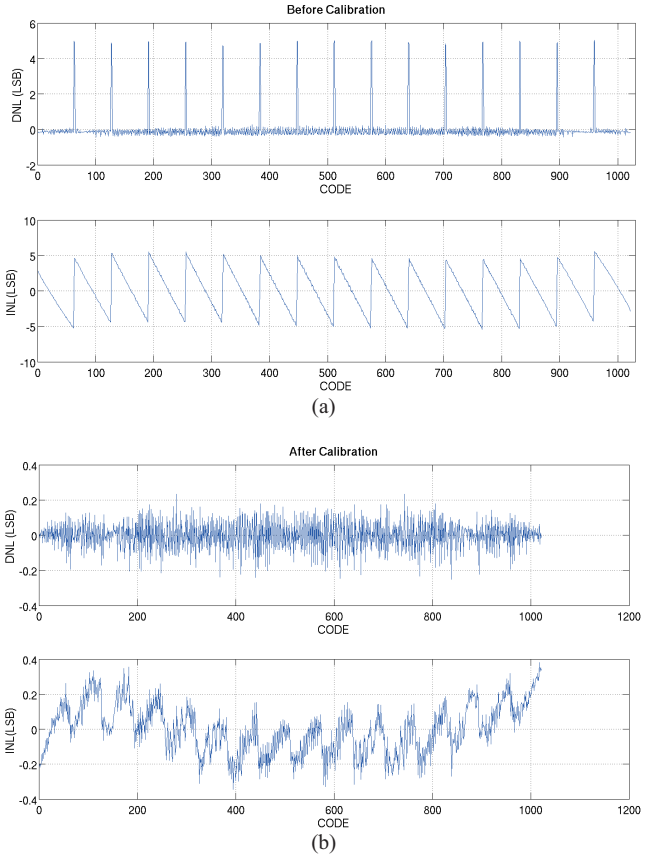

Figure 9. DNL and INL (a) Before Calibration (b) After Calibration

ADC first. Then it operates until the specified binary ratio is approached. The calibration is designed and simulated under a 10-bit 100MS/s SAR ADC structure, with 15% to 25% of top plate parasitic capacitance. The simulation results show that the proposed calibration technique can improve the THD from -41 dB to -59 dB at Nyquist input frequency for the worst case. The DNL/INL is improved from 5.02/5.6 LSB to 0.25/0.38 LSB, respectively.

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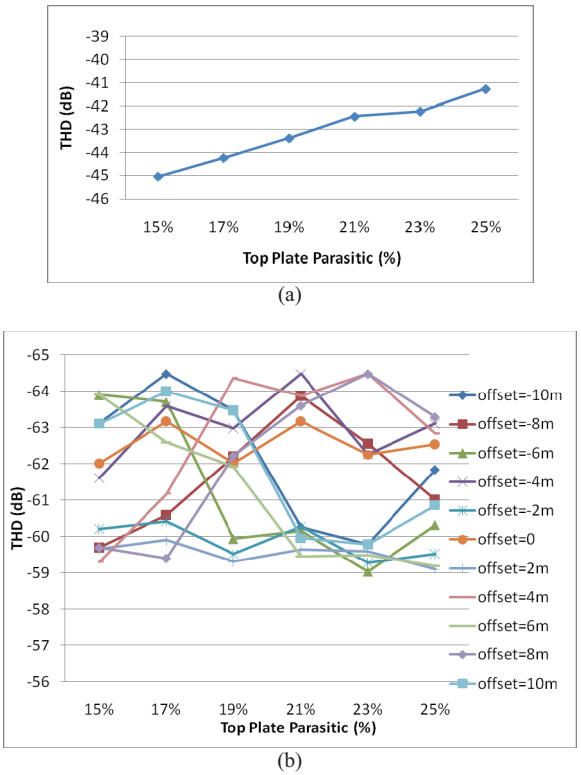

Figure 8. THD versus top plate parasitc at fs=100 MS/s, with Nyquist input frequency (a) Before calibration (b) After calibration

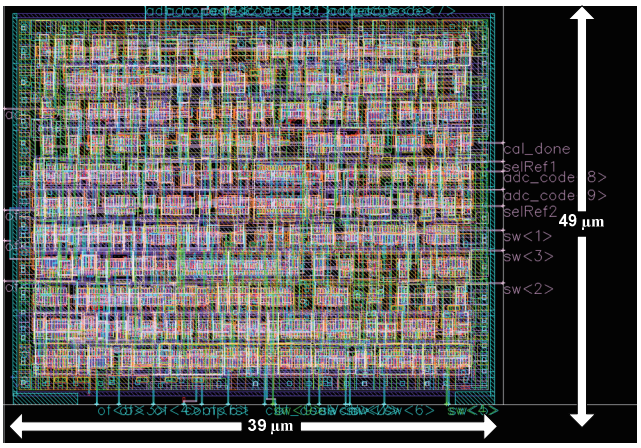

Figure 10. Layout of the calibration logic circuits (metal density filled)