A 39mW 7b 8GS/s 8-way TI ADC with Cross-linearized Input and Bootstrapped Sampling Buffer Front-end

Chi-Hang Chan, Yan Zhu, Zihao Zheng[2], R.P.Martins[2,3]
State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China
2 – Also with Department of ECE, Faculty of Science of Technology, University of Macau, Macao, China
3 – On leave from Instituto Superior Técnico/Universidade de Lisboa, Portugal
email: ivorchan@ieee.org

Abstract - **This paper presents an 8-way time-interleaved 1-then-2b/cycle SAR ADC which features a level-shifter-cross-linearized input (LSCL) and bootstrapped sampling (BSS) buffer to achieve a high-speed and low-power buffered ADC designs. A level-shifter and main buffer are cross-linearized through cascode devices with their outputs, where the inherent main buffer's level-shifted output also helps to linearize the BSS buffer. Unlike the conventional bootstrapped circuit, the proposed BSS buffer bootstraps the gate of the sampling transistor to its source at high speed with minimal signal amplitude loss due to the active operation. It also reduces the load from the main buffer to save power by providing isolation from the boosting circuit. Besides, we utilize a sparkle-error-tolerant decision register in the 1 GS/s 7b sub ADC to alleviate the sparkle-error at large amplitudes without additional latency. The ADC fabricated in 28 nm CMOS technology consumes 23/39 mW, achieving 37.7 dB SNDR@Nyq., with a Nyq.-FoM 81.6/48.1 fJ/conversion-step in w/o and w/ buffer scenario, respectively.**

I. Introduction

An easily driven and low sparkle-codes error rate (SER) ADC is a critical building block in wideband communication systems. The time interleaving (TI) techinque [1]-[4] is often adopted to achieve high speed with smaller power overhead when comparing it with large size-scaling in the transistors. However, such saving comes with the price of extra area as well as a more complex and heavily-loaded input front-end which makes the ADC extremely hard to drive. Besides, the time skew error among the channels requires correction by an additional calibration circuit, while other solutions such as inline-demux [1] or master-slave sampling [2], also ask for a low impedance input signal that leads to a more critical input buffer design in the sampling front-end.

A buffered front-end with the cascode sampler [3][4] can sample at high speed but suffers from the non-linearity of the input and loading pair thus limiting its achievable SFDR to only ~35 dB. Although the feedforward replica capacitor (FFRC) technique [5] can improve the buffer's linearity, it significantly reduces the ADC's input impedance. Besides, as Fig. 1 illustrates, the conventional ADC front-end (FE) comprising a buffer followed by a series bootstrapped (BS) sampling switch leads to a slow rise-time in the BS clock, as both the large final load (C_S) and parasitic capacitance significantly degrade the rise-time and amplitude of the boosting signal V_g.

Multi-bit SAR ADCs are often clocked in a synchronous (syn.) manner. In order to improve the SER, one can apply latching to the metastability flag bit [3] or a boundary-code-detection scheme [6]; however, both solutions lead to a longer conversion latency and/or complex decode logic.

In this work, we adopt master-slave sampling to avoid the timing calibration in an 8-way TI ADC. In order to provide a high input impedance and alleviate the long rise-time of the sampling clock from the BS circuit, while otherwise needs to budget more power on the input buffer, we present a level-shifter-cross-linearized (LSCL) input and bootstrapped sampling (BSS) buffers which have >5x input impedance at 4 GHz when compared to FFRC [5] obtaining a SFDR > 47 dB at the Nyquist input with a fast rise-time in the BS clock. Besides, we also propose a SE-tolerant decision register which achieves a more than 4-fold SER reduction from the previous

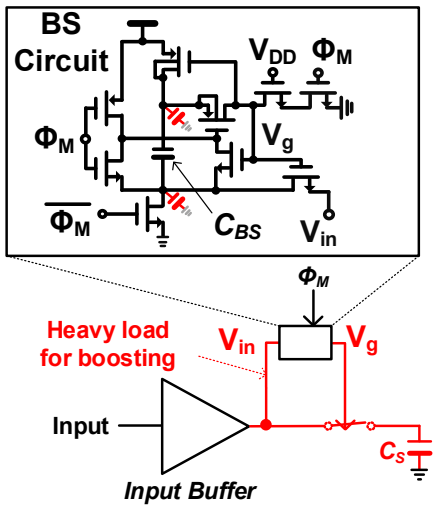

Fig. 1. Conventional sampling front-end (load highlighted).

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design [7] with only a single additional gate delay and no latency. The experimental results of a 28 nm CMOS prototype demonstrate a competitive energy efficiency comparing with a state-of-the-art design even with input buffer. The SNDR is 37.7 dB at Nyquist input and the SFDR is limited by the timing error only when the input is above 7 GHz. The ADC occupies a 0.03 mm^2 core area with a total power consumption of 39 mW, including the input buffer and an on-chip offset calibration circuit. The achieved Walden FoM is 81.6 fJ/conversion-step at Nyquist input, with a measured SER at large error amplitudes being suppressed to less than 10^{-10}.

II. ADC Architecture

Fig. 2 shows the overall buffered ADC architecture, which consists of a LSCL input buffer, BSS buffer, clock generator and 8-way TI ADC. Each channel has its own bootstrapped switch sampler and operates as 1-then-2b/cycle SAR architecture with background offset calibration [7]. To relieve the timing-critical clocks, we utilize a 1-8 hierarchical master-slave sampling front-end. The 50Ω terminated input is isolated by the LSCL buffer which uses a level-shifter (LS) to improve its linearity. The inherent level-shifted output from the buffer also feeds another BS buffer clocked by Φ_M at 8 GHz to offer a bootstrapped function for the master sampling switch (S_M). The slave switches in each channel sample at 1 GHz with $\Phi_{1\text{-}8}$ where one out of eight phases is coincident with Φ_M. While Φ_M ends 50 ps earlier than $\Phi_{1\text{-}8}$, the only jitter-critical clock remains Φ_M and the timing requirement among $\Phi_{1\text{-}8}$ is greatly relaxed.

The sub ADC utilizes the 1-then-2b/cycle SAR architecture due to its outstanding energy efficiency. We adopted capacitive interpolation techniques to reduce one DAC and the comparators' output passes through a SE-tolerant decision register before feeding the controls of the DACs. We calibrate the offset among the comparators in the background on-chip.

III. Proposed Buffered ADC Sampling Front-end

A. Input Buffer and Bootstrapped Sampling Buffer

The conventional bootstrapped, that consists of a buffer followed by a series sampling switch (Fig. 1), is very inefficient in the high-speed sampling front-end. During the sampling period, the bootstrapped voltage needs to be quickly shifted by the buffered input in order to provide a constant gate-source-voltage (V_{GS}) with low on-resistance for the sampling switch. However, both the large final load and parasitic capacitance at the top-plate of the boosting capacitor (C_{BS}) significantly degrade the rise-time and amplitude of the bootstrapped clock. While enlarging C_{BS} can moderate the amplitude attenuation, it leads to a diminished-return on the rise-time due to the larger parasitic or otherwise needs to budget more power on the input buffer.

Fig. 3 presents the circuit schematic of our buffered sampling front-end which comprises a LS, LSCL input buffer, BSS buffer and master sampling switch (S_M). To simplify the channel-length modulation on M_1, its drain-source voltage

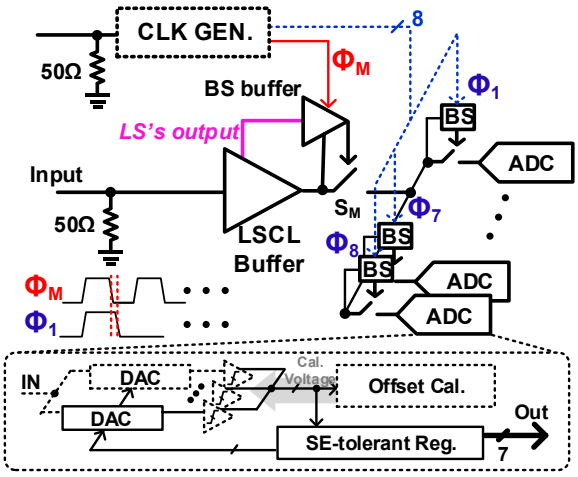

Fig. 2. Overall 8-way time-interleaved buffered ADC architecture.

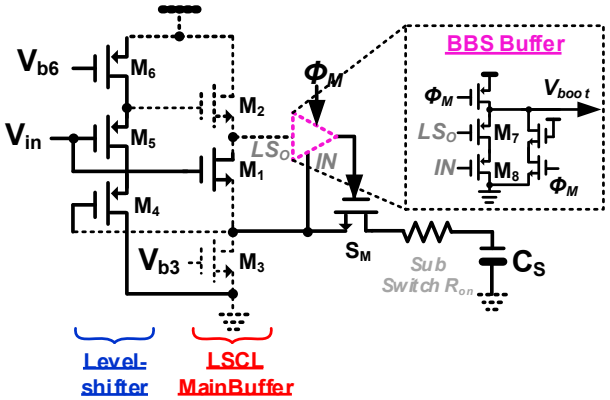

Fig. 3. Circuit schematic of the level-shifter, main buffer and bootstrapped sampling buffer in the sampling front-end.

(V_{DS}) variation is reduced by bootstrapping the drain voltage of the follower utilizing the LS and cascode device M_2 where the LS is also linearized by the feedback from the output of the main buffer through M_4. The linearized level-shifted output (LSo) also supports the BS buffer providing a fast rise-time for the sampling switch control with a constant V_{GS}. The BSS buffer is a clocked PMOS input source-follower where M_7 is also linearized by the main buffer's output using M_8. Unlike the conventional approach, the boosting gate voltage for the sampling switch is supported by an active buffer that avoids signal attenuation and also helps to isolate the additional loads from the S_M and boosting circuit. The additional power from the BSS buffer can be budgeted from the LSCL as now it drives less load when compared with the conventional one. Besides, the load of the BSS buffer is small as it mainly consists of the transistors' parasitic in the signal path. Based on the simulation, the level-shifter-cross-linearization and the BSS linearization improves the THD of the sampling front-end >15 and 5 dB, respectively.

B. Input Impedance Comparison

Except the kickback noise reduction from the sampling clock, one of the most common reasons to add a buffer before

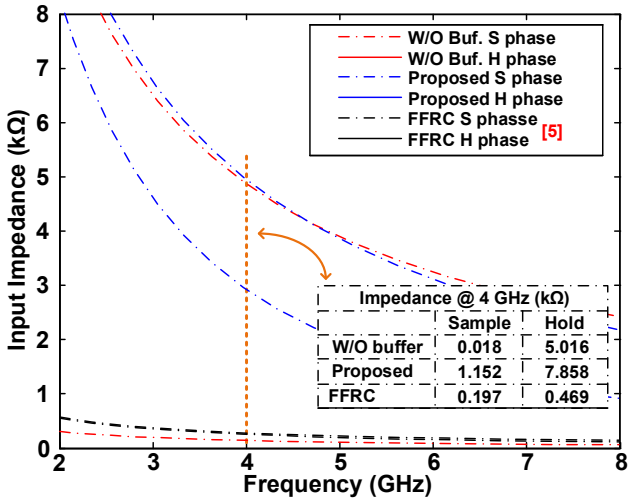

Fig. 4. Input impedance comparison between different sampling circuits.

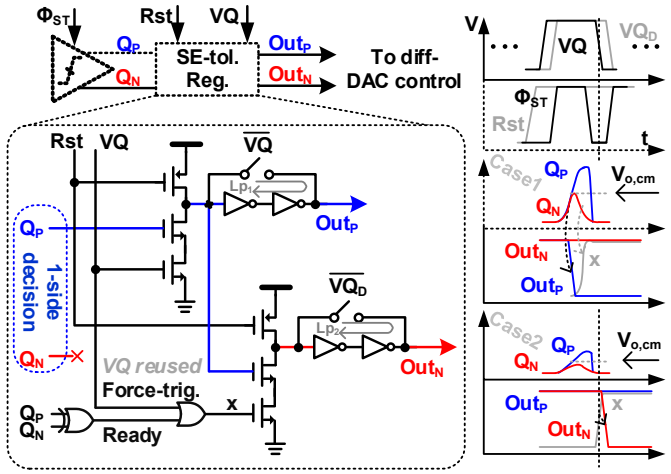

Fig. 5. Circuit schematic of the SE-tolerant decision register with signal behavior during faulty outputs from the comparator.

the ADC is to provide a high and constant impedance that can be easily driven by the previous circuit. In Fig. 4, we plot the input impedance simulation results with and without buffer for the different front-end sample and hold circuits. The values of the components, such as sampling capacitance (C_s) and on-resistance of the switch (R_{on}), are selected based on this work, where Cs = 240 fF and R_{on} = ~20Ω. Without the input buffer, it can be observed that the input impedance is very high during the hold-mode but it drops dramatically during the sample-mode. Such large time-variant impedance not only causes time-variant reflection but also makes the ADC harder to drive due to such low input impedance. While by inserting a buffer, the input impedance can be enlarged significantly. However, it can be found that the feedforward replica capacitor (FFRC) buffer [5] still suffers from a low input impedance even in both modes. While the FFRC technique aims for very high accuracy and speed, our front-end poses an intermedia solution for the moderate resolution and speed designs. The simulation results show the proposed LS assisted cross-linearized buffer achieving more than 5x higher input impedance when comparing it with the FFRC buffer under similar input transistor sizing.

IV. SE-TOLERANT DECISION REGISTER

Even though the regeneration time of the comparators is extended by the parallel conversion in multi-bit/cycle SAR ADCs, their SA loop is running synchronously which often leads to a SER worse than 1b/cycle with asyn. loop. On the other hand, the asyn. approach is not effective in multi-bit SAR ADCs due to the extra detection overhead from the multiple comparators and several-fold additional critical comparisons. Besides, a dynamic logic [7] is usually adopted to latch the comparator's outputs at a high speed while its faulty operations can also lead to a large SER. To mitigate the sparkle-code error, we use a SE-tolerant circuit for the SAR control. Fig. 5 shows the schematic of the logic circuit and its signal behavior. In the 1st and 2nd cases, during the comparison Φ_{ST}=1, the outputs of the comparator (Q_P&Q_N) initially pre-charge to a output common-mode voltage ($V_{o,cm}$) and cannot regenerate to a valid difference within a given time. In the conventional logic [7], QN in CASE1 can wrongly trigger the following dynamic logic due to the high $V_{o,cm}$ thus causing both logic outputs ($Outs_P$&Out_N) to be "0" while they offer both "1" with a low $V_{o,cm}$ in CASE2. These non-differential controls lead to a large SER and only CASE2 can be resolved by the asyn. approach. On the contrary, our logic circuit only monitors a single side output while the differential is triggered by an output ready or force-triggered signal (VQ reused). In the CASE1 example, OUT_P=0 is triggered by Q_P which also secures OUT_N=1 even and Ready forces node X to pull up. In CASE2, both Q_P&Q_N cannot trigger OUT_P&OUT_N. While OUT_P=1, node X is pulled up by VQ that secures OUT_N=0. Since the differential controls only depend on a single-side decision from the comparator, it significantly reduces the chance that the logic decision is affected by $V_{o,cm}$. Nevertheless, a deeply metastable condition can still possibly originate a SE. This scenario has to fulfill the following criteria: OUT_P&OUT_N keep not well-defined even with the gain from the logic and positive feedback loops (L_{P1}&2), which is extremely rare during the measurement (<1e-10). The DAC settling error due to a slow decision from OUT_N can also lead to a SE in a small amplitude that only can be suppressed by budgeting extra time for the DAC settling.

V. MEASUREMENT RESULTS

Fig. 6 exhibits the 8-way TI ADC with background offset calibration in 28nm CMOS, which consumes a total of 39mW power at 1/1.8 V supply under 8 GS/s. The power ratio of LS, main buffer and BS buffer is 1:10:4, where the buffer consumes ~ 16 mW from a 1.8 V supply. Fig. 7 illustrates the measured SNDR and SFDR versus the input frequencies after the cross-channel gain and offset calibration, where the SNDR stays above 37.7 dB up to the Nyquist input. Fig. 8 depicts the frequency spectrum at the near-Nyquist-input. The SFDR is mainly limited by the 3rd harmonic from the buffer before 6.9 GHz input. The

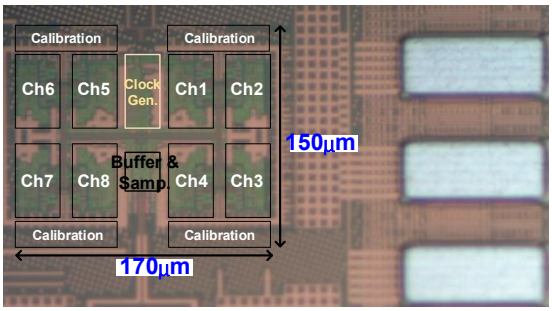

Fig.6. Die microphotograph of the ADC.

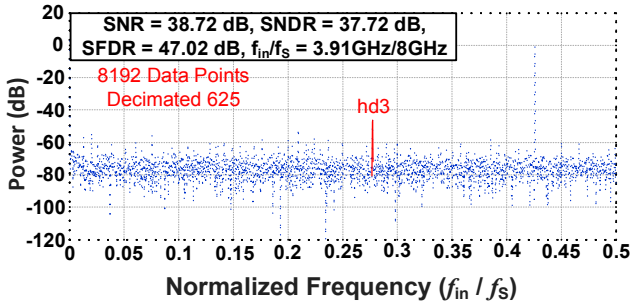

Fig.7. Spectrum with near Nyquist input (decimated 625x)

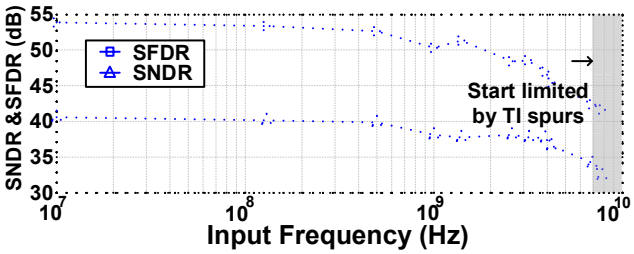

Fig. 8. Measured SFDR and SNDR vs. input frequency.

|DNL/INL| are both <1 LSB. Fig. 9 presents the measured SER in different modes of operation. In the conventional approach, the SER can be as large as 1E-4. While only by configuring the logic in the single-side mode can reduce it down to ~1E-6. Finally, by enabling the force-triggered clock, the SER remains <1E-8. Table I summarizes the ADC's performance and compares it with the state-of-the-art w/ and w/o the buffer, the Walden FoMs are 48.1 and 81.6 fJ/conv.-step, respectively. The energy efficiency of the proposed buffered ADC is competitive with other design w/o buffer but requiring timing calibration.

VI. Conclusions

This paper reports an 8-way time-interleaved 1-then-2b/cycle SAR ADC. A level-shifted assisted cross-linearized input and bootstrapped sampling buffer are proposed to achieve a high-speed sampling front-end at low power. The sampling front-end also experiences a high input impedance during both sample- and hold-modes which eases the ADC's driver. We presented a SE-tolerant decision register to alleviate the sparkle-error at large amplitude in multiple SAR ADCs. The measured results demonstrate that the SNDR of the ADC at Nyquist input is 37.7 dB with a SER better than 10^{-10} at large

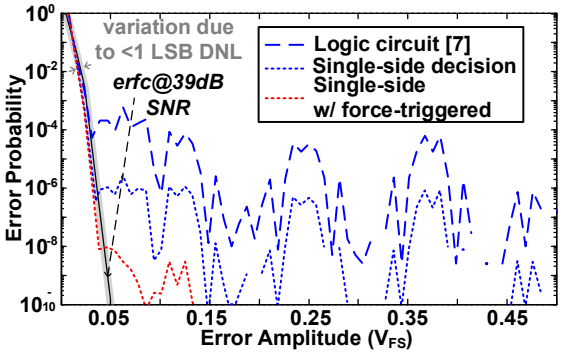

Fig.9. Measured SER from 1 channel at 1GS/s of three logic circuits in SAR control, which are [7], single-side and single-side with force-triggered.

TABLE I. Summary of Performance and Benchmark

Publication	VLSI'13 [8]	JSSC'14 [4]	ISSCC'16 [9]	This work	
Architecture	8xTI SAR	2b/cycle SAR	32xTI SAR	8xTI Multi-SAR	
Technology	32nm SOI	65nm	28nm	28nm	
Resolution	8b	6b	8b	7b	
f_S (GS/s)	8.8	12.8	16	8	
SNDR(dB)@f_{in}	36.98@ 3.8GHz	26.4@6.4GHz	37@7.8GHz	37.7@3.9GHz	
Power (mW)	27.4	*162	*320	23	*39
FoM@Nyq./$_{step}$	71fJ	*740fJ	*350fJ	48.1fJ	*81.6fJ
Area (mm^2)	0.025	0.232	0.534(ADC)	0.03	
Input Buffer	NO	YES	YES	YES	
Timing Cal.	YES(offchip)	No Need	YES(onchip)	No Need	

*w/ buffer

error magnitudes. The total area includes an on-chip calibration circuit with an area of 0.03 mm^2. The achieved Walden FoM is 81.6 fJ/conversion-step with input buffer which is competitive with state-of-the-art designs even without the buffer.

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