A Missing-Code-Detection Gain Error Calibration Achieving 63dB SNR for An 11-bit ADC

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Abstract - **This paper presents a calibration technique based on missing-code-detection (MCD) scheme to correct the gain error between the MSB and the LSB array in SAR ADCs with bridge-DAC structure. The MCD algorithm replaces the gain factor calculation with simple missing-codes count that significantly reduces the calibration digital overhead. It also relieves the linearity requirement of the testing signal; therefore, a simple charge-pump circuit can be utilized as a testing signal generator (TSG). An 80 MS/s 11-bit SAR ADC with the proposed calibration are integrated together in 65nm CMOS. It does not require any external calibration signal and the measurement results demonstrate that the calibration can improve the SNR of the ADC by 7.3 dB from 55.7 dB to 63 dB at the DC input frequency.**

I. INTRODUCTION

SAR ADCs [1]-[5] achieve excellent power efficiency due to their simple architecture and operation which allow moderate speed and high resolution. The DAC and the comparator limit typically the conversion speed and the accuracy in a conventional SAR ADC. To reduce the total number of capacitive units and interconnection for area and power saving the bridge-DAC structure is commonly used [1][3]. By separating the DAC into two arrays through an attenuation capacitor C_a, the bit weight of the MSB can be significantly reduced. However, the mismatch of the attenuation capacitor and the top-plate parasitics in the DAC's inner node [1][3] cause gain error between the MSB- and LSB-array, leading to a systematic DNL error and missing codes. Such conversion error is possible to be calculated and calibrated in digital domain [1][3][4]. The bitwise correlation (BWC) calibration [4] utilizes the pseudorandom signal injection to estimate the error; however, the injected signal reduces the dynamic range of the ADC and the calibration requires a long convergence time with 10 million samples. Another histogram based ratio mismatch (HBRM) [3] calibration estimates the error through the code statistics. The HBRM calibration does not need extra signal injection, but the statistic requires large memories and

computational efforts. Also the algorithm relies on a busy and uniform distributed input signal.

This paper reports a calibration technique for a bridge-DAC [3] employed in a SAR ADC. Based on missing-code detection with a simple TSG, the calibration algorithm can be simplified, thus reducing the digital overhead and removing the dependency of the input signal type when comparing it with the HBRM approach. As the proposed calibration detects the missing codes rather than performing the code statistic, only two adjacent outputs are stored for digital processing, consequently saving considerable memories. Besides, a TSG is implemented on-chip which is enabled at foreground for error detection. Searching for the missing codes only requires a staircase testing signal with a small step-size instead of high linearity thus relaxing the design complexity of the TSG. The calibration was implemented in an 11-bit 80 MS/s SAR ADC. The measured results show that the proposed MCD technique improves the DNL from 1.11/-1 to 0.74/-0.53 LSBs and achieves 63 dB SNR. The calibration only requires about 1500 samples (19 μs) including averaging in the worst case scenario which ensures a short completion time.

II. ADC ARCHITECTURE

Fig. 1 depicts the overall ADC architecture, which consists of a bridge-DAC array, a comparator, a SAR controller, a TSG and a calibration block. The SAR logic controls the DAC which performs the binary-searched feedback to the input signal,
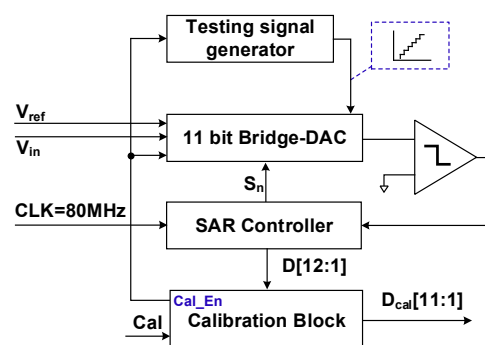
Fig. 1. Overall ADC architecture.

where the V_{cm}-based switching [2] is used for better conversion linearity. Once the calibration is activated by a "Cal" signal, the normal ADC sampling will be interrupted. The ADC input is switched to sample a staircase signal that will be quantized to search for the missing codes. The output will then be passed to the calibration block for the estimation of gain error. One extra bit is resolved during the calibration to further suppress the quantization error and enhance the calibration accuracy. Once the calibration finishes, the ADC will resume to its normal operation and the error will be fixed in the digital domain before the final ADC output.

III. PROPOSED MCD CALIBRATION

A. Static Error in Bridge-DAC

Fig. 2 shows an n-bit (n=k + i) bridge-DAC. Assuming the overall gain error caused by the parasitics C_{PA} and C_{PB} is ignored for discussion. Thus, the DAC output voltage V_{out} can be simplified to

$$V_{out} \approx (\underbrace{\frac{2^i C + C_{PB}}{\delta C_a} \sum_{j=1}^{k} 2^{j-1} C S_{i+j}}_{MSB\ Array} + \underbrace{\frac{1}{\delta} \sum_{j=1}^{i} 2^{j-1} C S_j}_{LSB\ Array}) \cdot V_{ref} \quad (1)$$

$$\delta = (2^i + 2^k - 1)C + 2^{i+k} C / C_a \quad (2)$$

where C is the unit capacitor, and S_j is equal to 1 or 0, representing the digital input. According to (1) the C_{PB} in the numerator results in a gain error between the MSB and the LSB array. Such conversion error can be compensated by enlarging the attenuation capacitor C_a [3]. For instance, if the C_{PB} is 20% of the total capacitance in the LSB array, C_a should be increased by 1.2 times accordingly. However, in practice, the compensation accuracy is vulnerable to process and mismatch, as there exists across-chip-variations of C_{PB} as well as the mismatch of the non-unit capacitor C_a, especially for high resolution target. The digital calibrations [3][4] simplify the ADC implementation as they require less modifications in the ADC itself. However, one design consideration for DAC needs to be taken into account. Fig. 3 illustrates the example of a (2+4) 6-bit ADC transfer characteristic (Fig.3 (a)) and the respective code histograms for several cases (Fig.3 (b-d)). As the MSB array resolves 2 bits it leads to 2^2 regions in the histogram. If the ratio α of C_a is set below the compensated value 1.2, the outputs near the decision boundaries are repeated creating DNL peaks as shown in Fig. 3 (b). Contrarily, in Fig. 3 (c), if C_a is adjusted to above the compensated value, it leads to missing codes with -1 LSB DNL. The positive DNL cannot be removed in digital domain, since the code accumulating cannot be separated in post signal processing [3], but the negative DNL
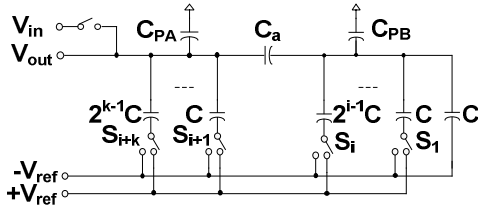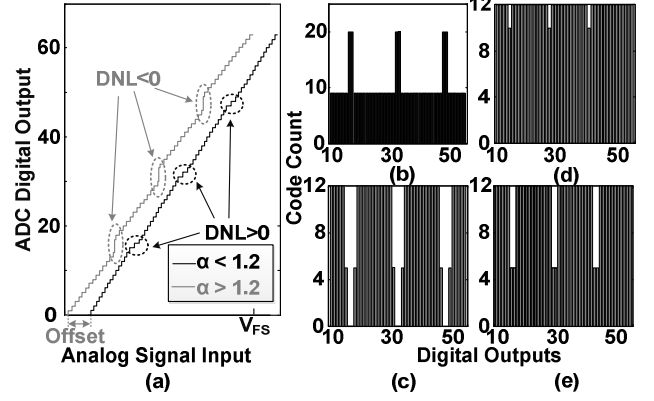

Fig. 3. (a) Transfer characteristic of a 6-bit ADC; (b) Code histogram with α <1.2, and (c) α >1.2; (d) Code histogram with α>1.2 after HBRM calibration, and (e) after MCD calibration.

and missing codes can be fixed. Thus, the C_a is initially designed larger than its compensated value, which results in the output codes inherently containing systematic missing codes that can be later fixed through the MCD calibration.

B. Missing Codes Detection Technique

The MCD calibration method compensates the error by adjusting the bit weight determined in the MSB array. It multiplies a gain factor β by the leading bits determined in the MSB array that can be expressed as

$$D_{cal} = \beta \sum_{j=1}^{k} 2^{j+i-1} D_{j+i} + \sum_{j=1}^{i} 2^{j-1} D_j \quad (3)$$

where D_j equal to 1 or 0 represents the ADC output. As k leading bits are quantized in the MSB array, the output histogram will be divided into 2^k regions. Ideally, since the LSB array determines i-bit, each region will contain 2^i codes. If there is a gain error the actual number of codes will be smaller. The gain factor can be calculated as the ratio between the measured and the ideal value:

$$\beta = \frac{Sum(CN)}{2^i} \quad (4)$$

$$Sum(CN) = 2^i - N_{mc} \quad (5)$$

where Sum (CN) is the measured occurrence of the codes and N_{mc} is the counted number of intrinsic missing codes per-region (2^i codes). The design of the ADC purposely contains several missing codes (≥2 codes) per-region obtained by enlarging the attenuation capacitor during the DAC implementation. Comparing with the HBRM calibration that compensates the negative DNLs < -0.5 LSB, the proposed MCD calibration removes the missing codes and retains the negative DNLs > -1 LSB. The output histograms after the HBRM calibration and the MCD calibration are shown in Fig. 3 (d) and (e), respectively. Though the solution sacrifices a bit the calibration accuracy (less than 0.5 LSB), the digital circuitry for the β estimation is significantly simplified. The logic for MCD calibration does not need to record the code count, instead only the occurrence of the consecutive missing codes which can be easily recognized by subtracting two adjacent outputs. If the

Fig. 2. An n-bit bridge-DAC structure (k+i=n).

result is larger than 1, it implies that the outputs are not consecutive and there are missing codes in the ADC. To completely eliminate the dependency of the input signal, a simple TSG is implemented for calibration purposes.

IV. CIRCUIT IMPLEMENTATION

A. Testing signal generator (TSG)

In this design the MSB- and LSB-array quantizes 7- and 5-bit, respectively, accordingly the range of the TSG covers at least 2^5 codes that is 18.75 mV with a full-scale of 2.4 V_{p-p}. Fig. 4 (a) shows the TSG circuit, which uses a simple PMOS transistor at the top-plate of the DAC working as a charge pump. According to the timing diagram shown in Fig. 4 (b), before calibration the input signal is sampled at the bottom-plate of the DAC. Once the calibration is trigged (Cal_En=1), the bottom-plate switches connecting to V_{in} are disabled. At the 1st sampling phase, both DAC top- and bottom-plates are reset to V_{cm}, after that the sampled signal is quantized normally. In the next sampling, the DAC top-plate stops being reset to V_{cm}, while the charge pump circuit is activated, which generates a small voltage step above the previous sampled value. The transition level of ϕ_{c2} is from V_{dd} to V_{cm} and by enabling the current source device for a short duration t_c (150 ps), the voltage step can be controlled sufficiently smaller than 1/2LSB. According to 100 runs of the Monte-Carlo process and mismatch simulation at 27°C, the 3σ step size variation is around 32% with a mean of 158µV. It guarantees that the worst case step size approximates 0.3 LSB under 12-bit resolution. Once the conversion is completed the bottom-plate switches are reset, restoring the DAC output to its sampled value before the next incoming sampling. Consequently, the charge-pump circuit generates a staircase testing signal. As the DAC output increases in Fig. 4 (c), the V_{DS} of the current source decreases leading to the reduction of the voltage step. However, it is not problematic, as the testing signal does not need a good linearity, thus the voltage step essentially smaller than 1/2LSB is enough to sense the missing codes. Under process variations, the TSG range is guaranteed larger than 18.75 mV while runs for 192 cycles with minimum step size, and it stops immediately once detecting the missing codes. The gain error estimation is based on 12-bit outputs, while the final ADC output is 11-bit.
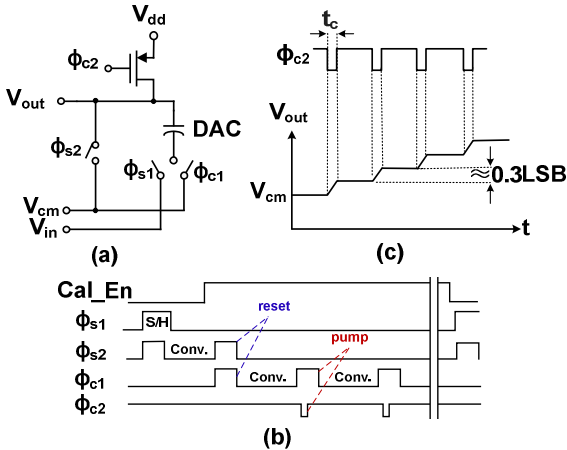

Fig. 4. (a) Charge pump circuit for the DAC; (b) Control timing diagram for calibration; (c) Signal behavior at the DAC output.

B. Digital Calibration

Fig. 5 shows the block diagram of the MCD calibration. The Cal_En signal activates the charge-pump circuit and disables the normal sampling in the ADC. The data processing block consists of several registers and arithmetic units. The registers store two adjacent outputs (D[t] and D[t-1]) and pass them to the subtractor to check whether the difference Δ is larger than 2. Considering the noise that may affect the conversion accuracy the detection threshold is set to 2. If it senses Δ >2, the TSG is reset and the number of missing codes $N_{mc}= Δ-1$ is stored. To average the noise, the above operation repeats 8 times. Once the counter arrives to 8, the calibration stops and the ADC returns to its normal sampling. One benefit of the proposed MCD calibration is the algorithm shown in (3)-(5) can be simplified to:

$$D_{cal,out} = \sum_{j=0}^{i+k} 2^j B_j - \overline{N_{mc}} * \sum_{j=1}^{k} 2^{j-1} B_{i+j} \qquad (6)$$

Now, the average number of missing code ($\overline{N_{mc}}$) instead of β is multiplied to the leading bits, which totally removes the β estimation circuits. The power consumption of the calibration block is 0.12 mW at 80 MHz from a 1.2 V supply. The digital gate count of the proposed calibration algorithm is ~0.5 k with an area of 0.004 mm². Compare with HBRM, our proposed calibration saves around 90% digital hardware thanks to the algorithm in (6) with omitting the β estimation.
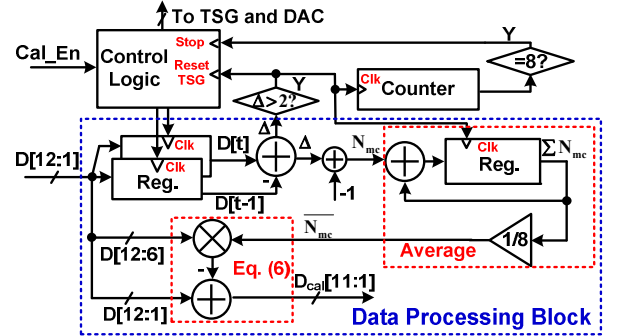

Fig. 5. Diagram of MCD calibration.

V. MEASUREMENT RESULTS

The proposed 11-bit SAR ADC with on-chip MCD calibration was fabricated in 65 nm CMOS process with MOM capacitors. Fig. 6 shows the die microphotograph; the active area is 0.015 mm² including the calibration circuits. Fig. 7 shows the measured FFT at a DC and a Nyquist input under a sampling rate of 80 MS/s. Before calibration, spurs are widely spread over the spectrum, limiting the SNR to 55.7 dB due to the gain mismatch between the MSB and LSB array. After calibration the spurs are removed and the SNR is improved to 63 dB. The SFDR is slightly improved by 1.5 dB, since the odd harmonics caused by the DAC mismatches dominate. The SNDR drops by 2.1 dB at a Nyquist input frequency. The measured dynamic performance before and after calibration are shown in Fig. 8 where the SNDR remains above 60 dB up to a 59 MHz input frequency. Fig. 9 shows the measured static performance before and after MCD calibration. The value of C_a
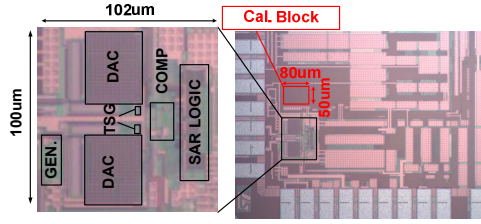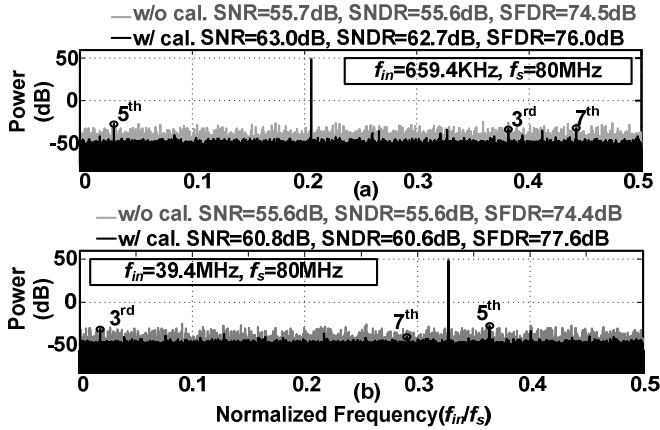
Fig. 6. Die microphotograph of the ADC.

Fig. 7. Measured FFT of the digital output (decimated by 25) at (a) low-frequency input and (b) Nyquist input.
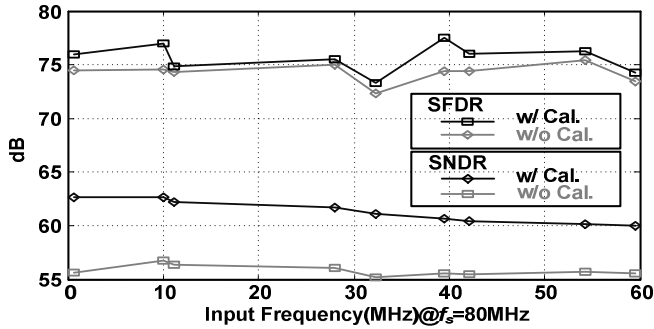

Fig. 8. Measured dynamic performance of the SAR ADC without and with calibration for different input frequency.
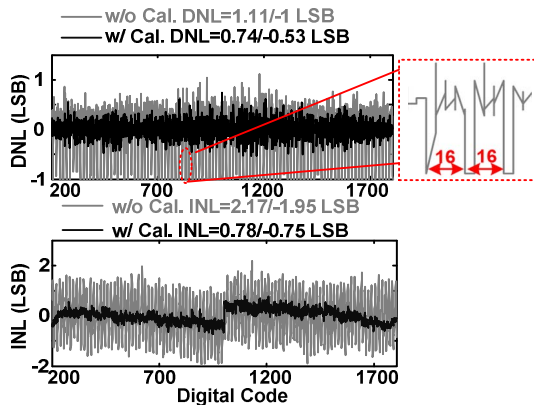

Fig. 9. Measured static performance of the SAR ADC before and after MCD calibration.

is enlarged by 1.45 times larger than its ideal value that can theoretically compensate the C_{PB} with a maximum value of 45% of the total capacitance in the LSB array. According to post-layout simulations the output contains 3 missing codes in every interval of 2^4 codes, while due to process and mismatch the

Table I SUMMARY OF PERFORMANCE AND BENCHMAR

	ISSCC '14 F. van der Goes	JSSC '15 Y. Zhou	ASSCC '16 K.H. Chang	ESSCIRC' 16 J.Y. Zhong	This work
Architecture	Pipelined-SAR	Pipelined-SAR	SAR	Pipelined-SAR	SAR
Technology(nm)	28	40	40	65	65
Resolution(bit)	14	12	12	12	11
Sampling Rate(MS/s)	80	160	150	180	80
Supply Voltage(V)	1.0	1.1	0.9	1.2	1.2
Power(mW)	1.5	4.96	1.5	6	1.4
ENOB @ Nyquist	10.7	10.5	9	9.8	9.8
SFDR(db) @ Nyquist	74	84.9	63.5	67.2	77.6
Area(mm^2)	0.137	0.042	0.04	0.068	0.015
FoM @ Nyq.(fJ/conv.step)	11.5	20.6	18.9	36.7	20
Calibration	Off-chip	Off-chip	Off-chip	On-chip	On-chip

measured DNL contains a maximum of 2 missing codes per-region before calibration. As the measured outputs is 11-bit instead of 12-bit, we normalized the region here to 2^4 codes. The missing codes are all removed after calibration, where the DNL and INL are improved to 0.74/-0.53 and 0.78/-0.75 LSBs, respectively. The total power consumption is 1.4 mW at 80 MS/s from a 1.2 V supply, where the analog and digital blocks (including calibration) consume 660 and 740 µW, respectively, leading to a FoM of 20 fJ/conv.-step @Nyquist. Table I summarizes and compares the overall measured performance with state-of-the-art SAR-type ADCs with similar specifications. This work exhibits a competitive FoM targeting high conversion accuracy with calibration and testing signal generator implemented on-chip.

VI. CONCLUSIONS

This paper reported a MCD calibration to correct the gain error in a bridge-DAC of a SAR ADC. The solution estimates the gain error by sensing the missing codes in a small range of the digital output simplifying the algorithm and allowing the implementation with less digital overhead. Moreover, as the calibration detects the missing codes releasing the constraint on the linearity of the testing signal, a simple charge-pump circuit is used to generate a monotonic signal for testing purposes that removes the calibration reliance on the type of input signal. The MCD calibration was verified on-chip in an 11-bit SAR ADC and the measured results demonstrate the effectiveness of the calibration.

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