11.5 A 2-Phase Soft-Charging Hybrid Boost Converter with Doubled-Switching Pulse Width and Shared Bootstrap Capacitor Achieving 93.5% Efficiency at a Conversion Ratio of 4.5

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High conversion ratio (*CR*) boost converters are in high demand for LED backlighting in a multitude of products including smartphones and tablets. The conventional boost (CB) converter with high *CR* has large inductor current ripples, thus requiring high-quality inductor to mitigate the efficiency degradation. Meanwhile, a narrow switching pulse width in the high *CR* converters limits the switching frequency (f_{SW}). The hybrid converter with flying capacitors (C_F) can widen the pulse width for the same *CR*, but hard-charging has been an issue in previous works [1-3].

Figure 11.5.1 shows the proposed 2-phase soft-charging hybrid boost (HB) converter, consisting of two branches. Each branch has an inductor L_1 (L_2), a flying capacitor C_{F1} (C_{F2}), and three switches M_1 (M_2), M_3 (M_4), M_5 (M_6). It operates in three states. In state-1, M_1, M_3, M_5 are on while M_2, M_4, M_6 are off. L_1 is energized, and current of L_2 (I_{L2}) decreases with a slope of α, and is divided into two parts, I_{C1} that flows into C_{F1} and I_{C2} that flows into the output (C_{F2} in series with output capacitor C_O). Considering $C_O >> C_{F2}$, I_{C1} and I_{C2} are almost equal but they have opposite polarities, hence, both have a slope of $\alpha/2$. The status reverses in state-2. In state-3, M_1 and M_2 turn on while others turn off, hence, L_1 and L_2 are charged and there would be no change on C_{F1} and C_{F2}. The proposed HB works with state-1⟶state-3⟶state-2⟶state-3 periodically.

There are several benefits for this scheme. 1) The 2-phase operation reduces input and output ripples. 2) Since there is no direct charge transfer between C_{F1} and C_{F2}, nor between C_F and C_O, soft-charging is achieved. 3) Only M_3 and M_4 need to sustain a high V_{DS} that is V_0 in state-2 and state-1, whereas other switches can use lower voltage devices as their V_{DS} stresses are only $V_0/2$, reducing the switching losses and silicon area. 4) Due to C_{F1} and C_{F2} charge balancing, V_{C1} and V_{C2} should be $V_0/2$, and $CR=2/(1-D)$, where D is the duty cycle. Here, for the 2-phase operation, D should be larger than 0.5, and thus the minimum *CR* is four. Comparing to the conventional boost, we double the switching pulse-width for the same *CR*, allowing a higher f_{SW}.

Figure 11.5.2 presents the schematic of the proposed HB. We use NMOS switches to reduce the silicon area and gate capacitances. A separate gate-drive voltage V_{DR}=5.5V is used for low conduction losses. M_3 and M_4 are isolated devices with a V_{DS} rating of 20V, while others use 10V devices. Due to the floating sources of $M_{3\text{-}6}$, their gate-drive supplies V_{DR34}, V_{DR5}, V_{DR6} should be bootstrapped. A type-III compensation network is used, in which the error between V_0 and V_{REF} is filtered and then compared with a saw-tooth wave working at $2\times f_{SW}$. The following 2-phase generator divides the compared output by two, and reconstructs it into the PWM control signals for each phase at f_{SW}.

Figure 11.5.3 illustrates the schematic of the bootstrap generator and the gate-drive scheme. The deadtime DT_1 is added between the control signals S_1 and S_4 (S_2 and S_3), to prevent the feedthrough from V_3(V_4) to the ground. For the bootstrap capacitors of M_3 and M_4, they should be several times larger than the gate capacitance. For a 2-phase CB (2P-CB), two bootstrap capacitors may be required for independent gate-drive supplies, doubling the area. However, considering that M_3 and M_4 only turn on alternatively in the proposed HB, the bootstrap capacitor (C_{34}) can be shared without doubling the area. C_{34} can drive M_3 and M_4 in state-1 (at t_1) and state-2 (at t_3), respectively, and be charged by V_{DR} in state-3 (at t_2 and t_4), through an active diode D_{34} controlled by S_A. The interleaved charging of M_3 and M_4 is obtained by connecting the bottom plate of C_{34} to either V_1 or V_2 through the switches M_B or M_C. Another deadtime, namely, DT_2 is added between S_B and S_C, to prevent V_1 and V_2 feedthrough. For the gate-drive supplies V_{DR5} and V_{DR6} of M_5 and M_6, they should be charged by a voltage source $V_0/2+V_{DR}$ first, then be bootstrapped to V_0+V_{DR} in state-1 or state-2. Coincidently, V_{DR34} is bootstrapped to $V_0/2+V_{DR}$ in both state-1 and state-2, and thus can be reused to charge the bootstrap capacitors C_5 and C_6. In state-1, C_6 is charged from V_{DR34} through an active diode D_6, while C_5 discharges to M_5 (at t_1), and vice versa in state-2 (at t_3). As V_{DR34} is reused to charge C_5 and C_6, an additional drop on V_{DR34} will occur at t_1 and t_3. However, thanks to the proposed topology, M_5 and M_6 are relatively small since they have low voltage stress and small high-side (HS) currents (to be explained next). This reduces both the sizes of C_5 and C_6, and the V_{DR34} drop.

Figure 11.5.4 normalizes the power losses of the proposed HB to those of a 2P-CB, with *CR*=4.5. We choose both the same inductor DCR and switch on-resistance (R_{ON}) for the two topologies. However, all the switches in 2P-CB should use 20V devices. The calculated inductor DCR loss in the proposed design is lower than that of a 2P-CB, because the ripple of I_L decreases with a smaller inductor voltage swing. This relaxes the inductor DCR requirement, reducing the inductor volume and cost. Thus, in the proposed design, we use 3.3μH inductors in 3010 package with a DCR of 166mΩ, instead of a 4020 package with a DCR of 38mΩ. Although we use two HS switches M_3(M_4) and M_5(M_6) in each phase, the summed conduction loss is still lower since they only conduct half of I_L with a reduced current ripple. However, the conduction loss of the low-side (LS) switches M_1 and M_2 is thereby higher. Since the HS root-mean-square (RMS) current is much smaller than that of the LS, smaller HS switches can be used. For the switching losses, all the switches benefit from the halved V_{DS} swing, while the low-stress switches further enjoy a reduced gate charge (Q_G). Thus, the switching losses of M_1, M_2, M_5, M_6 are only 0.11 times, and M_3, M_4 are 0.56 times that of the 2P-CB. The gate loss of LS decreases to 0.26 times from the C_{GS} reduction of the low-stress device, while that of the HS slightly increases by 1.26 times as a sum of two switches.

Considering the mismatches on L_1 and L_2, the inductor currents can be automatically balanced, because the error from mismatch is fed-back through the C_{F1} and C_{F2}, ensuring the charge balancing (Q_1=Q_2) and removing the conventional phase currents balancing. For the mismatches on the C_{F1} and C_{F2}, I_{C1} and I_{C2} will be different, but the ΔV_{C1} and ΔV_{C2}, caused by I_C discharging from the respective C_F, will compensate each other and leave V_0 unchanged. The mismatch effects on *CR* are also minor, as $R_L\times(C_{F1}+C_{F2})$ can be much larger than $1/f_{SW}$, where R_L is the load resistance.

Figure 11.5.7 shows the chip micrograph of the proposed HB that is fabricated in a 0.35μm HV CMOS process, where the core area occupies 1.15mm×0.75mm. M_1 and M_2 have a large size to accommodate a high RMS current. We use f_{SW}=2MHz to balance the conduction and switching losses with smaller passives. C_0=10μF and C_{F1}=C_{F2}=0.47μF, and their ESRs can also be relaxed because of the reduced HS RMS currents. Figure 11.5.5 plots the steady-state waveforms of V_1, V_2 , I_{L1}, I_{L2}, and V_0, where V_{IN}=4V, *CR*=5, and I_0=100mA. A 20V V_0 is obtained, with 15mV ripples. The measured peak efficiency is 93.5% at V_{IN}=4.2V, *CR*=4.5, and I_0=100mA, and is 91.7% at V_{IN}=3.3V, *CR*=6, and I_0=75mA. The efficiency drops when *CR* increases, due to the more conduction losses on M_1 and M_2. We estimate the power loss break-down, where the LS conduction loss is the largest portion as predicted. Figure 11.5.6 shows the performance comparison table. From the reduced voltage stress and shared M_3/M_4 bootstrap capacitor, we have achieved a small area. Also, we have reached higher efficiencies than the CB at high *CRs*, because of the reduced RMS currents, reduced switching losses, and the doubled pulse-widths. As compared to the previous HBs, this work prevents C_F hard charging, and thus it achieves higher efficiency with smaller C_F value. The efficiency can be improved by further optimizing transistor sizing, as in the current form the conduction loss dominates.

References:

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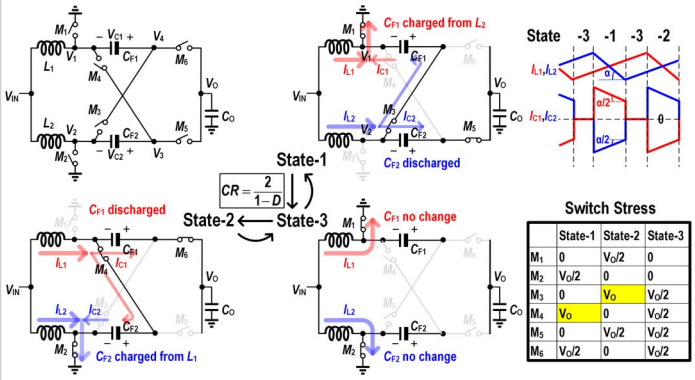


	State-1	State-2	State-3
M_1	0	$V_O/2$	0
M_2	$V_O/2$	0	0
M_3	0	V_O	$V_O/2$
M_4	V_O	0	$V_O/2$
M_5	0	$V_O/2$	$V_O/2$
M_6	$V_O/2$	0	$V_O/2$

Figure 11.5.1: Topology and working principle of the proposed 2-phase HB (left), its current profiles (top right), and the V_{DS} stress of all the switches (bottom right).

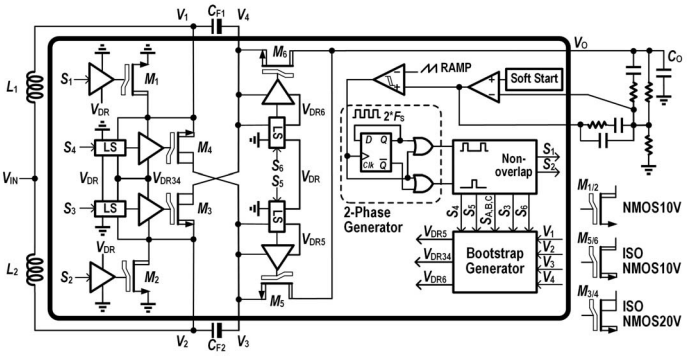


Figure 11.5.2: Schematic of the proposed 2-phase HB converter.

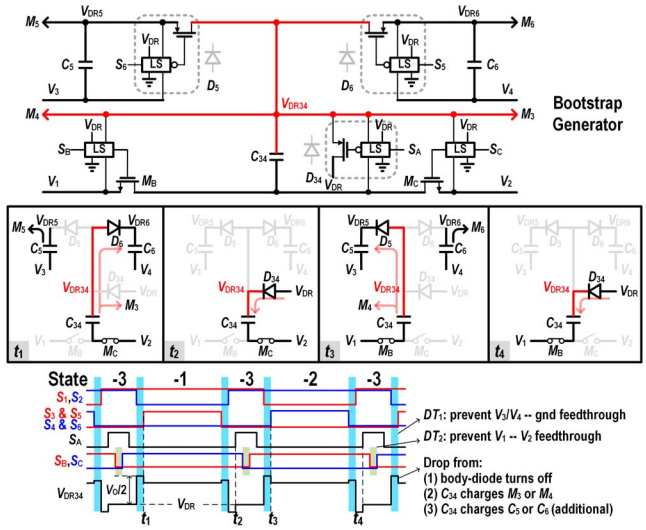
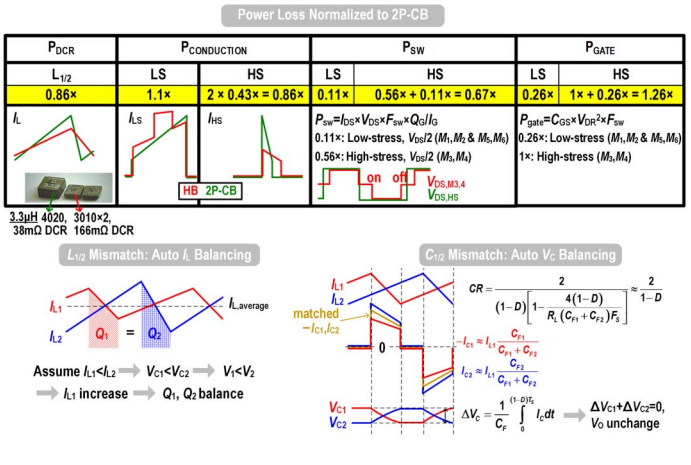


Figure 11.5.3: Schematic of the bootstrap generator (top), Working principles (middle), and timing diagram (bottom) of the bootstrap gate-drive scheme.



P_{DCR}	$P_{CONDUCTION}$		P_{SW}		P_{GATE}	
$L_{1/2}$	LS	HS	LS	HS	LS	HS
0.86×	1.1×	2 × 0.43× = 0.86×	0.11×	0.56× + 0.11× = 0.67×	0.26×	1× + 0.26× = 1.26×
I_L	I_{LS}	I_{HS}	$P_{sw}=I_{DS}\times V_{DS}\times F_{sw}\times Q_G/I_G$ 0.11×: Low-stress, $V_{DS}/2$ (M_1,M_2 & M_5,M_6) 0.56×: High-stress, $V_{DS}/2$ (M_3,M_4)		$P_{gate}=C_{GS}\times V_{DR}^2\times F_{sw}$ 0.26×: Low-stress (M_1,M_2 & M_5,M_6) 1×: High-stress (M_3,M_4)	

Figure 11.5.4: The power loss normalized to the 2P-CB (top) at *CR*=4.5. The auto I_L balancing with L_1 and L_2 mismatch (bottom left), and V_C balancing with C_{F1} and C_{F2} mismatch (bottom right).

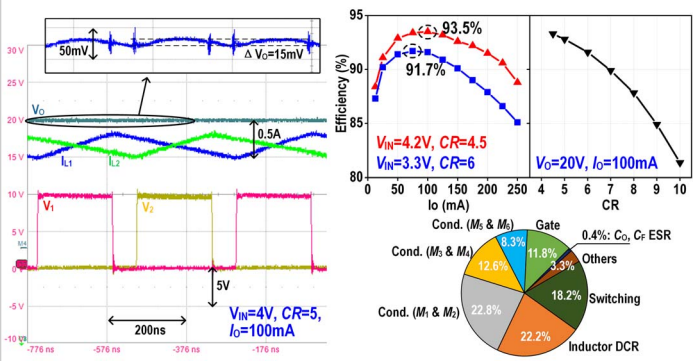


Figure 11.5.5: Measured transient waveform of the proposed HB, when V_{IN}=4V, *CR*=5, I_O=100mA (left). Measured efficiencies versus I_O and *CR* (top right). Calculated power loss breakdown when V_{IN}=4.2V, *CR*=4.5, I_O=100mA (bottom right).

	TI TPS61181A[4]	2014 JSSC [5]	2018 ISSCC [1]	2019 TPE [2]	This work
Process	n.a.	0.35um BCD	0.18um BCD	n.a.	**0.35um CMOS**
Area	n.a.	1.86mm^2	6mm^2	8mm^2	**0.86mm^2**
Topology	Conventional boost	Conventional boost	Hybrid boost	Hybrid boost	**Hybrid boost**
Input Voltage	4.5-27V	2.7-4.5V	2-4.2V	6-18V	**2-4.4V**
Output Voltage	4.5-38V	8V	3-5V	12-50V	**9-20V**
Load Current (I_L)	20-120mA	20-300mA	10-800mA	70-100mA	**10-250mA**
F_{SW}	1MHz	1MHz	1MHz	Max. 820kHz	**2MHz**
Multi-Phase	No	No	No	No	**Yes**
CR	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{2-D}{2-2D}$	$\frac{3-D}{1-D}$	**$\frac{2}{1-D}$**
Inductor L (DCR)	10μH (53mΩ)	10μH (11mΩ)	4.7μH (200mΩ)	18μH (n.a.)	**2×3.3μH (166mΩ)**
Output Capacitor	4.7μF	10μF	10μF	10μF	**10μF**
Flying Capacitor	n.a.	n.a.	10μF	2×260μF	**2×0.47μF**
Soft Charging	n.a.	n.a.	No	No	**Yes**
Peak Efficiency @ (CR)	94% (CR=1.67)	90% (CR=2.16)	95.2% (CR=1.4)	92% (CR=2.5)	**93.5% (CR=4.5)**
Effieicncy @ CR=6 (I_L=)	87.9% (I_L=70mA)	n.a.	n.a.	88.2% (I_L=70mA)	91.7% (I_L=75mA)

Figure 11.5.6: Performance comparison with the state-of-the-art.

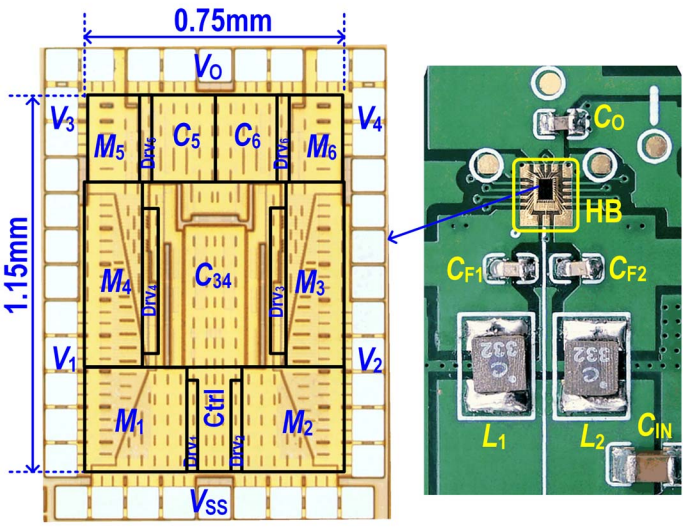


Figure 11.5.7: Chip micrograph and PCB of the proposed HB.

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