An ELD Tracking Compensation Technique for Active-RC CT ΣΔ Modulators

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***Abstract*— Excess Loop Delay (ELD) induced feedback DAC nonideality is a dominant factor causing error in the transfer function of CT ΣΔ modulators and eventually leading to instability. This paper will present a novel technique which aims to track the amount of excess loop delay, and compensate by using digital logic elements and an RC feedback network. A 2nd order CT ΣΔ modulator with 1-bit DAC was built at transistor-level in 65nm CMOS to demonstrate the efficiency of the method. The Cadence simulation results show that, by using the proposed technique, the modulator can track the ELD up to 50% of the clock period duration and compensate it, leading to 69.2dB SNDR when compared with the ideal value of 70dB SNDR.**

I. INTRODUCTION

Because of the benefits of large signal bandwidth, low power consumption, small silicon area, and also inherent anti-aliasing function, the Continuous-Time (CT) ΣΔ modulator has been widely used in broadband telecommunication systems. The integrator is the core component of both CT and Discrete-Time (DT) modulators, and its performance may significantly affect the performance of the overall modulator [1]. To implement the integrators in CT ΣΔ modulators, there are mainly three types of architectures: active RC, gm-C and MOSFET-C. Although the active RC integrator consumes more power, it is usually the most commonly used one compared with the other two structures as its higher linearity [2]. Besides, it can provide a wider range of signal swing with deep-submicron technologies. On the other hand, in contrast to its DT counterpart, the CT ΣΔ modulator is very sensitive to ELD, which degrades the system performance significantly [1]-[2]. Non-Return-to-Zero (NRZ) feedback is more sensitive to the ELD effect since it will shift a part of the feedback pulse into the next clock cycle. A certain shift amount of the feedback pulse will increase, mathematically, the order of the transfer function. This leads to the change of the Noise Transfer Function (NTF), and finally may cause the instability of the modulator. Due to the serious effect of ELD in the CT ΣΔ modulator with NRZ feedback, several compensation methods have been proposed and discussed in particular in [1]-[3] and [4]-[5]. Compared with the existing compensation methods, this paper will propose a novel compensation scheme to track ELD when NRZ feedback is used, and then the delay amount will be compensated correspondingly by using digital logic elements and an RC feedback network. The advantages of using this technique are: 1) simple implementation of digital logic elements; 2) compensation amount of ELD is tracked synchronously on a real-time modulator.

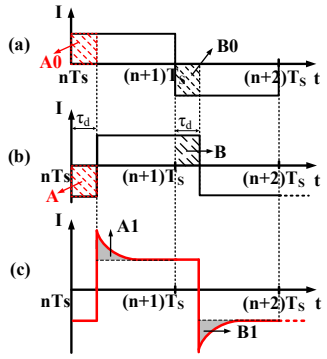

Fig.1 NRZ feedback with a) ideal case b) certain amount of delay τ_d c) the proposed compensation technique

The issues of ELD for NRZ feedback DAC in a CT ΣΔ modulator will be briefly reviewed in section II. Section III will introduce the working principle of the proposed compensation technique for the CT ΣΔ modulator. Section IV will present the simulation results, and the conclusions will be drawn in section V.

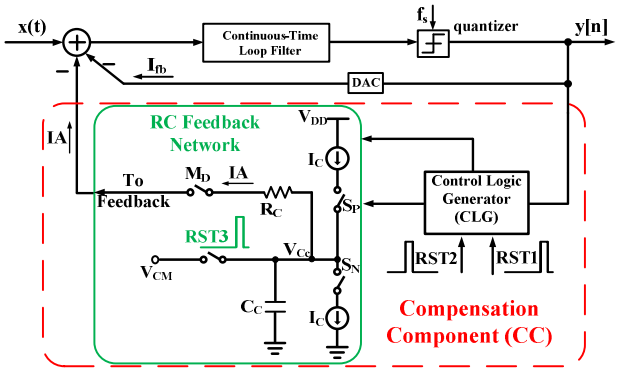

Fig.2 Block diagram of the proposed ELD tracking compensation technique

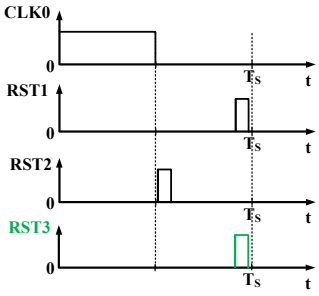

Fig.3 Clock and reset signals for Compensation Component (CC).

II. ELD Issues For NRZ Feedback In CT ΣΔ Modulator

As discussed above and in [1], [4]-[5], NRZ feedback is more sensitive to ELD. The proposed compensation method is based on the NRZ feedback. Fig.1 shows the NRZ DAC pulse in different cases: a) ideal case, b) with a certain amount of delay τ_d and c) with the proposed compensation technique. Compare waveforms in Fig. 1 (b) with the ideal case, the positive area A0 is lacking from the first clock cycle instead of the negative area A; on the other hand, in the subsequent clock cycle, there is a redundant positive area B. A0 and A are equal, as well as B0 and B, since 1-Bit DAC is used. In order to compensate the delay effect, grey areas A1 and B1, in Fig. 1 (c), should be the double of A0 and B0, respectively. The working principle of the proposed ELD tracking compensation technique implies the determination of the delay amount, and after that the lacking/redundant area is added /subtracted by A1/B1. A similar principle is also used in [4]-[5], but the advantages of this technique is its simple circuit implementation and real-time ELD records. Besides, the time domain equivalent theory from [6] will also be used to determine the coefficient of the compensation path.

III. Proposed ELD Tracking Compensation Method

The block diagram of the proposed compensation technique is illustrated in Fig. 2. Compare with a traditional ideal 2nd order CT ΣΔ modulator, it has an additional Compensation Component (CC). It contains the Control Logic Generator (CLG) and the RC feedback network. CLG controls the PMOS/NMOS switches S_P/S_N in the RC feedback network to charge/discharge capacitor C_C, and then the

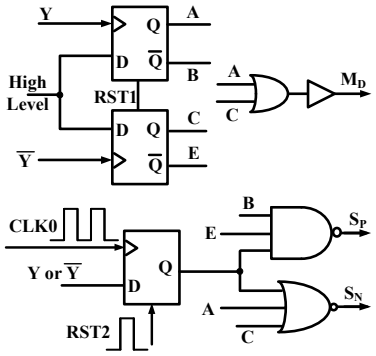

Fig.4 Implementation of the Control Logic Generator (CLG) with digital logic.

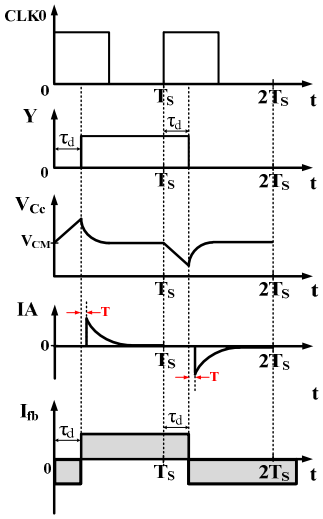

Fig. 5 Illustration of the proposed ELD tracking compensation technique.

lacking/redundant feedback amount due to delay will be stored in the capacitor C_C. At the same time, CLG also controls the compensation amount back to the main circuit through the switch M_D. Fig. 3 represents the clock and the reset signals of the compensation component. The signal CLK0 is the quantizer sampling clock. RST2 is used to reset the switches S_P and S_N, and RST3 resets the charge restored in capacitor C_C. Fig. 4 exhibits the implementation of the CLG and Fig. 5 illustrates the overall working principle of the proposed ELD compensation technique.

A. Compensation Component - Working Principle

In Fig. 5, I_{fb} is the current of the traditional CT ΣΔ modulator feedback path (as in Fig. 2). The working principle of the whole ELD tracking compensation technique can be disassembled into the following conditions (assuming for example that Y, the input of CC, has an original value of 0)

Referring to the CLK0 waveforms of Fig.5, the quantizer output Y and the feedback current I_{fb} have a delay of τ_d. Then there is a lack amount within the period $[0,T_S]$ and a redundant amount in the subsequent period. Being the task to add back the lack amount and subtract the redundant amount in each period. According to Fig. 4, the CLG component will turn on

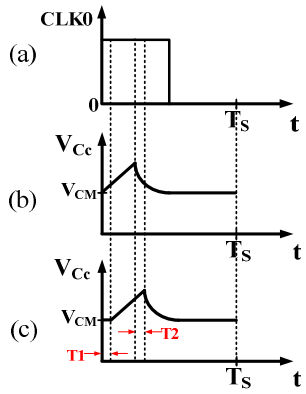

Fig.6 Waveforms of a) CLK0 b) theoretical V_{Cc} c) V_{Cc} with delay considered.

the PMOS switch (S_P in Fig. 2), and turn off both the NMOS and the M_D, switches. Besides, the voltage V_{Cc} will increase linearly as in Fig. 5, and the charge lack of the feedback current (due to ELD) will be stored in C_C.

At τ_d, the signal Y is rising from 0 to 1 and both PMOS and NMOS switches turn off. But, since the switch M_D turns on, the lack amount due to the ELD effect will be compensated.

At T_S, according to the assumption from Fig. 5, there is no change of Y, the PMOS switch turns off and the NMOS switch turns on. According to the current direction through the capacitor C_C, the voltage V_{Cc} drops from V_{CM} to a lower level.

At $T_S+\tau_d$, the delayed signal Y changes from high to low and both PMOS and NMOS switches turn off. Since the voltage V_{Cc} is smaller than V_{CM}, there is a voltage difference between V_{CM} and V_{Cc}. Hence, there is current through the capacitor to subtract the redundant amount from the main circuit.

Moreover, other conditions may imply that there are no signal changes in two consecutive periods nT_S and $(n+1)T_S$. In that case, one MOS switch is also opened (either PMOS or NMOS) from time nT_S to $(0.5+n)T_S$ to charge/discharge the capacitor C_C. Hence, the voltage V_{Cc} also changes. Being, the only difference that at the time instant $(0.5 + n)T_S$, the signal in the PMOS or NMOS switches will be reset by RST2 signal. Besides, the unaltered Y imposes the switch M_D to turn off; and in order to allow the compensation component to work properly, RST3 sets V_{Cc} equal to V_{CM} for the forthcoming period, as in Fig. 3.

B. Compensation Component - Delay Issues

From Fig. 4, it can be extracted that the logic elements will induce extra delay which may significantly reduce the performance, especially in high speed CT ΣΔ modulators. The delay will cause two effects: 1) the amount of charge Q stored in capacitor C_C may change, and, 2) the position of RC feedback pulse IA can also vary. The analysis of both effects will be covered in detail separately.

Firstly, analyzing the charge amount, and according to the previous introduction, during the delay τ_d, there is current I_C to charge/discharge capacitor C_C, which is controlled by the switch S_P/S_N. The charge Q amount in the capacitor is only

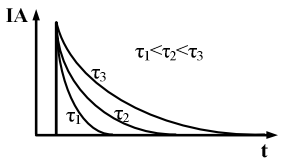

Fig.7 Current IA of the RC feedback network for different values of the time constant τ.

related with the time interval that starts with the turning on of the switch S_P/S_N, to charge C_C, and the time when the switch turns off. Then, it can be defined that the response time for the trigger signal to turn on switch S_P/S_N as delay T1 (as depicted in Fig. 6), and T2 is the delay caused by switch S_P/S_N to turn off. If T1 and T2 are equal, the charge Q equals to the theoretical value; if not, there will be an offset, which will imply the compensation failure. From Fig. 4, T1 is due to the response time of a D Flip-Flop and a NAND/NOR gate with 3 inputs. And the cause of T2 is identical with T1. Hence, T1 and T2 are definitely equal. Then, the charge in capacitor C_C (considering the delays T1 and T2) in CLG is obviously equal to the theoretical value, implying that both delays T1 and T2 do not affect the modulator's performance.

Secondly, there is a delay T due to response time of the switch controller M_D. From Fig. 5, it can be deducted that the feedback current waveform is shifted due to the delay T. The behavior of the current IA of the RC feedback network for different values of the time constant τ is depicted in Fig. 7, leading to different discharge times of the capacitor. When the value of the time constant is larger, the charges are released at a slower pace. Based on this, even though the delay T exists, the performance will not change if the charge in capacitor C_C can be released almost completely. Meaning that, in order to maintain the performance, the time constant τ of the RC network should be carefully chosen, namely: 1) if R_C is too large, the charge on capacitor C_C may not be released completely. 2) If R_C is too small, though the charge on capacitor C_C can be released completely, it may imply a very large peak value of the current. Next section will introduce in detail a design example with adequate choices of R_C and C_C.

IV. Simulation Results

Based on the proposed architecture of Fig. 2, a 2nd order, single-bit, low-pass CT ΣΔ modulator was modeled, and designed in 65nm CMOS, with Cadence design tools to further demonstrate the efficiency of the technique. The sampling rate of the designed modulator is 250MS/s; the input bandwidth is 2MHz, corresponding to the standard of 3G WCDMA receivers, and the OSR is 64. The amplitude of the input signal is P_{in}= –4.43dBFS. The transformed CT coefficients were scaled down to guarantee that the signal swing will not reach the saturation level of the loop filter. Furthermore, according to the time equivalent theory from [6], the shape of the waveform of the CT outputs within the [0, 1] period is irrelevant; the value at the sampling time t=nT mattered. After calculation, a proposed compensation path to the second integrator is needed, and the compensation current I_C should be 3 I_{fb2} (feedback current of the second integrator in an ideal second order CT ΣΔ modulator). Referring to the

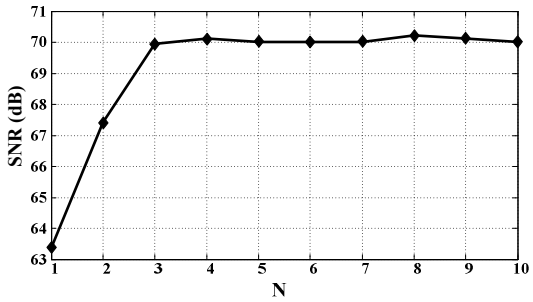

Fig. 8 Settle error tolerance of the RC feedback network.

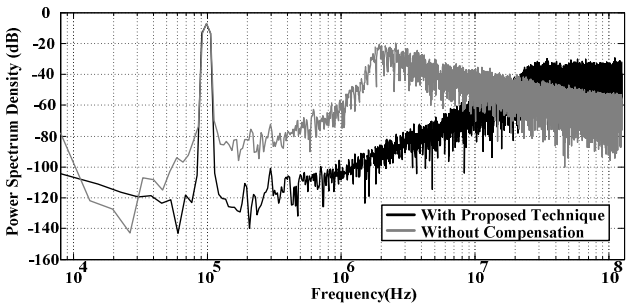

Fig. 9 Comparison of simulation results for 2 different cases when there is 50% Ts delay in the quantizer.

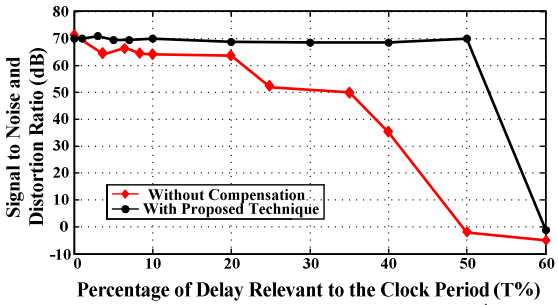

Fig. 10 Simulation results for system sensitivity to ELD in a 2nd order CT ΣΔ modulator with or without the proposed compensation technique.

compensation components show in Fig. 2 and Fig. 4, the value of the time constant τ composed by R_C and C_C should be determined. From Fig. 7 and the definition of RC feedback network (that has an exponential expression) the charge in the capacitor C_C cannot be completely released. Hence, the settle error tolerance should be obtained from probability statistics. In order to get the suitable time constant τ, the settle error tolerance can be defined by:

$$N=\frac{T_S-\tau_d}{\tau} \quad (1)$$

Equation (1) shows that larger N leads to smaller τ. In the current design, the modulator is supposed to have the ability to track and compensate the delay τ_d up to half cycle of the sampling period. There are two extreme delay cases in the modulator: 1) there is no delay, then τ_d=0; 2) there is a delay up to 50% of T_S, then τ_d =0.5T_S. Hence, if an RC network (which can release the charge almost completely) is adequate for a modulator that contains half cycle delay, then it would also be suitable for the case when the delay amount is less than half cycle. The settle error tolerance of the RC feedback network is shown in Fig. 8. When N is larger than 3, the performance of the modulator is stable, and it will nearly reach the ideal case. Due to the relation between N and τ (larger N leads to smaller τ), small R_C with fixed C_C will imply good performance (excluding the effect of high peak current). This result really confirms the results presented above. Then, for this case and referring to Fig. 8, N=4 is chosen, i.e. $\tau=5\times10^{-10}$. When C_C with 1fF is selected, R_C is 500Ω. After simulation, the modulator exhibits a 69.2dB SNDR, being 70dB the ideal case. On the other hand, the power spectrum density (PSD) of two different cases is depicted in Fig. 9. Simultaneously, the system sensitivity to ELD in a 2nd order CT ΣΔ modulator with the proposed technique is presented in Fig. 10, showing a loop delay tolerance of up to 50% of clock cycle.

V. CONCLUSIONS

This paper presents a novel technique to compensate the effect of ELD in CT ΣΔ modulators. It uses only a few digital logic elements to track the loop delay amount, and then compensates either the lacking charge back or subtracts the redundant charge by using an RC feedback network. The proposed compensation method can be easily demonstrated at circuit level leading to half clock cycle loop delay toleration in a 2nd order CT ΣΔ modulator with NRZ feedback. Simulated results in 65nm CMOS show that a loop delay up to 50% of clock cycle can be tracked and then completely compensated, with a final SNDR of 69.2dB close to the ideal. By contrast, the CT ΣΔ modulator with a similar delay amount but without ELD compensation is unstable, further demonstrating the effectiveness of the proposed technique.

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