Hardware and Software Design of A Low DC-link Voltage and Wide Compensation Range Thyristor Controlled *LC*-coupling Hybrid Active Power Filter

Lei Wang[1], Chi-Seng Lam[1,2] and Man-Chung Wong[1,2]
1 - Department of Electrical and Computer Engineering, Faculty of Science and Technology, University of Macau
2 - State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau, China
E-mail: cslam@umac.mo / C.S.Lam@ieee.org

***Abstract*-This paper presents the hardware and software design of an 110V-5kVA three-phase three-wire thyristor controlled *LC*-coupling hybrid active power filter (TCLC-HAPF). Unlike the active power filters (APFs) and the hybrid active power filters (HAPFs), the TCLC-HAPF can operate at a low dc-link voltage with wide compensation range. In this paper, the design of the thyristor and IGBT drivers, the transducer with signal conditioning circuits, and the software of digital control system of the TCLC-HAPF experimental prototype is presented. Finally, the performance of the designed TCLC-HAPF hardware prototype is verified by experimental results.**

***Index Terms*—Current harmonics, hybrid active power filter (HAPF), reactive power, thyristor controlled LC-coupling hybrid active power filter (TCLC-HAPF)**

I. INTRODUCTION

IMPLEMENTATION of power filters is one of the solutions for current quality problems such as low power factor, harmonic pollution and resonances problem, etc. In 1960s, thyristor based Static Var Compensators (SVCs) were implemented to dynamically compensate reactive powers [1]. However, SVCs have many inherent problems including resonance problem, slow response, poor harmonic compensation ability and self-harmonic generation. Afterwards, the remarkable concept of active power filters (APFs) was proposed for power quality compensation [2]-[4]. However, APFs require high dc-link voltage levels, which drive up their cost. Later on, a low-cost *LC*-coupling hybrid active power filter (HAPF) was proposed with low dc-link voltage [5]-[7]. Unfortunately, the HAPF has a narrow compensation range. When the HAPF operates outside its compensation range, it loses its low inverter rating advantage. In 2014, S. Rahmani in [9] proposed a thyristor controlled *LC*-coupling hybrid active power filter (TCLC-HAPF) topology which has the characteristics of a much wider compensation range and smaller dc-link voltage for compensation. However, the hardware realization of TCLC-HAPF is not included in [9]. In this paper, the hardware and software design including the thyristor and IGBT drivers, the transducer with signal conditioning circuits, and the software of digital control system of an 110V-5kVA TCLC-HAPF experimental prototype is presented. And the validity of the designed TCLC-HAPF prototype is verified by experimental results.

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II. CIRCUIT CONFIGURATION OF THE TCLC-HAPF

As shown in Fig. 1, the TCLC part consists of coupling inductor L_c, parallel inductor L_{PF}, parallel capacitor C_{PF} and thyristors with drivers. And the active inverter part is composed of a voltage source inverter (VSI) with dc-link capacitor C_{dc}, the IGBTs and their drivers. The control system includes transducer with signal conditioning circuits and DSP

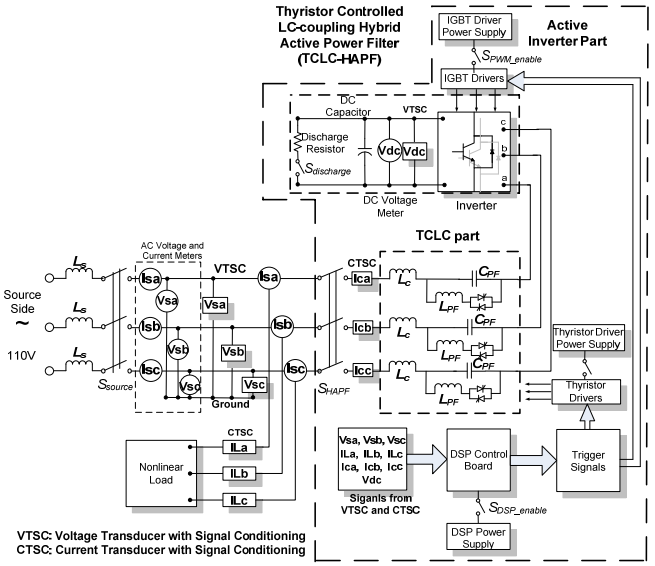


Fig. 1. System configuration of the 110V-5kVA TCLC-HAPF experimental prototype

controllers. The outputs of four voltage transducer and six current transducers with signal conditioning circuits are considered as inputs to the DSP-based control system to generate control signals to the thyristor and the IGBT drivers.

Based on the circuit system configuration in Fig. 1, the hardware and software realization of TCLC-HAPF is discussed in the following.

III. Hardware and Software Realization of the 110V-5KVA TCLC-HAPF

In this section, the hardware and software design of the TCLC-HAPF experimental prototype will be presented in three parts: *A*. Thyristor and IGBT with their divers, *B*. Design of the transducer with signal conditioning board and *C*. Selection of the digital controller and its software design.

A. Thyristor and IGBT with their divers

The TCLC part is used to compensate reactive power under the fundamental frequency, so that the low-frequency switching devices thyristor is selected. At the same time, the active inverter part provides instantaneous operation to regulate the compensating currents. Faster switching devices IGBTs are selected for the VSI. The SanRex PK110FG160 thyristors are used for the TCLC part, while the Mitsubishi IGBT modules PM300DSA60 are selected as the switches for active inverter part.

The POWER-SEM PSHI23 is selected to drive the thyristors. In PSHI23 board, 5V logic voltage is selected and InterLock Function is set to be cancelled (suitable for individual thyristor driving). In addition, the outputs are set to provide individual gate ON and OFF signals.

The designed IGBT drivers consist of a voltage divider, an isolated DC/DC converter (M57140-01), an I/O protector (SN74HCT08) a photo-coupler (PC817) and a low-pass filter to eliminate noise.

B. Transducer with signal conditioning boards

The three-phase load voltages v_x, load currents i_x, compensating currents i_{cx} and dc-link voltage v_{dc} of the TCLC-HAPF are measured by transducers with signal conditioning boards. The purpose of the transducer with signal conditioning boards is to transfer the large voltage and current electrical signals into small analog signals. Then, the output small signals from the signal conditioning boards are sent to the A/D converter to convert into digital signals for digital controller. And the proposed signal conditioning circuit is given in Fig. 2.

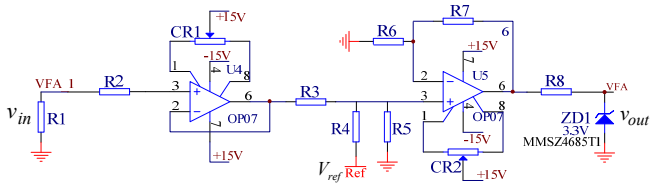


Fig. 2. Proposed signal conditioning circuit

For 110V-5kVA system, the current in each phase are normally lower than 15A (without considering transient current). The LEM LA-55P (50A/50mA) current transducers with routing double-loop are selected, and the input/output becomes 25A/50mA. And the LEM LV25-400V (400V/25mA) voltage transducers are used to feedback load voltages and the dc-link voltage.

As shown in Fig. 2, the signal conditioning circuit is constructed by two amplifiers, a zener diode and resistors. The signal conditioning circuit output can be expressed as:

$$v_{out} = \frac{R_6 + R_7}{R_6}\left(\frac{R_3 \cdot R_5}{R_3R_4 + R_3R_5 + R_4R_5} \cdot V_{ref} + \frac{R_4 \cdot R_5}{R_3R_4 + R_3R_5 + R_4R_5} \cdot v_{in}\right) \quad (1)$$

where $v_{in} = R_1 \cdot i_{out}$

In (1), V_{ref} is designed to be 3V which is provided by the chip REF5030. With carefully selected resistor values R_1~R_7, the peak of v_{out} can be designed to be within 0-3.3V to consistent with the I/O of the digital controller. In addition, v_{out} is limited by the zener diode to avoid over-voltage problem.

According to the experimental conditions, the maximum measurement ranges for load currents and compensating currents are set as $\pm 20A_{peak}$. And the maximum measurement range of the load voltages and dc-link capacitor voltages are set as $\pm 160V_{peak}$ and +100V respectively. And the parameters of signal conditioning board are provided in Table I.

Table I parameters of signal conditioning board

Range (peak value)		v_{in} (V)	v_o(V)	R_1(Ω)	R_3(Ω)
i_{Lx}	-20~20A	-4 ~ 4	0~3.191	100	40k
i_{cx}	-20~20A	-4 ~ 4	0~3.191	100	40k
v_{sx}	-160~160V	-4 ~ 4	0~3.191	400	40k
v_{dc}	0~100V	0 ~ 5	0.412~2.988	400	4k

Notes: x stands of phase a, b and c, R_2=10kΩ, R_4=30kΩ, R_5=20kΩ, R_6=40kΩ and R_7=10kΩ.

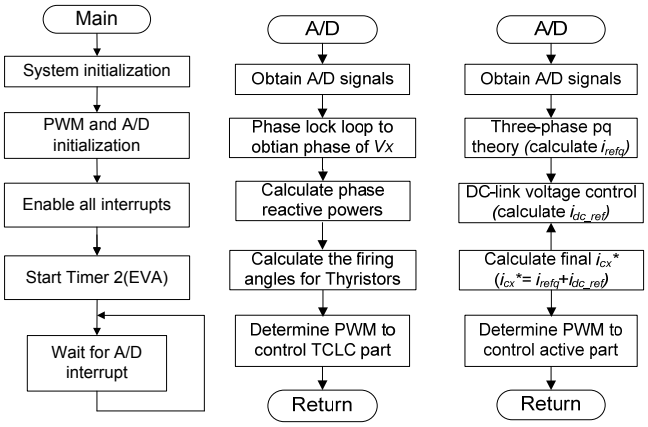
C. Selection of the digital controller and its software design

The control system is composed of two parallel DSP-TMS320F2812s to separately control the TCLC part and the active inverter part. Each TMS320F2812 consists of two event managers (EVs), EVA and EVB. And each EV module contains two general purpose (GP) timers (totally 4 timers). In the control systems of TCLC-HAPF, each timer is designed for different purposes: Timer 1 and Timer 3 are responsible for generating PWM, Timer 4 is used to activate the A/D conversion, and Timer 2 is used to define the sample rate of A/D and process signals.

For the 110V-5kVA TCLC-HAPF experimental prototype, the sampling frequency is set to 25kHz in Timer 2. For every 1/25kHz(s) period, the Timer 2 will provide a trigger signal to process A/D conversion and the corresponding interrupt. And there are totally 10 channel signals (3 load voltages v_x, 3 load currents i_{Lx}, 3 compensating currents i_{cx}, and 1 dc-link capacitor voltages V_{dc}) are converted into digital values.

Fig. 3 shows the program flow charts for the DSP-TMS320F2812 in performing A/D signal sampling, generating the trigger signals for controlling the TCLC part and generating the PWM signals for controlling the active inverter part. And it is noticed that the main program for control TCLC

part and active inverter part are same, while the interrupt routines for TCLC part and active inverter part are different.



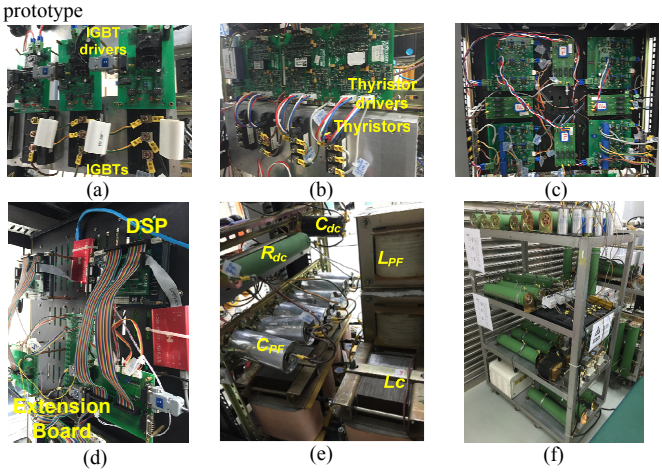
(a) (b) (c)

Fig. 3. DSP flowcharts of the TCLC-HAPF: (a) main program, (b) interrupt routine for the TCLC part and (c) interrupt routine for the active inverter part

IV. Experimental Results

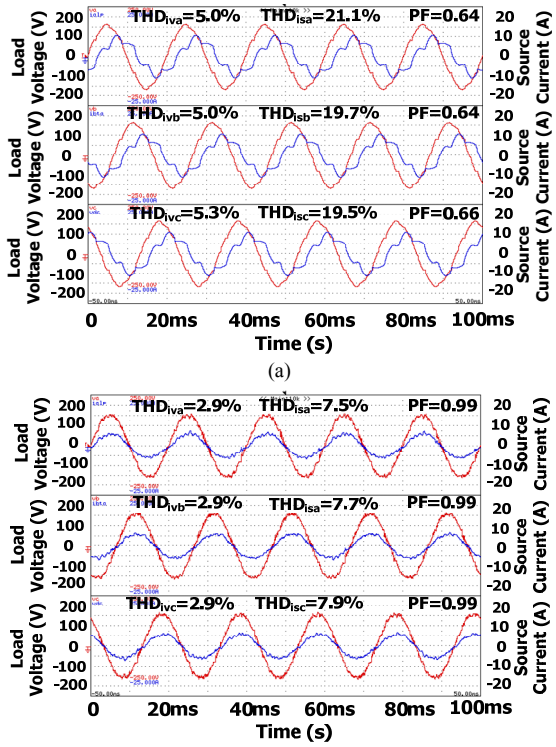
Fig. 4 shows the experimental setup of the 110V-5kVA TCLC-HAPF experimental prototype with dc-link 80V voltage and Fig. 5 gives the detailed system construction of the TCLC-HAPF and the loading system.

Fig. 4 Experimental setup of the 110V-5kVA TCLC-HAPF experimental prototype



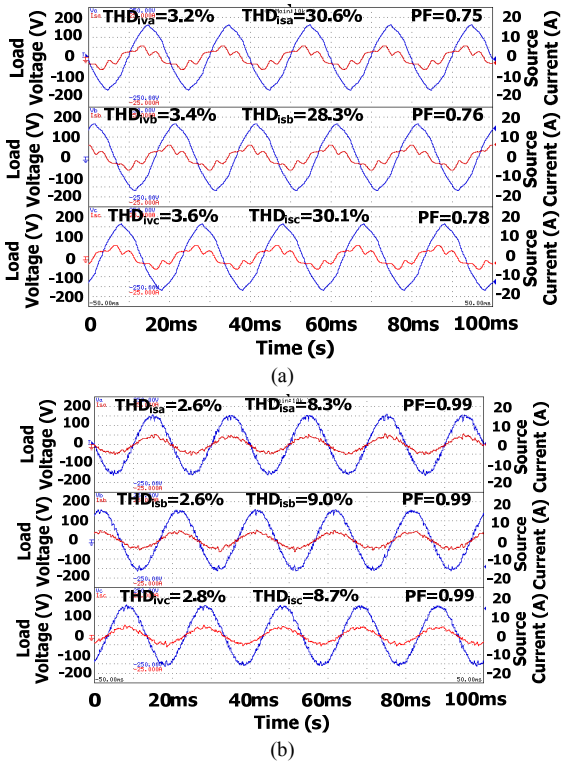
(a) (b) (c) (d) (e) (f)

Fig. 5 The 110V-5kVA TCLC-HAPF and loading system: (a) IGBTs and their divers, (b) thyristors and their divers, (c) transducers with signal conditioning circuits, (d) DSPs and their extension boards, (e) TCLC part components, dc capacitor and discharge resistor and (f) loading system



(a) (b)

Fig. 6 Experimental load voltage and source current of the TCLC-HAPF for inductive loads compensation: (a) before compensation and (b) after compensation



(a) (b)

Fig. 7 Experimental load voltage and source current of the TCLC-HAPF for capacitive loads compensation: (a) before compensation and (b) after compensation

Fig. 6 and Fig. 7 give the experimental load voltage and source current of the TCLC-HAPF for inductive and capacitive loads compensations. After applying the TCLC-HAPF compensation, the worst phase THD_{vsx} and THD_{isx} have been compensated to 2.9% and 7.9% from the original THD_{vsx}=5.3% and THD_{isx}=21.1% for inductive loads, and to 2.8% and 9.0% from the original THD_{vsx}=3.6% and THD_{isx}=30.6% for capacitive loads compensation, which can satisfy the IEEE 519-2014 standard [10]. Moreover, the worst phase power factor has been compensated to 0.99 from original 0.64 (for inductive loads) and 0.75 (for capacitive loads). In addition, the dc-link voltages for both cases can be kept at a low voltage level of V_{dc}=80V.

V. Conclusions

The hardware and software design of an 110V-5kVA three-phase three-wire TCLC-HAPF is presented in this paper. The design of the thyristor and IGBT drivers, transducers with signal conditioning circuits, and the digital control system are presented. Finally, the experimental results show that the designed TCLC-HAPF experimental prototype can provide satisfactory compensation performances with a low dc-link voltage.

VI. Acknowledgment

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