## 24.4 A 0.18V 382µW Bluetooth Low-Energy (BLE) Receiver with 1.33nW Sleep Power for Energy-Harvesting Applications in 28nm CMOS

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For true mobility, wearable electronics should be self-powered by the environment. On-body thermoelectric (~50µW/cm$^2$) is a maturing energy source but delivers a deeply low and inconstant output voltage (0.05 to 0.3V) hindering its utility. With the limited power efficiency of ultra-low-voltage (ULV) boost converters (64% in [1]), there is a rising interest in developing ULV radios that can operate directly at the energy-harvester output, reducing the waste of energy and active-sleep latency. The 2.4GHz receiver in [2] validates 0.3V operation, but is a non-standard design without I/Q demodulation. Also, its focus is on the active power (1.6mW) assuming its 0.3V supply is constant.

This receiver (Fig. 24.4.1) aims at the BLE standard, consuming just 382µW at 0.18V, and can tolerate 50% variation of its energy-harvesting supply ($V_{DD,EH}$) up to 0.3V. Unlike [2], on-chip input matching and I/Q demodulation are included. The most power-hungry blocks - LNA and VCO - are directly operated with $V_{DD,EH}$ to maximize the current efficiency. Other RF blocks - I/Q generator and mixers - are passive. Only the ultra-low-power blocks - Bandgap reference (BGR) and baseband (BB) amplifier - are powered-up internally by a micropower manager. The manager features ring-VCO-locked charge pumps (CPs) to secure low-voltage startup, and stabilized bias voltages against $V_{DD,EH}$ variation. Implicit and explicit power-gating are enforced everywhere to suppress the sleep power that is as critical as the active power in low-duty-cycle radios.

The forefront is a two-stage power-gating LNA ($M_{1,2}$) with LC tanks as the load (Fig. 24.4.1). Without elevating the power, a very low $V_{DD,EH}$ allows bleeding more bias currents into $M_{1,2}$ to improve the NF and linearity. A 50Ω input impedance is generated at the $M_1$ source node, where an AC-grounded transformer ($T_1$) resonates out the input parasitic capacitance ($C_P$), and negatively couples the RF input ($V_{in}$) to the $M_1$ gate node, improving further the gain and NF at no extra power. Although the forward-body bias can raise the transistor's $f_T$, it is detrimental when concerning the leakage current (e.g., 20nA/transistor in [2]). In contrast, our LNA utilizes only high-$V_{TH}$ thin-oxide transistors, and $M_{1,2}$ can be implicitly power-gated when pulling the gate bias ($V_{G,LNA}$) to ground. As such, and thanks to the deeply-low $V_{DD,EH}$, the measured sleep power of the LNA is reduced to 0.33nW at 0.18V. With a fixed $V_{G,LNA}$ (≈0.56V) mirrored from a BGR current, the LNA measures ~16dB gain, insensitive to $V_{DD,EH}$ variation.

The I/Q signals ($V_{rf3,I}$, $V_{rf3,Q}$) are generated after the LNA. As BLE covers only an 83.5MHz bandwidth at 2.4GHz and entails a low IRR (21dB), a 1$^{st}$-order RC-CR network is adequate [3]. This scheme facilitates the use of a 2.4GHz VCO and its native outputs ($V_{osc±}$) to directly drive up the passive mixers ($M_{MIX}$), eliminating the power-hungry dividers and buffers. $V_{G,MIX}$ (≈0.42V) is the gate bias of $M_{MIX}$ provided by the same BGR as the LNA. Four inverter-based amplifiers (INV) with RC feedback, input and output capacitors, improve the BB stopband rejection. Their supply voltage ($V_{DD,INT}$≈0.46 to 0.5V) is generated by a CP. The sleep power of INV is hindered by an explicit tail switch.

A Class-D VCO [4] is promising for ULV operation due to its large output swing: ideally ~3×$V_{DD,EH}$. To secure a fast startup, a Class-C starter ($M_C$) that operates in saturation, is paralleled with a Class-D core ($M_D$) functioning like switches (Fig. 24.4.2). With $M_C$ biased at $V_{BS}$=$V_{DD,INT}$ during the startup, it offers adequate initial currents ($I_{startup}$) to excite the LC tank. By sensing $V_{osc±}$ via a passive CP, $V_{CP}$ will grow up when $V_{osc±}$ reaches the steady state. Meanwhile, $M_C$ turns OFF ($V_{BS}$=0), leaving $M_D$ to sustain the oscillation. Since $M_D$ has a permanent gate voltage of $V_{DD,EH}$, the tail switch is essential for power-gating. The simulated VCO startup time is 25ns.

The micropower manager governs the internal voltages (Fig. 24.4.3). To tolerate a time-varying $V_{DD,EH}$, while avoiding dedicated low-dropout regulators, a ring-VCO-locked loop rounds $CP_1$ ($CP_2$) regulating $V_{DD,PM1}$ and $V_{DD,INT}$. An auxiliary $CP_3$ offers $V_{DD,PM2}$ and powers-up another BGR to deliver $V_{ref,PM}$ for the error amplifiers ($A_{1,2}$). The BGR powered-up by $CP_1$ (3 sub-cells in series) generates the biases $V_{G,LNA}$ and $V_{G,MIX}$. $CP_2$ (5 sub-cells in parallel) offers more current (~100µA) to $V_{DD,INT}$ for powering the 4 BB amplifiers (Fig. 24.4.1). The schematic of each CP sub-cell is the same as that in Fig. 24.4.2 (upper right). The required 6-/10-phase clocks (CLK) are generated by a 3-/5-stage ring-VCO. Inside the ring-VCOs all inverters are differential and bootstrapped to boost the clock swing (~2.3×$V_{DD,EH}$ in simulation, adequate to directly drive up the CP). Unlike the single-ended solution [5], $M_{ip,in}$ here is driven more synchronically, reducing the power loss due to reverse currents. Also, by separating the sub-inverters ($B_1$ and $B_2$), the oscillation frequency and output drivability of the ring-VCO are decoupled. The forward diodes at $V_{DD,PM1}$ are for over-voltage protection when $V_{DD,EH}$>0.35V.

As $V_{DD,INT}$ comes directly from $CP_2$ (Fig. 24.4.3), reducing its ripple calls for large decoupling capacitor ($C_{DE}$). To address it, equally distributing the 10-phase CLK to the 5 sub-cells of $CP_2$ can reduce the output ripple ~5× when comparing with a 2-phase CLK. At a 40MHz CLK rate, the simulated $V_{DD,INT}$ ripple is <0.7m$V_{pp}$ at an affordable $C_{DE}$ of 18pF, which will be suppressed further at the receiver's differential BB outputs.

Fabricated in 28nm CMOS, the micropower manager ($CP_{1-3}$) stabilizes in ~200µs (Fig. 24.4.4, left), which can be overlapped with the startup time (~400µs) of the BLE crystal oscillator [6]. Thus, the agility of the receiver in launching a connection should not be affected. Measured over a wide range of $V_{DD,EH}$ from 0.156 to 0.3V (Fig. 24.4.4, right), the variations of $V_{G,LNA}$ and $V_{DD,INT}$ are within 0.18% and 12%, respectively, saving the excessive power by ~2.5×.

The RF performances (Fig. 24.4.5) are coherent between 0.18V and 0.3V without tuning (except the VCO frequency due to no PLL). With the $S_{11}$ BW upshifted by ~50MHz, we measured the total gain, NF and out-of-band IIP3 at 2.5GHz. The VCO shows a worst phase noise of -113dBc/Hz at 2.5MHz offset, and covers 2.32 to 2.65GHz (13.3%). At 0.18V, the input-referred $P_{1dB}$ is -29dBm (not shown), which can be improved by adding a low-gain mode at the LNA to handle the blockers.

Benchmarking with the recent art (Fig. 24.4.6) [2,3,7], this work succeeds in using a ULV and inconstant supply, while consuming the lowest active power. The sleep power is well controlled, and the main expense is the active area (1.65mm$^2$) as Fig. 24.4.7 shows.

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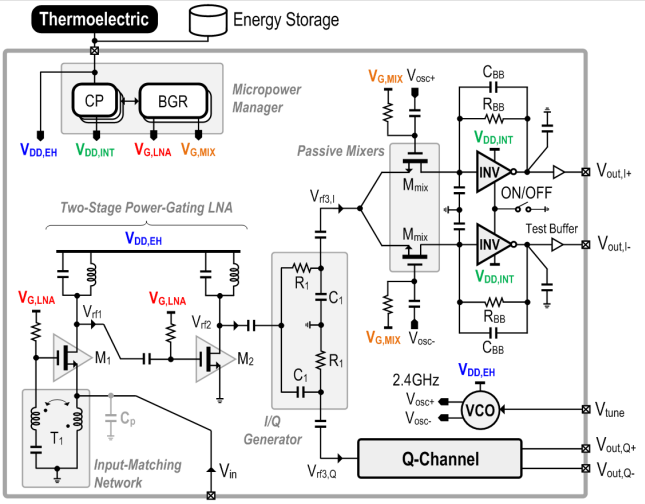


Figure 24.4.1: Proposed energy-harvesting BLE receiver, with LNA and VCO powered by $V_{DD,EH}$ directly. A micropower manager supplies other internal power and biases.

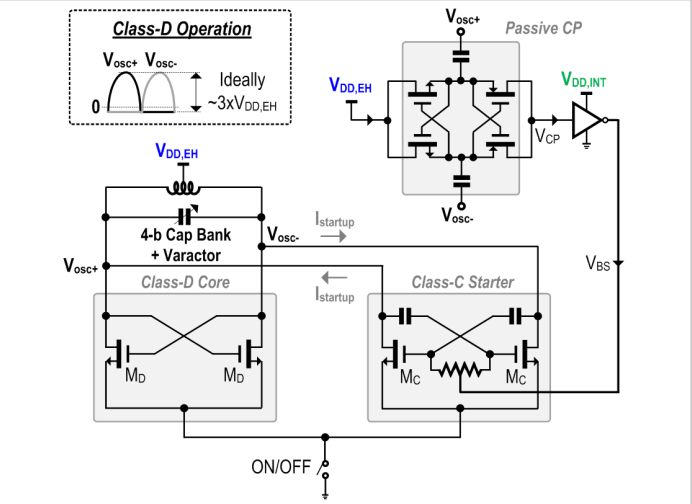


Figure 24.4.2: Proposed ULV Class-D VCO with a Class-C starter. The passive charge-pump (CP) senses $V_{osc\pm}$ to activate/stop the Class-C starter during/after the startup process.

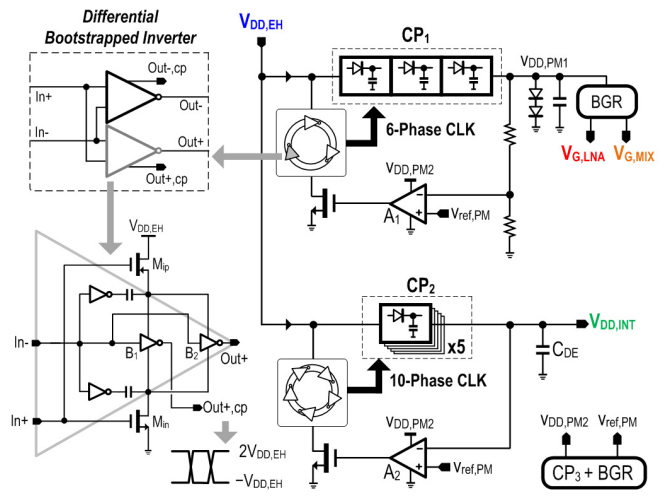


Figure 24.4.3: Proposed micropower manager using ring-VCO-locked $CP_1$ ($CP_2$) to regulate $V_{DD,PM1}$ ($V_{DD,INT}$). Each ring-VCO delivers a high-swing output via bootstrapped inverters.

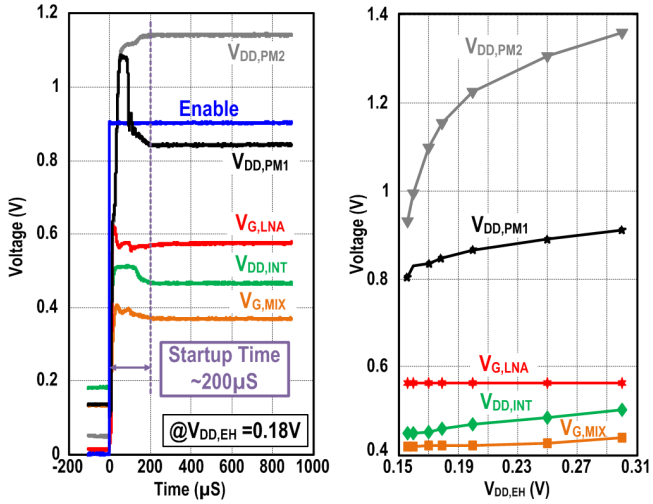


Figure 24.4.4: Measured startup time (left) and locking conditions (right) of the micropower manager. The very steady $V_{G,LNA}$ stabilizes the RF performances against $V_{DD,EH}$.

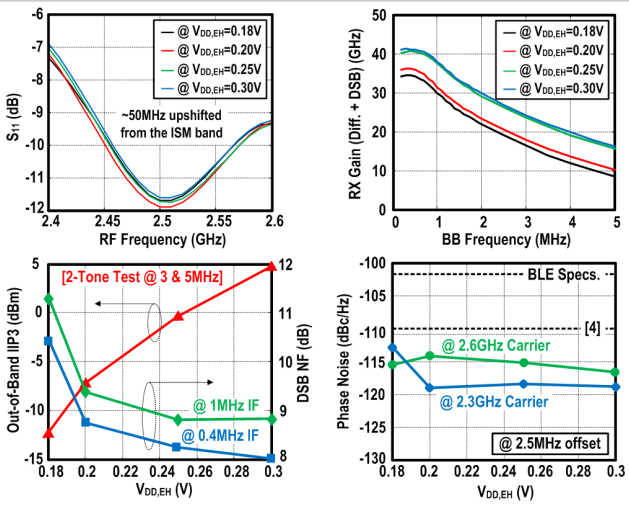


Figure 24.4.5: Measured receiver performances: (Upper) $S_{11}$ and BB gain against frequency at different $V_{DD,EH}$; (Lower) NF, out-of-band IIP3 and VCO phase noise against $V_{DD,EH}$.

| | This Work | | ISSCC'15 [3] [A. Selvakumar, et al.] | ISSCC'13 [2] [F. Zhang, et al.] | ISSCC'13 [7] [Z. Lin, et al.] |
|---|---|---|---|---|---|
| Applications | 2.4GHz BLE | | 2.4GHz BLE | 2.4GHz Non-Standard | 2.4GHz ZigBee |
| Key Architecture & Circuit Techniques | Power-Gating LNA + ULV Class-D VCO + Passive I/Q Gen. + Micropower Manager | | Current-Reuse Quadrature-LNA-Mixer-VCO Cell | Transformer-Coupling LNA and VCO + IF N-Path Filter | Current Reuse RF-to-BB Cell + VCO & DIV-by-4 |
| External Matching | Zero | | 1 inductor + 1 cap. | 1 inductor + 2 caps. | zero |
| Supply Voltage (V) | 0.18 | 0.3 | 0.8 | 0.3 | 0.6 & 1.2 |
| Active Power (µW) | 382 | 1305 | 600 | 1600 | 2700 |
| Sleep Power (nW) | 1.33 | 3.32 | N/A | N/A | N/A |
| NF (dB) | 11.3 | 8.8 | 15.1 to 15.8 | 6.1 | 9 |
| VCO Phase Noise (dBc/Hz) @ Offset | -113 to -115.5 @ 2.5 MHz | -116.6 to -118.9 @ 2.5 MHz | -109 @ 2.5 MHz | -112.8 @ 1 MHz | N/A |
| | [BLE spec: -102 @ 2.5 MHz] | | | | |
| Out-of-Band IIP3 (dBm) | -12.5 | +4.8 | -15.8 to -16.8 | -21.5 | -6 |
| | [BLE Spec: -30] | | | | |
| IRR (dB) | 26.2 | 25.1 | 30.5 to 37.3 | N/A (no I/Q) | 28 |
| | [BLE Spec: 21] | | | | |
| Voltage Gain (dB) | 34.5 | 41.3 | 55.5 to 56.1 | 83 | 55 |
| BB Style | With I/Q | | With I/Q | Without I/Q | With I/Q |
| BB Filtering | 3 real poles | | 2 complex poles | 2 N-path filters | 3 complex poles |
| Active Area ($mm^2$) | 1.65 | | 0.25 | ~1.7 * | 0.26 |
| Technology | 28nm CMOS | | 130nm CMOS | 65nm CMOS | 65nm CMOS |

Figure 24.4.6: Chip summary and benchmark with the prior art. *Estimated from chip photo.

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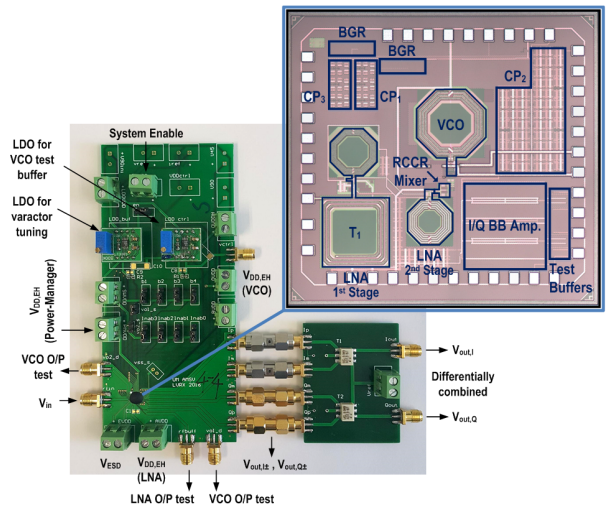


**Figure 24.4.7: Die micrograph of the BLE receiver in 28nm CMOS. Separated $V_{DD,EH}$ in PCB for LNA, VCO and micropower manager allow active/sleep power measurements of each block.**


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