PID Control Considerations for Analog-Digital Hybrid Low-Dropout Regulators (Invited Paper)

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***Abstract*—This paper briefly introduces the developments of the fully-integrated low-dropout regulators (LDOs) at the beginning. Then, we use the classic proportional-integral-derivative (PID) control theory to discuss and categorize the existing LDOs, and present our design considerations for analog-digital hybrid LDOs in an intuitive way.**

Keywords—Analog, digital, hybrid, low dropout regulator (LDO), PID control, transient enhancement.

I. INTRODUCTION

Low dropout regulator (LDO) is a supply regulation block widely used in almost all the systems-on-a-chip. To reduce the number of pins and capacitors on board, and to obtain a clean as well as fast transient response point-of-load supply, fully-integrated low dropout regulators have been a very popular research topic in the past 15 years [1]-[10]. Hundreds of papers have been published in this area, with the citations (Google Scholar) of both [1] and [2] being ~500 now.

In the internet-of-things (IoT) era, to prolong the battery recharge/replacement cycle, or to operate with weak ambient energy sources, energy efficiency becomes one of the most important issues. The supply voltage kept going down to the near-threshold region (~0.5V) for energy-efficient computing. In such case, LDOs with analog control suffer from low DC loop gain, thus exhibiting reduced output accuracy.

In 2010, a seminal paper on digital LDO [11], cited ~150 times so far, proposed to use a bidirectional shift register (digital integrator) to control a switch array and consequently control the output current. But its performances, both transient response and power supply rejection (PSR), are obviously below that of the analog LDOs. Therefore, several research groups have obtained significant advancements on the digital LDOs with multi-mode operation [12]-[21]. But still, the performances of the digital-only LDOs are limited by the analog-to-digital interface, in other words, the comparator.

Recently, to amend the fundamental limits of the digital LDO, we proposed analog-assisted techniques for fast and intrinsic response with negligible current consumption [22], [23]. Meanwhile, analog-digital hybrid LDO is a promising architecture combining the benefits of both analog and digital controls [24]-[28]. This paper intends to categorize all the existing LDO designs by their control methods.

II. PID CONTROL

The classic proportional-integral-derivative (PID) control can basically be applied to all the systems that have feedback loop(s). Fig. 1 shows a system diagram of the PID control with three paths and the plant under control. The PID function can be expressed as:

$$u(t) = K_P e(t) + K_I \int_0^t e(x)dx + K_D\, de(t)/dt \qquad (1)$$

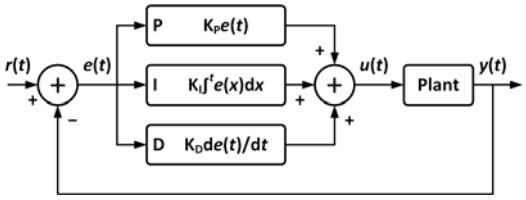

Fig. 1. A system block diagram with PID control.

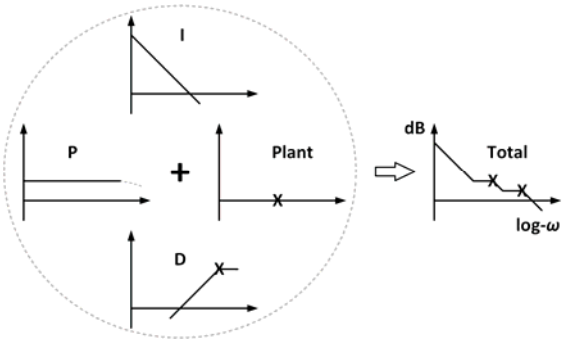

Fig. 2. Conceptual Bode plots of a system with PID control.

where K_P, K_I, K_D are the gain factors of the P, I, and D paths, respectively.

*The P path output is proportional to the **current** error.*

*The I path integrates the **past** information.*

*The D path predicts the **future** based on the rate of change.*

Fig. 2 shows the conceptual Bode plots of the P, I, and D paths, respectively. Obviously, the I path is a low pass filter. The P path has a constant gain across full spectrum in the ideal case, but in reality, the P path may have poles that are beyond the frequency of interest. The D path processes the high frequency signal, which means it is also vulnerable to high frequency noise. Therefore, the D path is usually accompanied by one or two high frequency poles to attenuate the out-of-the-signal-band noises. The plant, which is the power stage in an LDO, usually consists of one pole (or more). Therefore, theoretically, an LDO with PID control can achieve a wider unity gain bandwidth by compensating the pole(s) in the band by the zero(s) from the P or D paths.

III. PID CONTROL IN ANALOG/DIGITAL/HYBRID LDOS

Although the PID control theory is well established, the real circuit implementations still require a lot of efforts and design tricks to accommodate practical issues, like supply voltage, quiescent current, component sizes, and circuit-/transistor-level limits, etc. So, how to implement the PID control paths in the analog and digital domains, respectively?

A. Load Transient Response of an LDO with PID Control

Fig. 3 shows the load transient responses of an LDO with either PID control or PI control, respectively. When the load

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current I_{LOAD} changes from light to heavy, the output voltage V_{OUT} starts to drop rapidly. With PID control, the D path responds well to the large dv/dt, and boosts the LDO output current I_{LDO} at the very beginning of the load transient. When certain dv happens, the P path contributes more accordingly. V_{OUT} drops to the bottom when I_{LDO}=I_{LOAD}, at where dv/dt=0. After that, the P path effect on I_{LDO} reduces gradually as V_{OUT} starts to recover, and the D path effect changes its polarity. So far, the I path keeps accumulating the dv error until V_{OUT} goes higher than its nominal value. During the V_{OUT} recovery process, the D path (negative output) keeps compensating the I path (accumulating positive output), therefore, the voltage recovery overshoot can be much reduced.

On the other hand, if there is no D path, as shown in Fig. 3(b), I_{LDO} is much larger than I_{LOAD} when V_{OUT} recovers back to its nominal value for the first time, and the V_{OUT} overshoot happens due to the accumulated error in the I path. Last but not least, the I path helps V_{OUT} to finally settle at the nominal value with good accuracy.

B. PID Circuit Implementations in Analog LDOs

In analog LDOs, when we design the dominant pole of a loop at the output node, that means the inner poles should be out of the unity-gain frequency (UGF). This feature becomes easier to be achieved with more advanced processes [6], [7], [29]. Then, we obtain a flat wide bandwidth, corresponding to the Bode plot of the P path (Fig. 2). Alternatively, when we use an NMOS transistor in the power stage, the NMOS is configured as a source follower, of which the output current is intrinsically related to the output voltage regardless of the frequency, which means it is ideally a P path [30].

If we have a loop with a low frequency internal dominant pole, acting as the integrator, we get an I path. Since the duty of the I path is to improve the DC error, we need a high gain error amplifier for it. How about the D path? A derivative function requires a capacitor, which acts as a differentiator, to convert the rate of change of the load current into voltage, and feed it back to the inner loop [2]-[5], [9], [10]. When we use Miller compensation in the error amplifier, the Miller capacitor feeds back the high frequency output variations, which can be considered as a D path. But, in the meantime, the Miller capacitor also lowers the dominant pole, acting as an integrator, which means it also affects the I path.

C. PID Circuit Implementations in Digital LDOs

In digital LDOs, the shift register serves as a perfect integrator, the I path can operate at a very low supply with a pole (1/s) at DC. Its UGF shifts with the sampling rate (clock frequency) and the step size of the power switch array. Unfortunately, the DC gain of a digital LDO is also related to the gain of the quantizer, which is an uncertain value (quantization error) related to the input value. As the digital outputs are binary only, 1 (supply) or 0 (ground), when the input level is close to the quantization levels, the quantization error is small, and the equivalent gain is large, and vice versa. This uncertain DC gain and consequently the uncertain UGF results in the unwanted limit cycle oscillation (LCO) [31], [32].

When we bypass the integrator and control a power switch directly by the comparator output, we get a simple digital P path [32]. But due to the LCO issue, we cannot have a standalone digital P path, and need an I path to attenuate the LCO ripple. Other publications used a multi-bit analog-to-digital converter for the P path, which needs extra comparators and reference levels or time-domain architectures [16], [17], [33], [34].

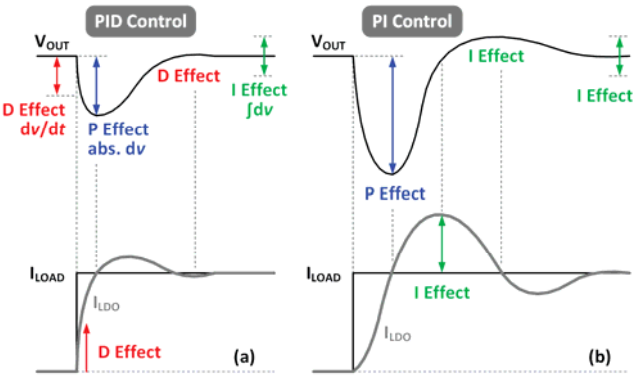

Fig. 3. Load transient responses of an LDO with either (a) PID control or (b) PI control, respectively.

For the D path in the digital domain, at algorithm level, we can of course implement it by calculating the rate of change between clock cycles. But, the transient response requirement for an LDO in high-performance digital systems is very stringent usually being in the sub-nanosecond range.

Then, can we also have the digital D path at circuit level, such that it can get the D information within half clock cycle? The work in [19] proposed a slope detector, which computes the V_{OUT} slope with four discrete-time comparators. The slope detector is triggered through the continuous-time dead-zone comparators. And then, to obtain a digital D path, the detected slope information is processed with asynchronous feed-forward logics. However, this D path has still experienced two comparator delays and certain logic delays, undermining the response speed. Alternatively, the successive approximation logic (switching 1/2 of the power switches for the first cycle, and then 1/4, 1/8 …) is a coarse prediction for the required output current [12], [18], [21]. But the coarse prediction may only work well for certain large load steps, and may generate extra voltage overshoots/undershoots in boundary conditions.

D. Analog-Digital Hybrid LDOs

As mentioned above, digitally controlled LDO becomes popular in recent years for low-voltage operation. Also, the digital control is flexible, can have good communication with the load, such that it can react in advance when it gets the request signal from its load [35]. However, when an ultra-fast response is necessary (close to the limit of the transistors), the standalone digital control is limited by the clock frequency. Analog circuit techniques are still faster, more straight-forward, and more energy-efficient. Therefore, it is good to have an analog-digital hybrid LDO that combines the large signal and high gain properties of the digital LDO and the fast P and D paths in the analog domain [22]-[28].

Our works [22] and [23] found a way to add a coupling capacitor (D path) between V_{OUT} and the digital internal nodes for the PMOS and NMOS digital LDOs, respectively. Plus, our work [28] designed a low-voltage (0.6V) analog LDO (P path) with improved load regulation capability to support the digital LDO (I path), achieving −22dB PSR at 1MHz. Table I summarizes the existing LDOs by its control methods.

IV. CONCLUSIONS

Digital control is flexible, process scalable, good for low-voltage operation, and is suitable for implementing the I path in the control loop. Analog control is intrinsic, fast, energy efficient, and is suitable for the P and D paths. By combining

TABLE I CATEGORIZATION OF LDOS BY CONTROL METHODS

Category	Publications	
Analog P	[28] Ho, JSSC 2010	
Analog PI	[6] Lu, TCAS-I 2015	[7] Lu, ELL 2016
Analog PID	[2] Milliken, TCAS-I 2007	[9] Bu, TCAS-I 2018
Digital I	[11] Okuma, CICC 2010	
Digital PI	[16] Kim, JSSC 2017 [32] Huang, 2016	[17] Lim, TVLSI 2017
Digital PID	[12] Li, TPEL 2016 [19] Kim, SSC-L 2018	[18] Salem, JSSC 2018
Digital I + Analog P	[25] Nasir JSSC 2018 [27] Zhang, TCAS2 2019	[26] Nasir, TCAS2 2018 [28] Huang, CICC 2019
Digital I + Analog D	[22] Huang, JSSC 2018	
Digital I + Analog PD	[23] Ma, ISSCC 2018	

the benefits of both analog and digital control loops, the hybrid LDO can be a good low-voltage solution with fast transient response and also certain power supply rejection.

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