A 0.8 µW 8-bit 1.5~20-pF-Input-Range Capacitance-to-Digital Converter For Lab-on-Chip Digital Microfluidics Systems

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***Abstract*— This paper presents an ultra-low-power capacitance-to-digital converter (CDC) for digital microfluidics systems that demand a wide capacitive sensing range. It is structured with a switched-capacitor capacitance-to-current front-end interface, followed by a differential current-mode SAR analog-to-digital converter (ADC). By using subthreshold-biased transistors, the differential current-mode SAR ADC significantly saves power and reduces sensitivity to supply voltage and clock variation. The 8-bit 1-kS/s CDC designed in 0.35-µm CMOS exhibits a capacitance sensing range from 1.5 to 20 pF while consuming a total power of 0.8 µW. The ENOB of the current SAR ADC is 7.46.**

I. INTRODUCTION

Digital microfluidics systems using the Electro-Wetting on Dielectric (EWOD) technique are increasingly popular for manipulating µL or nL droplets over a hydrophobic surface. Example applications of EWOD are immunoassays, DNA sequencing, and the detection of airborne particulate matter. The EWOD is expected to open up a prospective direction of low-cost assess of biochemical and reagents, while the complex operations such as droplet sensing, splitting and manipulation can be relied on the low-cost CMOS integrated circuits [1]. Fig. 1 shows the side view of a generic EWOD digital microfluidics system, which fundamentally operates with two parallel plates coated with hydrophoization materials. The presence or absence of droplet in a particular position shows electrically a variation of capacitance [2]. When a conducting discrete droplet aligns with the buried electrode, a larger capacitance is expected to be created, due to the change of dielectric material. This *change of capacitance* provides a mean to detect and control the position of the droplets, which is the desired sensing metric of this research work.

In order to cover a wide range of capacitance variation (e.g., due to different volume of the droplet) with small power and area, a direct capacitance-to-digital converter (CDC) is proposed. When the CDC scans the capacitance of the bottom electrode to the top electrode and digitizes the output for the back-end digital controller, a closed-loop digital microfluidics system can be formed. The expected capacitance variation of our system with reference to [3] is from 5 to 15 pF.

Among the recently published CDCs, voltage and period are more popular chosen as the medium variable for transforming the capacitance change to electrical signals, and then are converted into digital codes by an analog-to-digital converter (ADC) or semi-digital values by pulse counter [4-5]. These kinds of CDCs typically involve a number of power-hungry operational transconductance amplifiers (OTAs) to balance the noise issue and feedback stability. Particularly, for large sensing capacitance the feedback resistors or capacitors become too sizeable to be integrated on-chip, and the sensing range is also limited by the output voltage swing of the OTA. Another choice for CDC design is based on the charge redistribution technique [6]. It involves a capacitive sensor and a ranging capacitor array. Regrettably, the capacitance sensing range is highly limited by the size of the capacitor array.

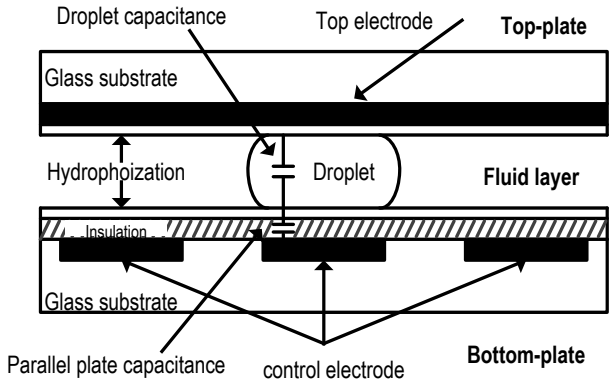


Fig. 1 Side view of the EWOD digital microfluidics system.

The proposed solution presented in this paper is based on the sensing of the current flowing through the capacitors, and directly converting the current value to digital codes using a current-mode 8-bit resolution SAR ADC. Targeting an operation frequency of 1 kHz, the achieved capacitance sensing range is 1.5 to 20 pF, while showing 7.46 ENOB (SAR ADC) at 0.8 µW of power consumption.

II. CIRCUIT CONFIGURATION

The block diagram of the proposed CDC is shown in Fig. 2. It consists of a capacitance-to-current interface followed by a current-mode differential SAR ADC. A constant current I_{ref} flows through both the reference capacitor C_r and sensing

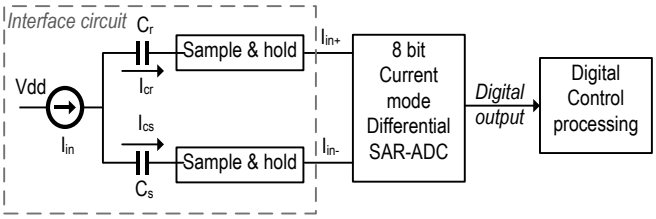


Fig. 2 The block diagram of the proposed CDC.

capacitor C_s. In this way, depending on the difference between the two capacitors, a differential current can be obtained. Such a differential current is then sampled and held at a certain time to conduct the current samples I_{in+} and I_{in-} ready for back-end SAR-based digitization.

In order to save power and area, the following techniques are applied in the proposed CDC: 1) the interface circuit is based on the passive switched-capacitor (SC) technique for its simplicity and no static power; 2) the CDC is operated in current mode with improved sensing range and each device is biased in the sub-threshold region; 3) OTAs with resistors or capacitors are completely avoided while the total required capacitance is minimized; 4) The use of a current-mode SAR ADC leads to high power- and area-efficiencies [7-8] and is insensitive to environmental noise.

A. Forefront Capacitance-to-Current Interface

The capacitance-to-current conversion is based on,

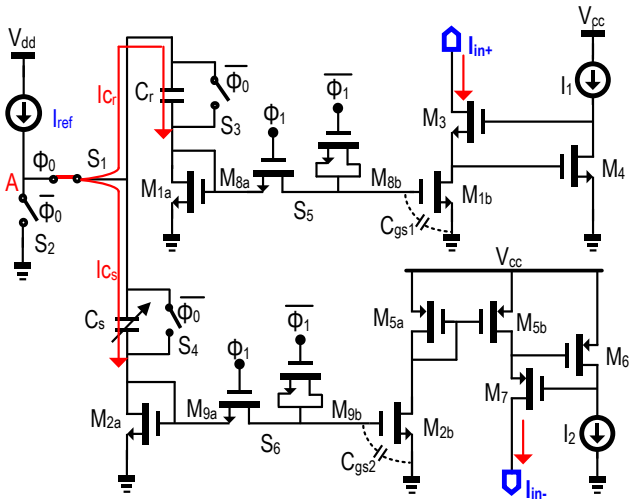
$$I = C \cdot \frac{dv}{dt} \tag{1}$$

In order to obtain the differential current [4], the front-end capacitance-to-current interface circuit is shown in Fig. 3(a). I_{ref} is the input constant current. S_1~S_4 are complementary switches to reduce the on-resistance variation. S_5~S_6 are NMOS dummy switches to avoid the clock feedthrough and charge injection. When the circuit sets to operate, the clock Φ_0 is high, S_1 is on, S_2~S_4 are off, and then the input current flows through the two capacitors C_s and C_r. Since the impedance of the diode-connected transistors M_{1a} and M_{2a} is at least 10^8 less than that of C_s and C_r, respectively, their effects on accuracy can be safely neglected. According to (1), the current through C_s (Ic_s) and the current through C_r (Ic_r) are written as in (2),

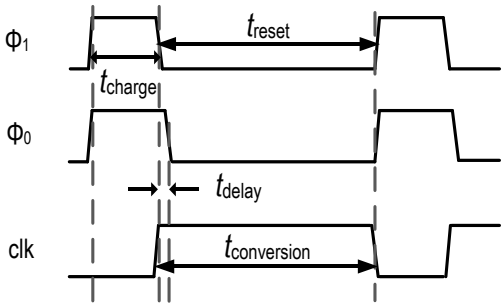
$$I_{C_s} = I_{ref} \cdot \frac{C_s}{C_r + C_s} \quad , \qquad I_{C_r} = I_{ref} \cdot \frac{C_r}{C_r + C_s} \tag{2}$$

Assuming that $C_s = C_r + \Delta C$, (2) can be rewritten as

$$\begin{cases} I_{C_s} = \dfrac{I_{ref}}{2} + \dfrac{\Delta C}{2C_r + \Delta C} \cdot \dfrac{I_{ref}}{2} \\ I_{C_r} = \dfrac{I_{ref}}{2} - \dfrac{\Delta C}{2C_r + \Delta C} \cdot \dfrac{I_{ref}}{2} \end{cases} \tag{3}$$



(a)



(b)

Fig. 3 (a) The capacitance-to-current interface circuit, (b) timing diagram.

For ideal operation,

$$I_{C_s} - I_{C_r} = I_{in-} - I_{in+} = \frac{2 \cdot \Delta C}{2C_r + \Delta C} \cdot \frac{I_{ref}}{2} \tag{4}$$

The obtained differential current ΔI is defined as

$$\Delta I = \frac{\Delta C}{2C_r + \Delta C} \cdot \frac{I_{ref}}{2} \tag{5}$$

Eqs. (3) and (4) clearly illustrate the differential nature in capacitance-to-current conversion. From (5), we observe that the current ΔI is only determined by the variance of the sensing capacitance for fixed values of I_{ref} and C_r, which implies that a large input capacitance range (i.e. large ΔC) can be achieved by the following direct current-mode conversion. In order to cover the capacitance variation range in a digital microfluidics control system, the values of I_{ref}, C_r and the charging time t_{charge} should be properly chosen.

According to (1), the potential voltage at the node A (V_A) is calculated as:

$$V_A = \frac{I_{ref}}{C_r + C_s} \cdot t_{charge} \quad (6)$$

With the increase of C_s, more charging time is required to obtain stable current, and hence, the minimum t_{charge} is determined by the maximum C_s when I_{ref} and C_r are both fixed. While for the minimum C_s, the potential V_A will not exceed the voltage limitation of the process. In the design, the input constant current I_{ref} is optimized to be 51.2 nA with the reference capacitor of 1 pF. The t_{charge} is set at the value of 200 μs to achieve the capacitance sensing range of 1.5 to 20 pF. The input constant current source, which is supplied by a high voltage $V_{dd}=5V$, is designed using wide-swing current mirrors with both large output headroom and enhanced output impedance for I_{ref} [4]. The other part of the circuitry is supplied by a low voltage $V_{cc}=1V$ for saving power.

Fig. 3(b) describes the timing diagram of the interface circuit, with the corresponding sample-and-hold operation. Φ_0 and Φ_1 are both high to start the interface and generate the differential currents. At the end of Φ_1, S_5 and S_6 are turned off to sample Ic_r and Ic_s. Φ_0 will delay for several microseconds to be low to turn off S_1 and turn on S_2~S_4 for discharging to prepare for the next conversion. The currents through the capacitors C_s and C_r are firstly converted to voltages by M_{1a} and M_{2a}, and the gate voltages are held by the parasitic capacitors C_{gs1} (C_{gs2}) of M_{1b} (M_{2b}), then, the current through M_{1b} and M_{2b} will be generated and mirrored to the differential inputs of the SAR ADC.

To achieve better power efficiency, all the transistors are biased in the sub-threshold region. As subthreshold transistors exhibit exponential I-V relationship, a slight variation in the gate voltage can lead to a significant change in the drain current. One way to solve this issue is to increase the channel length of transistors for improved matching. Another approach is to enhance the current mirror output impedance. In the proposed design, $M_{3\text{-}4}$ and $M_{6\text{-}7}$ are utilized to increase the impedance for Ic_r and Ic_s, respectively, so that the current variation during conversion is limited to less than 1 LSB. The PMOS current mirror M_{5a}-M_{5b} is used to achieve opposite current flow for Ic_s. Notice that Ic_s should be larger than Ic_r for correct operation in this design. As a result, C_s should be larger than the reference capacitor C_r (i.e. $\Delta C \geq 0$) so that (I_{in-} - $I_{ref}/2$) > 0 during A/D conversion.

B. Current-Mode Differential SAR ADC

Current-mode SAR ADC features not only high power-efficiency for low speed conversion, but also high area-efficiency since the current-steering digital-to-analog converter (DAC) can be built by using only transistors. Fig. 4 shows the 8-bit differential current-mode SAR ADC, which consists of a current-steering DAC, a current-mode comparator, and a SAR logic unit. Cascading is used in the DAC to further improve the current mirror accuracy. Also, as all the transistors are operating in the sub-threshold region, matching is critical in order to minimize errors. The transistor

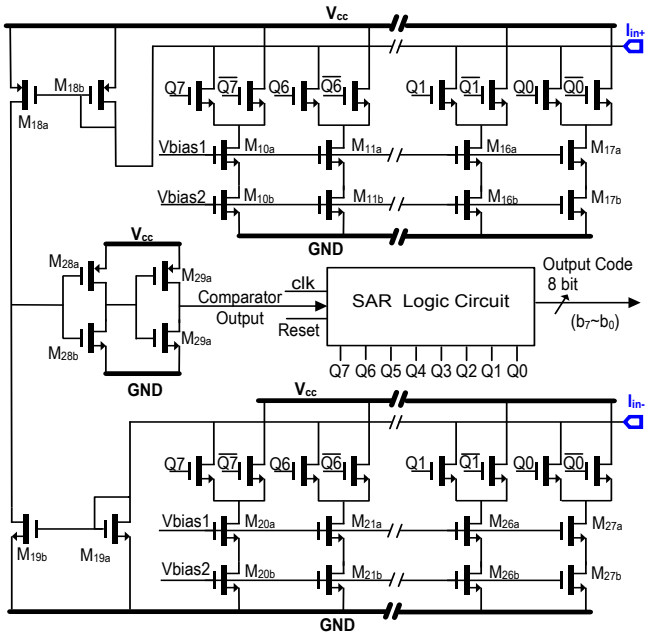


Fig. 4 The differential current-mode SAR ADC.

was dimensioned to achieve the target resolution of 100pA/LSB.

In the current-steering DAC, the differential currents I_{in+} and I_{in-} are either added or subtracted from the DAC current. M_{18a}-M_{18b} and M_{19a}-M_{19b} then mirror the resultant current to the comparator. The current mode comparator is built by a cascaded inverter structure, which can achieve small size and low power consumption. It consists of two inverters M_{28a}-M_{28b} and M_{29a}-M_{29b}. The first inverter operates as an integrating current-to-voltage converter by using the gate capacitance and the second is used for sign inversion. The parameters of the two inverters are the same to ensure a matched threshold level to reduce offset.

III. SIMULATION RESULTS

The CDC is designed and simulated in a 0.35-μm CMOS process at room temperature. It is capable of sensing a capacitance range from 1.5 to 20 pF, which is adequate for the digital microfluidics control system in practice. The SAR-ADC achieves an ENOB of 7.46 while operating at 1-kHz. The total power consumption is 0.8 μW.

Fig. 5 shows the simulation results of the capacitance to digital conversion, with an input capacitance ranging from 1.5 pF to 20 pF. The corresponding output codes vary from 51 to 231. The non-linear conversion characteristic as described in (5) can be readily observed. The highest conversion error as observed in simulation is 2.6% at 20 pF. This error can be tolerated in most digital microfluidics control system where accurate capacitance measurement is usually not required.

The charge injection and leakage current induced by switches in the interface circuit limit the accuracy of the designed CDC. These errors can be partly compensated by the

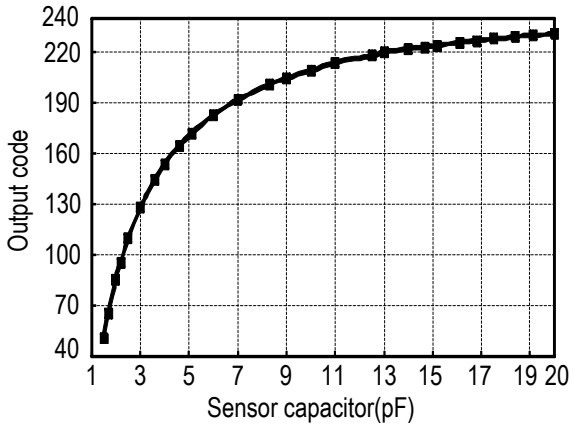


Fig. 5 The simulation results of the capacitance to digital conversion.

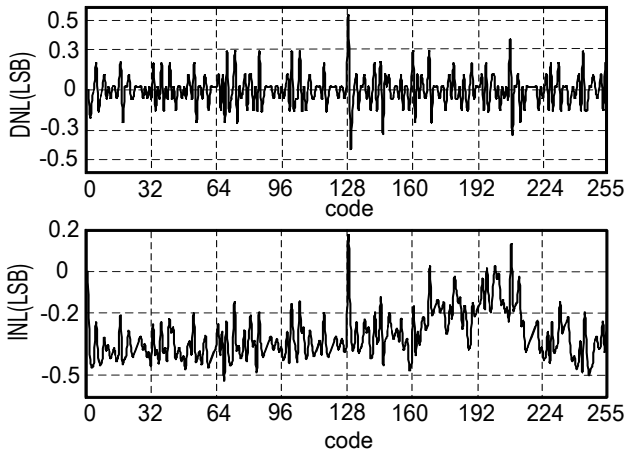


Fig. 6 INL and DNL of the current-mode SAR ADC.

use of dummy switches (i.e. S_5 and S_6). The use of differential SAR ADC can also reduce these common-mode errors during Ic_r and Ic_s sample-and-hold operation. Simulation results show that the induced error can be limited to less than 1LSB when compared to theoretical values.

Fig. 6 shows the INL and DNL plots for the current-mode SAR ADC. In our design, the maximum DNL is +0.54/-0.40, and the maximum INL is +0.18/-0.49.

Although all results were obtained via simulations, a preliminary comparison with similar prior arts can also be made (Table I). By using direct capacitance-to-current conversion and differential current-mode SAR ADC, the designed CDC exhibits a much larger capacitance sensing range while drawing much lower power.

IV. Conclusions

This paper presents an ultra-low-power CDC for digital microfluidics systems that demand a wide capacitive sensing range. A switched-capacitor capacitance-to-current front-end interface followed by a differential current-mode SAR ADC effectively realizes A/D conversion with small power (0.8 μW). The CDC designed in 0.35-μm CMOS with 8-bit resolution achieved 7.46 bit ENOB (of SAR ADC) at 1-kS/s operation frequency. The capacitance sensing range is from 1.5 to 20 pF.

Table I.
COMPARISON WITH PREVIOUS WORKS

	[4] TIM'09	[5] TIM'12	[6] ASSCC'07	This work
Architecture	C-V interface	C-F and PWM	Charge Redistribution	C-I and SAR ADC
CMOS Technology	0.8μm	0.35 μm	0.18 μm	0.35 μm
Supply Voltage	5 V	3 V	1.4 V	5 V,1 V
Resolution	N/A	9.3 bit	8bit (6.83)	8 bit (7.46)*
Conversion Speed	500 kS/s	25 kS/s	262 kS/s	1 kS/s
Power	725 μW	54μW	236.6 μW	0.8 μW
Cap. Range	1-1.75 pF	2.5-2.8 pF	50-53 pF	1.5-20 pF

* ENOB of the current-mode SAR ADC at room temperature.

Acknowledgement

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