25.5 A 1.7mW 0.22mm² 2.4GHz ZigBee RX Exploiting a Current-Reuse Blixer + Hybrid Filter Topology in 65nm CMOS

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Nanoscale CMOS offers sufficiently high f_t and low V_t favoring the design of ultra-low-power wireless receivers (RX) via stacking the RF-to-BB functions in one cell, while sharing the smallest possible bias current. Also, the signals can be conveyed in the current domain to enhance the area efficiency (i.e., no AC-coupling capacitor), RF bandwidth and linearity at those inner nodes. The 2.4GHz LMV cell [1] for ZigBee RX is an example that unifies one LNA, two mixers (I/Q) and one VCO. The power is low (2.4mW), but the NF, gain and S_{11} are sensitive to its external high-Q inductor that performs narrowband input match and passive gain boost. Although one VCO (i.e., one inductor) can save area and power, the I/Q generator has to be placed in the RF path. Realized as a g_m-C network, it suffers from a 3dB gain loss deteriorating the RX NF (12dB), while rendering the I/Q accuracy more susceptible to process variation.

The QLMV cell [2] for GPS RX facilitates I/Q generation via adopting a QVCO. Although its power is further optimized (1mW), three on-chip inductors and one off-chip balun are entailed, penalizing both die area and cost. In any case, both LMV and QLMV cells only can generate a 50%-duty-cycle LO for the mixing, which is less effective than its 25%-duty-cycle counterpart in terms of gain (i.e., 3dB higher), NF and I/Q isolation [3]. Finally, as their channel selection and image rejection are out of their current-reuse paths, any out-channel blocker will be converted into the voltage domain before adequate filtering, constituting a hard tradeoff between noise, linearity and power (i.e., 1.2mW BB power in [1] and 5.2mW BB power in [2]).

This paper describes a zero-external-component 2.4GHz ZigBee RX (Fig. 25.5.1) with 1.7mW RF-to-BB power and 0.22mm² active area. The RF signal (V_{RF}) is pre-gained by a low-Q passive network to ensure a wideband S_{11}. A Blixer (Balun-LNA plus I/Q mixers) amplifies and downconverts the current signal to a 2MHz IF. Out-channel blockers are immediately filtered in the current domain by a hybrid filter, which is stacked atop the Blixer for current reuse. A non-cascode high-swing VGA drives a 3-stage RC-CR polyphase filter (PPF) for robust image rejection. The final stage is an inverter amplifier. An LO generator creates a 25%-duty-cycle 4-phase output using a wideband div-by-2 (DIV1) and an external reference LO (LO_{ext}). A div-by-4 (DIV1+DIV2) and a 10GHz VCO are also integrated for additional testability.

The Blixer (Fig. 25.5.2) features a passive-/active-gain-boosting technique. The passive part is based on a low-Q and compact (0.048mm²) 4.16nH inductor (L_M) and tapped capacitors (C_p and C_M) for impedance downconversion and resonance. L_M also serves as the bias inductor for M_1. C_p stands for the parasitic capacitance from the pad and ESD diodes. The achievable gain is determined by the ratio of $\sqrt{(R_P//R_{in})}$ and $\sqrt{Rs}$. The –3dB bandwidth given by ω_0/Q [$\omega_0=1/\sqrt{C_{eq}L_M}$ and $Q=(R_P//R_{in})/2\omega_0L_M$] benefits from a small Q being less sensitive to C_p. Together with the bondwire inductance (L_{BW}), ~4dB (simulation) passive gain boost is stably achieved. M_1 and M_2 are the common-gate and common-source amplifiers, respectively. The active gain boost is achieved via an AC-coupled self-biased inverter amplifier (A_{GB}). It generates a loop gain around M_1 to lower R_{in} and improve NF, while keeping the bias current of M_1 and M_2 small and equal. The small bias current allows more devices to be cascoded atop the Blixer even though the supply is just 1.2V (V_{DD12}). Differently, A_{GB} is separately powered at 0.6V (V_{DD06}) to enhance its g_m-to-current efficiency.

The I/Q mixers use a double-balanced structure. Long-channel MOS reduces the 1/f noise and V_t. Their small bias current (defined by M_1-M_2) reduces the entailed LO swing to succeed the current commutation, saving the LO-path's power. Unlike the balun-LNA in [4] that entails an extra balancer to correct the differential mismatch, here, the I/Q mixers driven by a 25%-duty-cycle 4-phase LO inherently perform differential and I/Q balancing.

A GHz-range div-by-2 is compact and wideband enough to generate a 4-phase LO with a duty cycle not necessarily 50%. Here, DIV1 accepts a 50%-duty-cycle 2-phase input, and delivers a 25%-duty-cycle 4-phase output. To save power, the LO generator is designed at a 0.6V supply. Since an LO amplitude of ~$0.4V_{pp}$ is optimum for the mixing in terms of gain and NF, while the buffered LO is as high as $0.6V_{pp}$, C_{LO} was added to create a capacitor divider with $C_{MIX,in}$ (input capacitance of the mixer). This act brings down the equivalent load ($C_{L,eq}$) of the LO buffer by ~33% for power savings.

A current-domain Biquad [5] can be stacked atop the I/Q mixers for effective filtering [4]. However, its noise-shaping zero is located at DC, unsuitable for low-IF RX. The proposed Biquad uses an active inductor (L_{act}) to realize IF-noise-shaping (Fig. 25.5.3). M_{i1}-M_{i4} feature an equal $g_{m,act}$ realizing $L_{act}\approx C_i/g_{m,act}^2$. The $L_{act}C_{f1}$ resonance shifts the noise-shaping zero to the 2MHz IF, with the channel bandwidth spanning from 1 to 3MHz. Interestingly, L_{act} also serves as a current-domain AC-coupler suppressing the 1/f noise of the Blixer. At the resonant frequency, the noise reduction is mainly determined by L_{act}'s Q and the source-node impedance of M_{f1}-M_{f2}. At high frequency, the pole g_{mf1}/C_{f1} forces most of the M_{f1}-M_{f2}'s noise to be absorbed by C_{f1}.

Unlike the original Blixer [3] that uses an RC load, the proposed "load" synthesizes a 1st-order complex pole (Fig. 25.5.4). R_L comes from the diode-connected M_L realizing the real part, and $g_{m,Mc}$ comes from the I/Q-cross-connected M_C realizing the imaginary part. Together with the Biquad (Fig. 25.5.3), 3rd-order channel selection and 1st-order image rejection are achieved. M_L and a segmented M_{VGA} also act as a current-mirror VGA handling the NF and linearity of the BB circuitry. Since the current-mode Biquad (Fig. 25.5.3) already offers two poles, the linearity of the VGA is relaxed. Outside the current-reuse path, the BB circuitry furthers the image rejection (>50dB in corner simulations) and signal amplification. Thanks to the small span (f_{max}/f_{min}=3) of the image band, large resistors (~150kΩ) and small capacitors (~0.47pF) are allowed in the PPF to save area.

The RX, fabricated in 65nm CMOS is optimized at 0.6V and 1.2V supplies. Since there is no frequency synthesizer, the results in Fig. 25.5.5 were measured under LO_{ext}. The –10dB S_{11}-BW is ~1.3GHz in packaged and chip-on-board tests. Thus, both gain (55 to 57dB) and NF (8.3 to 11.3dB) are wide at RF, more immune to process variations. A two-tone test at [LO+12MHz, LO+22MHz] shows an IIP3 of –6dBm at a maximum gain of 57dB. The asymmetric IF response shows 22dB (43dB) rejection at the adjacent (alternate) channel, and 36dB IRR.

The chip summary is given in Fig. 25.5.6. The results obtained under a free-running 10GHz on-chip VCO are also included, but they are more sensitive to test uncertainties. Benchmarking with the prior art [1,2,6], this work succeeds in advancing the IIP3, power and area efficiencies, while offering a wideband S_{11} with zero external component. Fig. 25.5.7 shows the die micrograph.

Acknowledgements:
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References:
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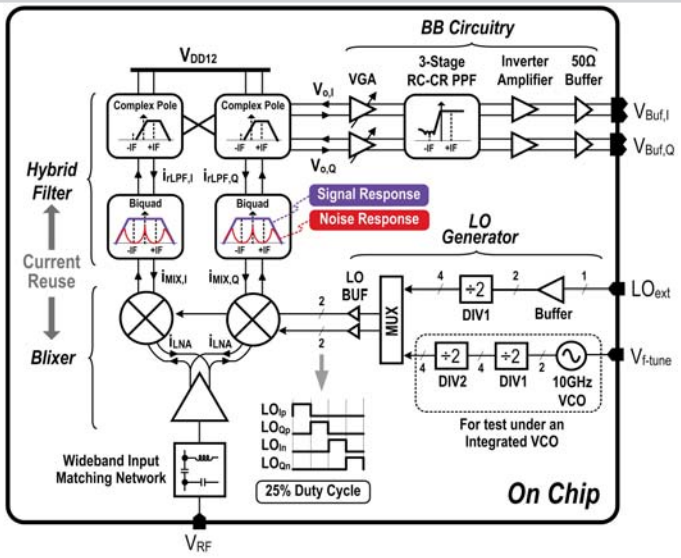

Figure 25.5.1: A 2.4GHz ZigBee RX.

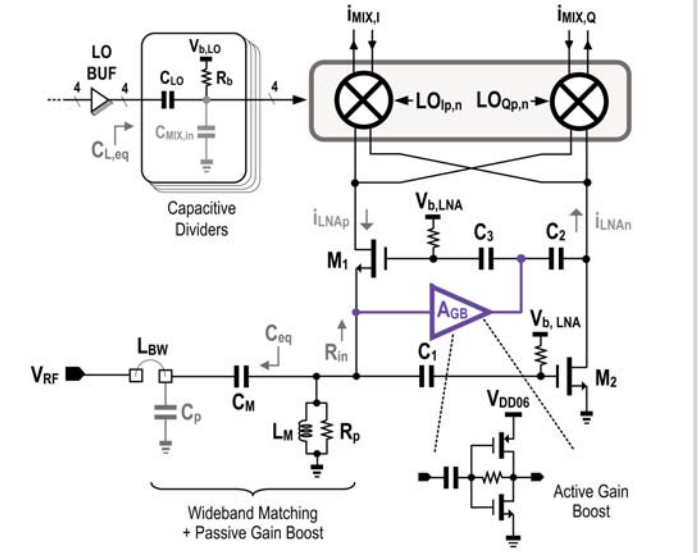

Figure 25.5.2: Blixer and LO generator.

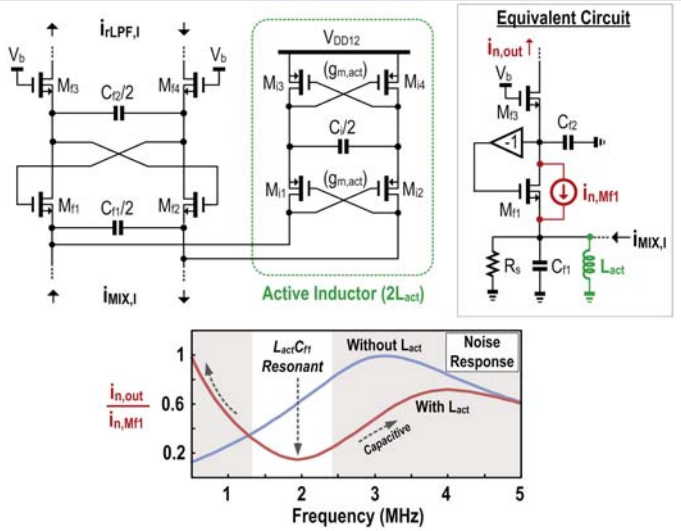

Figure 25.5.3: IF-noise-shaping Biquad. The $L_{act}C_{f1}$ resonance shifts the noise-shaping zero to the 2MHz IF.

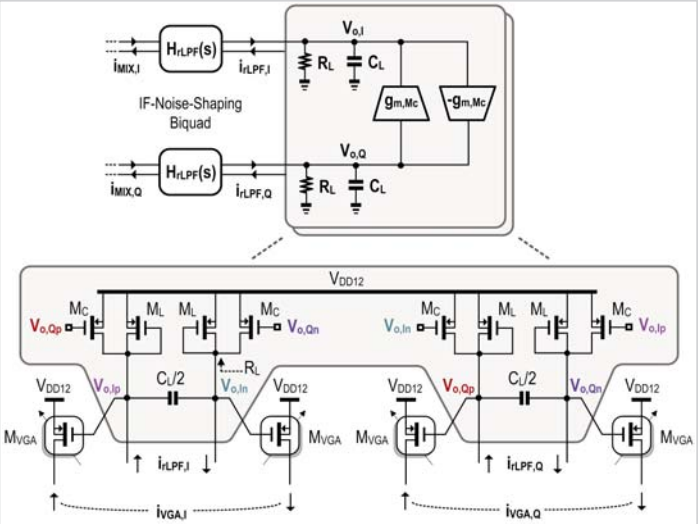

Figure 25.5.4: Complex-pole load. Upper: Block diagram. Lower: Schematic. M_L and M_{VGA} also form a current-mirror VGA.

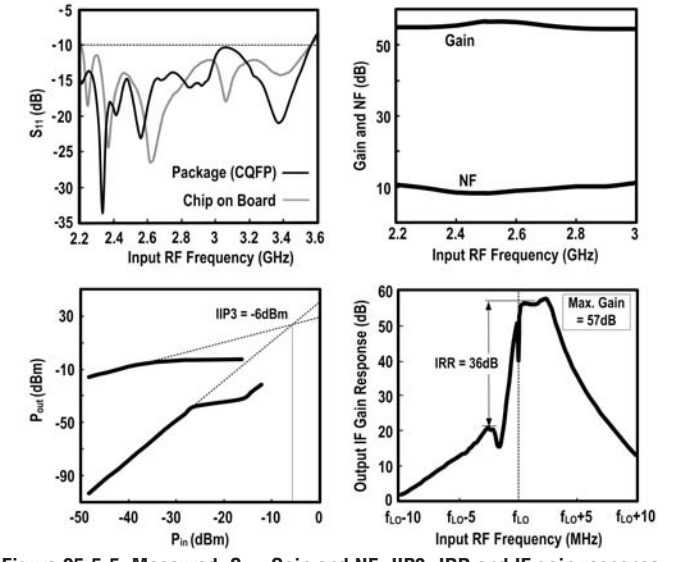

Figure 25.5.5: Measured: S_{11}, Gain and NF, IIP3, IRR and IF gain response.

	This Work		ISSCC'08 [1]	JSSC Mar.'10 [6] *	JSSC Mar.'10 [2]
Standard	ZigBee		ZigBee	ZigBee/Bluetooth	GPS
Architecture	Blixer + Hybrid-Filter + Passive RC-CR PPF *(1 Biquad + 4 complex poles)*		LMV Cell + Complex Filter *(3 complex poles)*	LNA + Mixer + Complex Filter *(3 complex poles)*	QLMV Cell + Complex Filter *(2 complex poles)*
External Components	***zero***		one inductor & one capacitor	one inductor & one capacitor	one passive balun
S_{11} <-10dB BW (MHz)	***1300 (2.25 to 3.55 GHz)***		N/A	>400 (<2.2 to 2.6GHz)	100 (1.55 to 1.65 GHz)
Integrated Inductors	1	2	1	2	3
Integrated VCO	No	Yes	Yes	No	Yes
Gain (dB)	57	55	75	67	42.5
NF (dB)	8.5	9	12	16	6.5
$IIP3_{out\text{-}channel}$ (dBm)	***-6***	***-6***	-12.5	-10.5	-30
IRR (dB)	36 (worst of 5 chips)	28	35	32	37
LO-to-RF Leakage (dBm)	-61	-61	-60	N/A	-75
Power (mW)	***1.7***	***2.7***	3.6	20	6.2 (inc. ADC)
Active Area (mm^2)	***0.22***	***0.26***	0.35	1.45	1.5 (inc. ADC)
Supply Voltage (V)	0.6 and 1.2 (dual V_{DD})		1.2	0.6	1
Technology	65nm CMOS		90nm CMOS	90nm CMOS	130nm CMOS

* The frequency synthesizer is already excluded for fair comparison.

Figure 25.5.6: Chip summary and performance benchmarks.

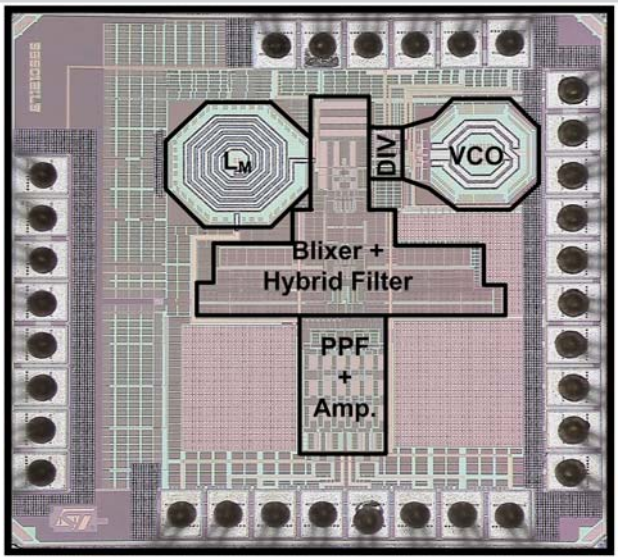

Figure 25.5.7: The RX die photo.

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