A Noise-Insensitive Offset Calibration Technique for Time Interleaved SAR ADC

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Abstract—**Digital calibration can be used to aid ADCs in improving their performances. In this paper a calibration method is proposed to reduce the effect of the channel offset mismatch in the time-interleaved ADC, with the calibration circuit in the digital domain. In order to avoid the circuit noise that degrades the calibration performance an averaging algorithm will be employed. A 12 bit two-channel time-interleaved SAR ADC is used to verify the calibration technique. The simulation results using a 65-nm CMOS process show that the calibration can reduce the offset between different channels and improve the SNDR.**

Key Words: Digital offset calibration, Noise averaging, Time interleaved ADC.

I. INTRODUCTION

Recently the CMOS technology is scaling down very quickly and digital circuits become faster and consume less power. On the other hand, the analog circuits continue to be difficult to implement. As a result, digital calibration is developing very fast as an aid instrument for better performance of analog circuits [1],[2]. As the technology scales further down the transistor sizes are smaller and the matching is poorer. For the input pair of both opamps and comparators this mismatch results in an input-referred offset. Traditionally, auto-zeroing techniques are used to deal with the offset. However, a digital calibration offers a better choice. For a time interleaved SAR ADC, if the comparators of different channels have different offset, there will be a channel offset mismatch which leads to a tone appearing at 1/N of sampling frequency, where N is the number of the interleaved channels [3]-[5]. These tones are the channel mismatch tones and will decrease the SNDR. So, for the time interleaved SAR ADC the offset between the channels must be calibrated.

In this paper, a digital offset calibration technique is proposed that can alleviate the offset mismatches between time-interleaved channels. The calibration circuit first measures the output codes of both channels when the input is nulled, then the difference of the code between channels can be found. However, usually due to the noise effect, the difference is not the actual offset because it is distorted with noise. The noise component will be stored in the difference between channels and becomes an additional static offset. Thus, the mismatch tone is not suppressed thoroughly. In this work, an average algorithm is applied when detecting the channel offset. Several samples are averaged to remove the noise effect. The offset after averaging is accurate enough to represent the true value. The calibration technique is very simple and straight forward and can be implemented on chip easily with only a little power consumption.

II. SAR ADC AND COMPARATOR OFFSET

The successive approximation ADC converts a continuous-time analog signal into a quantized digital code by binary search through all the possible quantization levels. The block diagram is shown in Fig.1.

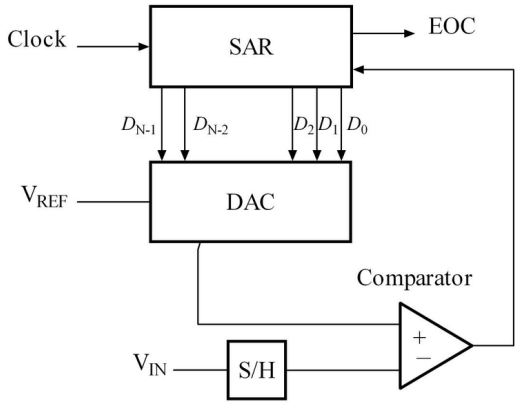

Fig.1 SAR ADC block diagram [1]

The SAR ADC basically contains four elements. A sample-and-hold block samples the input signal V_{in}. An analog comparator compares V_{in} to the output of the internal DAC and outputs the result of the comparison to the successive approximation register. A successive approximation register sub-circuit was designed to supply an approximate digital code of V_{in} to the internal DAC. An internal reference DAC that supplies the comparator with an analog voltage

equivalent of the digital code output of the SAR for comparison with V_{in} [1]. According to the operation of the SAR ADC, we know that the input referred offset of the comparator can be regarded as a DC input level shift. Therefore, the output codes have a DC level shift also.

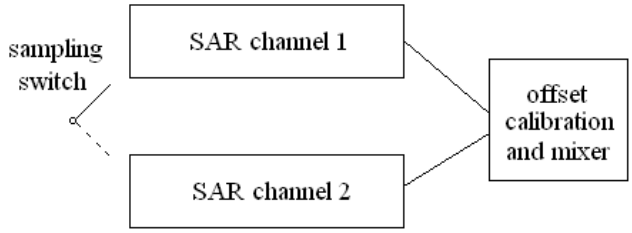

Fig.2 Time interleaved SAR block diagram

For a Time-Interleaved (TI) SAR ADC, the offset of the comparator is a DC offset between channels. The circuit block diagram of the TI-SAR ADC is shown in Fig.2. The input analog signal is sampled by a sampling switch which selects corresponding channel to quantize the signal. The digital code from both channel 1 and channel 2 cannot output directly. They should be passed through an offset calibration and mixer block, in which the offset between channels is first detected, and then an embedded adder is used to compensate the offset. After that, the compensated digital code passes a mixer circuit, so that a continuous quantized signal is obtained.

III. CALIBRATION ALGORITHM AND CIRCUIT

The idea of the proposed calibration method is to eliminate the offset between channels. So first of all, we have to know how much the channel offset is. This can be done with a detector circuit when the input of the ADC is grounded, then the output of each channel will be the offset value. However, because of the noise, the output is not the actual offset value. It may vary a little bit of amount, sometimes, it is 1LSB larger and sometimes it is 1LSB less, but the mean value is the still the channel offset. If only one output sample is taken as the offset value, the calibration is not accurate because the noise effect is included. To remove the noise effect, several samples instead of one are obtained and averaged. The average is close to the actual offset because the mean value is the channel offset. To find the average value easily in digital domain, eight samples are chosen. The block diagram of the calibration circuit is shown in Fig.3.

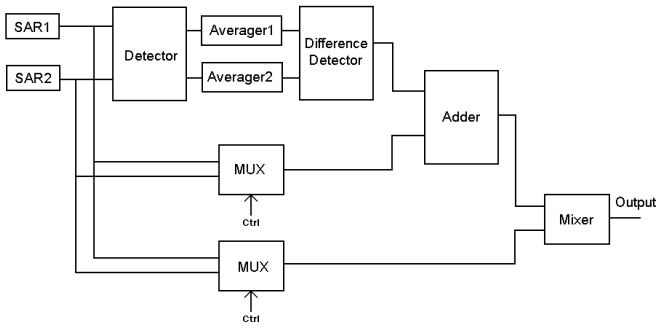

Fig.3 Block diagram of the calibration circuit.

In this calibration circuit, the channel offset is first extracted by a detector. Then we use a difference detector to find the difference of the offset between the two channels. After that, the difference is added to a channel which has a less offset, finally, the corrected code from two channels is mixed to give the final output.

The detector circuit is implemented by a set of D-flip-flops. The clock is synchronized with the SAR ADC channels. A counter is used to count for eight samples. After the eight samples are detected, they are delivered to an averager to take the average. The averager circuit is shown in Fig.4.

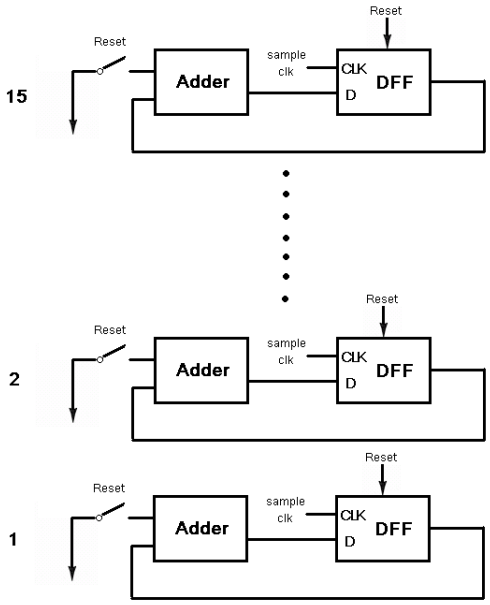

Fig.4 12-bit 8-samples averager.

Before the calibration circuit starts, the full adders and the D-flip-flops are reset. During the calibration, the 12-bit sample is first stored in the D-flip flop according to the sample clock. Since the DFF and the full adder are connected as a loop, the stored 1st sample is actually appeared at the output of the full adder. When the second sample clock comes, the DFF delay the 1st sample by one clock cycle and thus the full adder receives the second sample and adds to the first samples. There are totally 15 pairs of DFF and full adder. That is because we are taking average of 8 samples and the ADC has 12 bit resolution, if we sum all the 8 samples, it is a 15 bit code. After we get the sum of the samples, we need to do the division by 8. For a binary division, we can just remove the last three bits from the 15 bit code, so that we can get the averaged offset of the ADC channels.

When the offset values of channels are detected, the difference can be found. The next step is to find a correct channel to add the difference. There is the multiplexer to choose the channels. The control signal for the multiplexer can be generated by a 12 bit digital comparator. The 12 bit digital comparator is implemented by a 12 bit subtractor, the carrier determines which input is larger. After choosing the right channel, the difference of the channel offset is added, this completes the calibration. The final step is to mix the time

interleaved code to become a continuous ADC code. This is done by a simple mixer.

IV. CIRCUIT IMPLEMENTATION

The comparator is a key element in the SAR ADC. The precision and the noise performance of the comparator determine the ADC resolution. But we can add a pre-amplifier to improve the noise performance and reduce the kick back noise. However, the additional pre-amplifier stage dissipates additional static power. When the circuit is operating in a high speed, we need to add much more current to maintain the bandwidth of the pre-amplifier. This increases the total power dissipation of the ADC significantly. Therefore, in this project, a dynamic Lewis Gray comparator is utilized without the pre-amplifier. The circuit of the comparator is shown in Fig.5 [8].

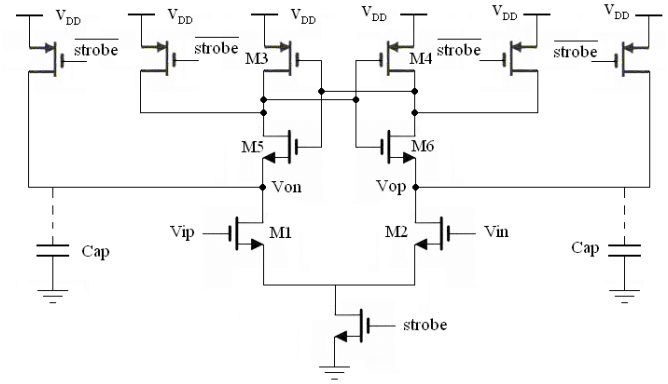

Fig.5 Dynamic comparator without pre-amp.

The M1 and M2 are input differential pair, and together with M3 and M4, they formed a positive feedback loop. When the strobe pulse is off, the output node and the drain of M5 and M6 are reset to V_{dd}, meanwhile, the gate of M5 and M6 is V_{dd}, so they are like an on-switch. When the strobe pulse is on, suppose the input Vip is larger than Vin, the Von is lower than Vop, so the drain of M6 or the gate of M3 becomes higher, the drain of M5 or the gate of M4 becomes lower. It makes the Von is lower that before and Vop is higher than before. The speed of the comparator is determined by the regeneration time which is actually the positive feedback time. Therefore, if we want to minimize the regeneration time, we need to minimize the transistors in positive feedback loop. However, for the input differential pair, we can not use the minimum size, because most of the offset are generated by the mismatch of the input differential pair. On the other hand, if the input differential pair is too large, the input capacitance becomes a problem for the capacitor DAC array. The Monte-Carlo simulation for the comparator is shown in Fig.6, which shows a 3-sigma offset of 23mV.

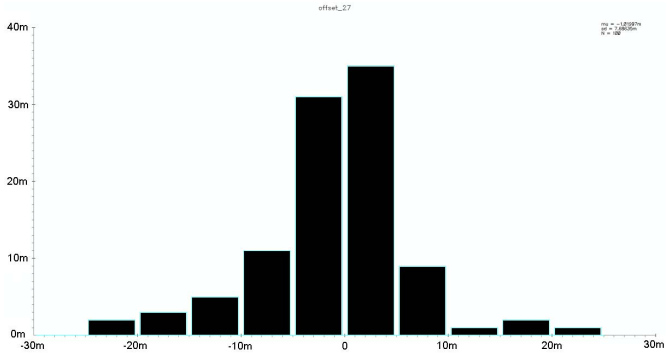

Fig.6 Monte-Carlo simulation of comparator.

Since we didn't add the pre-amplifier stage before the comparator, the noise may degrade the performance significantly. To reduce the noise effect, we can add a capacitor at the output node of the comparator. The additional capacitor can effectively suppress the noise but it makes the regeneration time be longer. Another problem is if there is some mismatch between the capacitor, it becomes the offset of the comparator. Fortunately, this problem can be eliminated by the calibration circuit.

There are some methods to calibrate the comparator offset in analog domain by adding a variable capacitor at the output node [9]. But this method will degrade the precision of the comparator. It does not suitable for a high resolution ADC. In this project, only digital circuit is added, there is no additional analog component introduced, so the comparator precision is not affected.

V. SIMULATION RESULTS

To verify the calibration technique, a 12-bit, 1V, 60MS/s two-channel time interleaved SAR ADC was designed in 65nm CMOS process. In the calibration mode, the ADC input is connected to common-mode V_{cm} so that the differential input is 0. When the calibration finishes, signals can be applied to the ADC. In this project, we used an average algorithm when we detect the channel offset. We used the Nyquist frequency signal input to do the test. Fig.7 shows the FFT both before and after calibration but average algorithm is not applied.

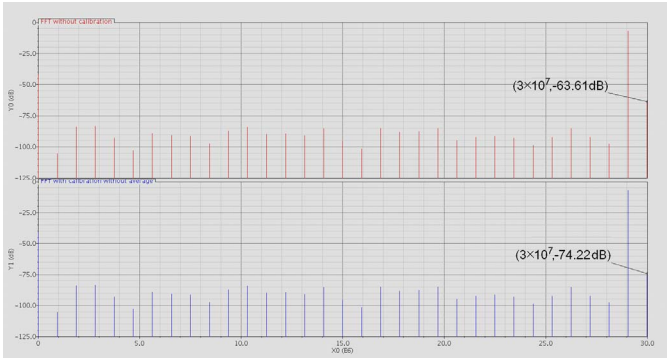

Fig.7 FFT before and after calibration without average.

Fig. 7 shows the FFT spectrum of the TI-ADC before and after calibration, without the averaging circuit enable. We can

see that before calibration, the mismatch tone is -63.61dB and after calibration, it becomes -74.22dB. There is 10.61dB improvement. The mismatch tone is not suppressed thoroughly because of the noise effect. Fig. 8 shows the corresponding FFT spectrum with the averaging circuit active. We can see that the mismatch tone is -64.07dB before the calibration. And after the calibration, it becomes -79.43dB. There is 15.36dB improvement. Comparing Fig.7 and Fig. 8, we can conclude that the average algorithm does improve the calibration accuracy. It can draw out the actual channel offset more precise from the noise-disturbed signal.

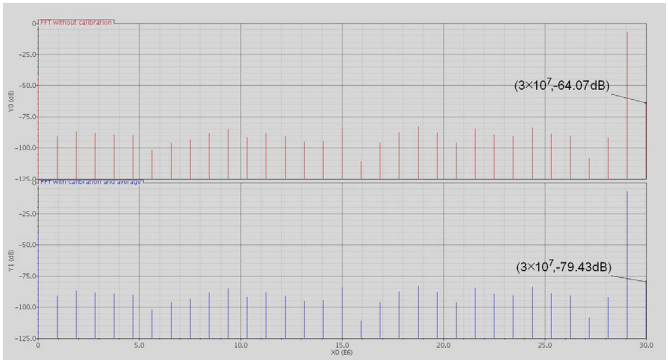

Fig.8 FFT before and after calibration with average.

The channel offset mismatch is a signal independent non-ideality in time interleaved ADC. It only gives a non-harmonic tone in the frequency spectrum. Therefore, this channel offset mismatch will not affect the linearity [6]. The INL and DNL is the same before and after the calibration, shown in Fig.9.

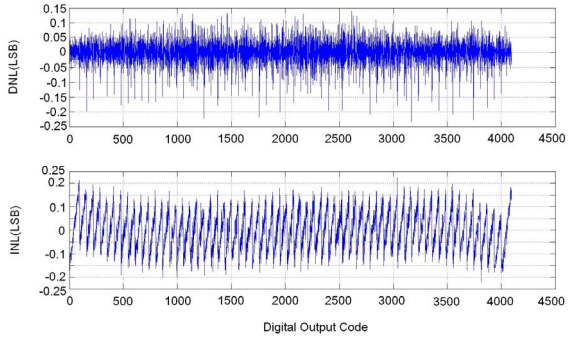

Fig.9 INL and DNL characterisitics.

The performance summary for the 2 channel time interleaved ADC and the calibration algorithm is shown as follows.

Resolution	12 bit
Sampling Frequency	60M S/s
SNDR without calibration	56.28dB
SNDR using calibration without averaging	64.13dB
SNDR using calibration with averaging	65.84dB
DNL	+0.15/-0.23 LSB
INL	+0.22/-0.23 LSB

Table.1 Performance summary.

VI. Conclusions

In this paper a noise-insensitive digital offset calibration technique is proposed for a time-interleaved ADC, which has been verified through the design of a 1V 12-bit, 60MS/s two-channel time interleaved SAR ADC. The average algorithm is employed during the detection of the channel offset and the simulation results show that it can suppress the noise effect when detecting the offset. Finally, it can improve the SNDR by 10dB when compared with the results without calibration.

Acknowledgment

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