# A 10-bit 1GS/s 4-Way TI SAR ADC with Tap-interpolated FIR Filter based Time Skew Calibration

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***Abstract*—This paper presents a 10-bit 1GS/s 4-way time-interleaved (TI) successive approximation register (SAR) analog-to-digital converter (ADC). To reduce the time skew among the TI channels, the master clock based sampling technique is adopted that can effectively suppress the interleaving spurs to -54dB at Nyquist input. Morever, a tap-interpolating fractional delay (TIFD) filters based time skew calibration technique is proposed, which operates at background and can further reduce the interleaving spurs to be less than -70dB. The prototype was fabricated in a 65nm CMOS technology. The measurement results show that the ADC operating at 1GS/s achieves a SNDR of 49.6dB and SFDR of 61.6dB at Nyquist input resulting in a figure of merit (FoM) of 32fJ/conversion-step.**

***Keywords—Time-interleaved, SAR ADCs, Time skew calibration***

## I. Introduction

SAR ADCs are the most power efficient architecture at hundreds of MS/s sampling rate due to its simple and digital dominant structure. To further boost the conversion speed to GHz range, the time-interleaved (TI) scheme is typically used [3], [5]-[6]. However, the TI SAR ADC suffers the mismatches from offset, gain and timing skew. The gain and offset mismatches can be easily solved in digital domain [8], while the time skew is the main design limitation. The digital overhead from the time skew calibration and clock distribution increase heavily. The digital time skew calibration based TI ADCs suffer from limited calibration range and considerable bandwidth scarification. The state-of-the-art TI SAR ADC [5] with digital background time skew calibration utilized the differentiating FIR filter to estimate and compensate and timing offset, which consumes large power and area overhead.

This paper presents a 1GS/s 10-bit 4-way TI SAR ADC achieves 458MHz bandwidth with 49.6dB SNDR. The channel-selection-embedded bootstrap technique [9] is utilized that synchronizes the sampling instants to the master clock, thus effectively suppressing the spurs from time skews below -54dB. To further compensate the residual time spurs, a TIFD FIR correction filter based calibration is proposed, which consumes less computation units and has less bandwidth constrain. The measured results show the proposed timing calibration can further suppress the spurs to be below -70dB.

## II. Overall ADC Architecture

The overall ADC architecture is shown in Fig. 1, which consists of 4-way sub-SAR ADCs operating at 250MS/s for an aggravate 1GS/s. To reduce the time skew, the sampling instant of each channel is only determined by the falling edge of the 1GS/s master clock $clk_s$, while the corresponding TI clock signals $\Phi_i$ ($i$=1, 2, 3, 4) are used to perform the channel selection [9]. The sub-channel SAR ADC is designed with 1-bit redundancy to relax the comparison accuracy in the leading bits. The outputs of ADC are followed by an encoding circuit (ENC) to obtain the final 10-bit. The offset errors are extracted and compensated by average and accumulation in digital domain[8]. The gain mismatch is tolerated by intrinsic capacitor matching and no gain calibration is used in this design.

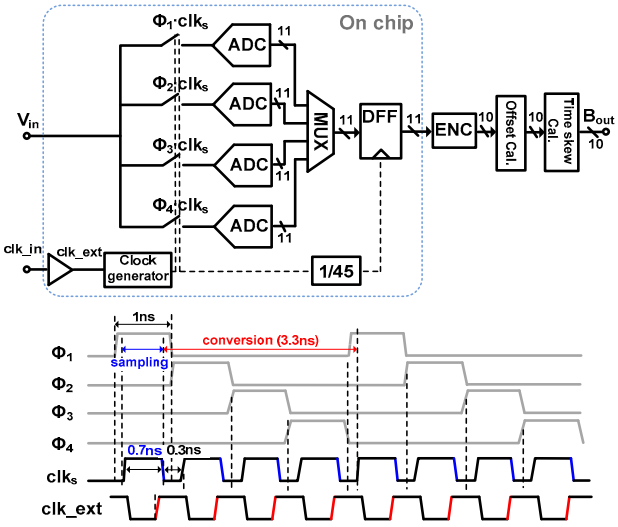


Fig. 1 Four-way TI SAR ADC and its timing diagram.

The schematic of internal clock generator is shown in Fig. 2, where *clk_ext* is the external clock input. Signal $Q_1$ and $Q_2$ are generated by divide-by-2 and divide-by-4, respectively. The signal $clk_s$ is obtained from *clk_ext* with duty cycle changed. When $clk_s$ is high, one of four sub-channels operates in sampling phase. Using $Q_1$ and $Q_2$, the $\Phi_i$ ($i$=1, 2, 3, 4) can be generated through AND gates shown in Fig. 2. In this design, the rising edge of the buffered *clk_ext* goes through only one NAND gate to generate the falling edge of $clk_s$ (shown in Fig. 2), introducing less additional clock jitter. The schematic of channel-selection-embedded bootstrap circuit for sampling switch is shown in Fig. 3. When $\Phi_i$ is high, the transistor M3 is turned-off and the NAND gate is enabled. The

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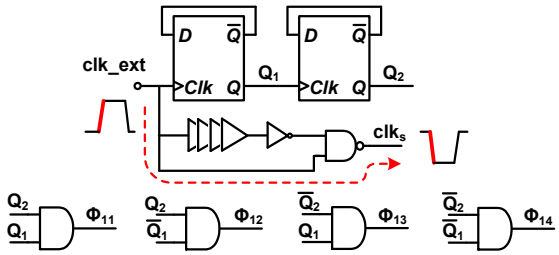


Fig. 2 Schematic of the internal clock generator.

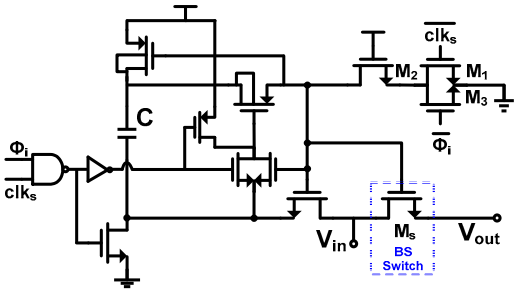


Fig. 3 Schematic of the channel-selection-embedded sampling switch.

corresponding bootstrapped switch $M_s$ is selected. The sampling instant could be further dominated by the falling edge of $clk_s$, which turns on the transistor M1 and disconnects the bootstrapped capacitor $C$. Although each channel is sampled by the same clock signal $clk_s$, there are still some time skew error sources, including threshold mismatch of the sampling switches (transistor $M_1$, $M_2$, $M_s$) and size mismatch after fabrication that could possibly limit the SFDR to be less than 60dB.

## III. Proposed Time Skew Calibration

Fractional delay filters could be utilized to compensate the time skew error in digital domain [1]. Supposing $T$ is the overall ADC sampling period, and $T_d=\alpha T$ represents the fractional delay. For conventional fractional delay filter based time skew calibration technique [1], the input signal bandwidth for calibration is limited to sub-channel sampling rate and the range of $\alpha$ could not be small due to large time skew introduced by the analog front-end sampling network. Benefiting from the time skew suppressed sampling scheme, the range of $a$ in this design could be constrained into around +/- 0.2% in simulation. The calibration of time skew is divided into two parts: detection and correction. The time skew detection technique in [7] is employed, which compares the mean value (by accumulation and average) of the multiplication of signals $x_m(n)$ in two adjacent channels to detect the polarity of time skew error $p(t_m)$ and updates the coefficients of fractional delay FIR filter $F(a_m)$ adaptively as shown in Fig. 4. For time skew correction, the proposed fractional delay FIR filter architecture is shown in Fig. 5, where only the second-channel ($m$=1) is illustrated and the length of FIR correction filter is $2N$+1 ($N$=2, 4, …) ($N$=2 in Fig. 5). The $\alpha$ indicates the time error to be compensated. $C_j$ =[$c_{j,0}$, $c_{j,1}$] ($j$=0, 1… 4) are the coefficients of TIFD filters. $I_{m,m+1}(n)$ is the interpolation filter to generate the interpolated tap between channel $m$ and channel $m$+1. $M$ is number of interleaved channels.

The coefficients $C$ could be updated adaptively according

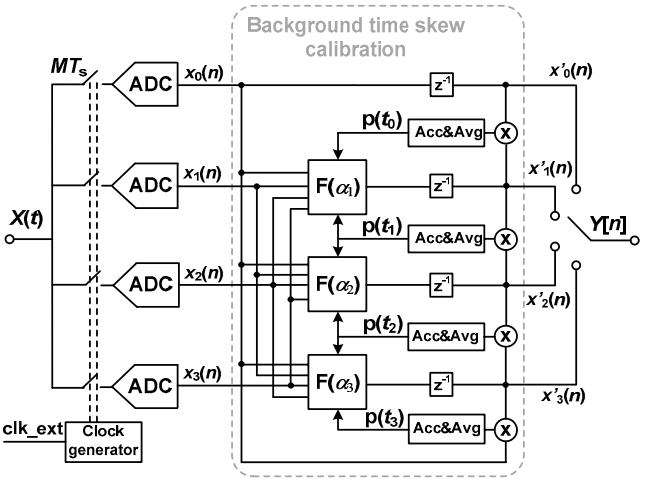


Fig. 4 The architecture of the proposed digital background time skew calibration.

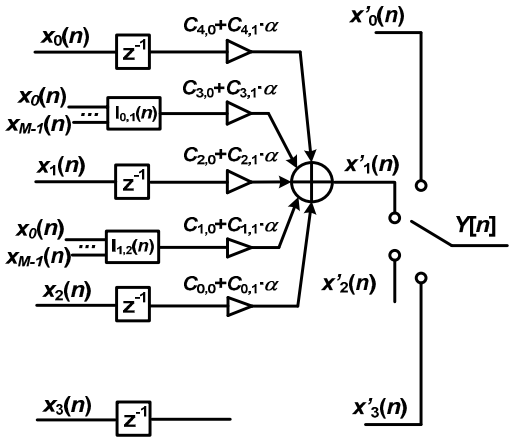


Fig. 5 The structure of FIR correction filter in a four-channel TI-ADC, where only the second-channel is illustrated and $N$=2.

to detected time skew error $\alpha$. The coefficients are approximated by linear polynomials of $\alpha$. The approximation error is

$$e(\omega,\alpha)=F(\omega,a)-D(\omega,a)\,, \tag{1}$$

where

$$F(\omega,a)=\sum_{n=0}^{N}(c_{2n,0}+\alpha c_{2n,1})e^{-j\omega(n+\frac{K-N}{2})T} + \sum_{n=0}^{N-1}(c_{2n+1,0}+\alpha c_{2n+1,1})\sum_{k=0}^{K-1}e^{-j\omega(k+n)T} \tag{2}$$

and

$$D(\omega,a)=e^{-j\omega(\alpha+\frac{K}{2})T}\,. \tag{3}$$

$F(\omega,\alpha)$ and $D(\omega,\alpha)$ are the transfer function of the TIFD filter and the ideal fractional delay function, respectively. Variable $K$ ($K$=2, 4, …) is the length of interpolation FIR filter. For ideal fractional delay filter, $\alpha$ and $K/2$ are the factional and integral delay respectively. The approximation error is minimized by using certain criterion. The TIFD FIR filter coefficients vector is $C$=[$c_{0,0}$, $c_{0,1}$, $c_{1,0}$, $c_{1,1}$, …, $c_{2N,0}$, $c_{2N,1}$], whose length is $4N$+2, are to be optimized. The transfer function $F(\omega,\alpha)$ of the FIR filter can be rewritten as

TABLE I: Performance Comparison of Digital Calibration

| | Filter Length (taps) | Bandwidth Penalty | Error (dB) | Adaptive |
|---|---|---|---|---|
| [1] | 60 | 10% | -72 | No |
| [2] | 75+30 | 33% | -72 | Yes |
| [5] | - | 9.25% | -70 | No |
| This work | 38+5 | 5% | -70 | Yes |

$$F(\omega,a)=C\cdot(c(\omega)-js(\omega))^{\mathrm{T}}, \tag{4}$$

where

$c(\omega)$=[cos((*K*/2-1) $\omega$), cos((*K*/2-1) $\omega$), $\sum_{k=0}^{K-1}\cos(k\omega)$, $\sum_{k=0}^{K-1}\cos(k\omega)$, …, $\sum_{k=0}^{K-1}\cos((k+N\text{-}1)\omega)$, $\sum_{k=0}^{K-1}\cos((k+N\text{-}1)\omega)$, cos((*K*/2-1+*N*) $\omega$), cos((*K*/2-1+*N*) $\omega$)],

and

$s(\omega)$=[sin((*K*/2-1) $\omega$), sin((*K*/2-1) $\omega$), $\sum_{k=0}^{K-1}\sin(k\omega)$, $\sum_{k=0}^{K-1}\sin(k\omega)$, …, $\sum_{k=0}^{K-1}\sin((k+N\text{-}1)\omega)$, $\sum_{k=0}^{K-1}\sin((k+N\text{-}1)\omega)$, sin((*K*/2-1+*N*) $\omega$), sin((*K*/2-1+*N*) $\omega$)].

To minimize the approximation error, the following min-max problem need be solved:

$$\min_{C_{n,m}}\{\max|e(\omega,\alpha)|\},\qquad \omega\in\Omega,\ \alpha\in\mathrm{A} \tag{5}$$

where $C_{n,m}$ contains all the filter coefficients to be optimized. $\Omega$ and A are the ranges of frequency band and time delay for optimization respectively. The objective in (1) can be written as

$$\begin{aligned}&|e(\omega,\alpha)|\\&=|F(\omega,\alpha)-D(\omega,\alpha)|\\&=\left\|\begin{bmatrix}R^{F}(\omega,\alpha)\cdot C^{\mathrm{T}}-R^{D}(\omega,\alpha)\\ I^{F}(\omega,\alpha)\cdot C^{\mathrm{T}}-I^{D}(\omega,\alpha)\end{bmatrix}\right\|_2\\&=[R^{FD}(\omega,\alpha)^2+I^{FD}(\omega,\alpha)^2]^{1/2}\end{aligned} \tag{6}$$

where

$$\begin{aligned}&R^{D}(\omega,\alpha)=[D(\omega,\alpha)]_R,\ I^{D}(\omega,\alpha)=[D(\omega,\alpha)]_I\\&R^{F}(\omega,\alpha)=[(c(\omega)-js(\omega))]_R\\&I^{F}(\omega,\alpha)=[(c(\omega)-js(\omega))]_I\\&R^{FD}(\omega,\alpha)=R^{F}(\omega,\alpha)\cdot C^{\mathrm{T}}-R^{D}(\omega,\alpha)\\&I^{FD}(\omega,\alpha)=I^{F}(\omega,\alpha)\cdot C^{\mathrm{T}}-I^{D}(\omega,\alpha)\end{aligned}$$

Here $[\cdot]_R$ and $[\cdot]_I$ represent the real and imaginary parts of a complex number or vector respectively. Therefore, the min-max problem can be reformulated as

$$\min_{C}\ \delta \tag{7}$$

$$\text{subject to}\ \ \delta-[R^{FD}(\omega,\alpha)^2+I^{FD}(\omega,\alpha)^2]^{1/2}\geq 0\,.$$

The above optimization problem within a given range of frequency $\omega$ and fractional delay value $\alpha$ could be solved by a standard SOCP solver. To save calibration cost, multiplier-less realization of digital filters is employed. For instance, a 38-tap interpolation filter could be realized by using only 55 full adders. As shown in Table I, with 38-tap interpolation filter and 5-tap TIFD filter, a -70dB error level could be obtained with only 5% bandwidth scarified.

## IV. SUB-CHANNEL SAR ADC

The architecture of the non-binary SAR ADC is shown in Fig. 6, and 11 conversion cycles are needed including one redundant bit. The non-binary weights $D_{10}$~$D_0$ are 384, 288, 168, 88, 46, 24, 12, 6, 4, 2, 1. The numbers of redundant LSB $d_i$ ($i$=1, 2, …11) of each cycle are set to the powers of 2. In this design, the value of $d_i$ ($i$=1, 2, …11) are set to 128, 32, 8, 4, 2, 1, 1, 1, 0, 0, 0. With the different constraints of error tolerance range, the redundant value of each cycle and the number of redundant cycles could be properly chosen. The adder based encoding circuit is utilized that converts the ADC output with redundancy to binary codes. Only 12 full adders (FA), 8 half adders (HA) and 1 OR gate are used to build the encoding circuit resulting in low power consumption and less design complexity.

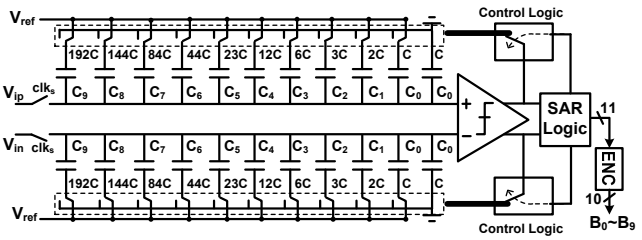


Fig. 6 Proposed non-binary high speed SAR ADC architecture.

## V. MEASUREMENT RESULTS

The ADC is fabricated in a 1P9M 65nm CMOS process with low-$V_{th}$ option. The die photo is shown in Fig. 7, and the ADC core occupied 300μm x 100μm (0.03mm$^2$). The power consumption is 7.95mW (excluding the offset and time skew calibrations) at 1.2V power supply when operating at 1GS/s. The offset mismatch and background time skew calibration are implemented off-chip, of which the estimated power consumption is 8mW and the area is 0.038mm$^2$ with 39600 gate count. The measured DNL and INL are shown in Fig. 7. The DNL and INL is +1.2/-0.7 LSBs and +1.3/-1.2 LSBs, respectively. The measured FFT at Nyquist input is shown in Fig. 8. Before calibrations, the offset mismatch limits the SNDR and SFDR to 36.2dB and 36.4dB, respectively. The interleaving spurs are around 54dB (0.6ps *rms* equivalently). After enabling both offset and timing calibrations, the offset spurs are suppressed below -75dB and the interleaving spurs are all below -70dB, which significantly improves the SNDR to 49.6dB. The 3rd harmonic dominates the SFDR to 61.6dB. The length of TIFD filter and interpolation filter are set as 5 and 38 respectively. The coefficients of TIFD filter are listed in Table II. Assuming the first channel as the reference channel, the measured sampling switch mismatch caused time skew of other 3 channels in one chip are -0.6ps, 0.1ps and -1.5ps. The iterative time step $T_{\mathrm{step}}$ for the adaptive calibration is set to 0.1ps. Fig. 9 illustrates the dynamic performance of the ADC. The performance summary and comparison with state-of-the-art ADCs is shown in Table III. The proposed ADC achieves an excellent FoM of 32fJ with competitive conversion accuracy.

## VI. CONCLUSION

This paper reported a 10-bit 4-way TI SAR ADC that achieves a sampling rate up to 1GS/s and 49.6dB SNDR at Nyquist input. The master clock based sampling network is adopted to reduce the interleaving spurs and the proposed TIFD filters based time skew calibration can effectively compensates the remaining timing error to be lower than -

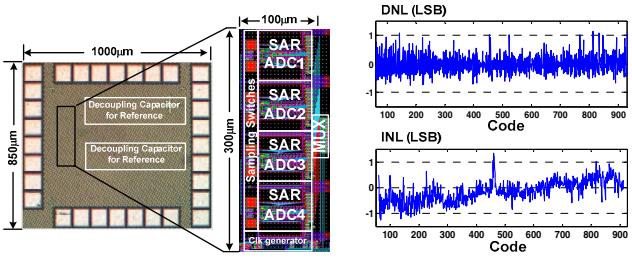


Fig. 7 Chip micrograph and layout, and measured DNL & INL.

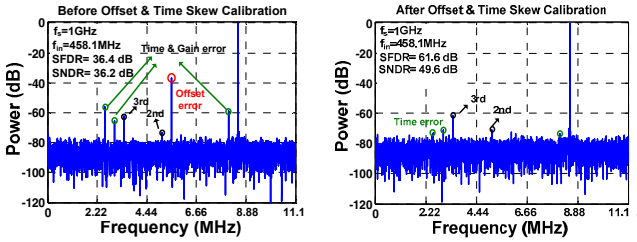


Fig. 8 Measured 8192-point FFT (digital output is decimated by 45) with $f_{in}$=458.1MHz before and after offset calibration.

70dB. This design exhibits lower calibration complexity and achieves higher efficiency in terms of power and area consumption, when compared with the state-of-the-art ADCs.

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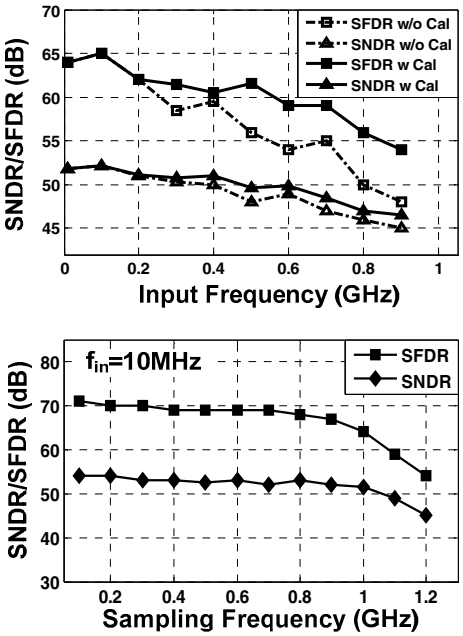


Fig. 9 SFDR and SNDR versus input frequency at $f_s$=1GHz and $V_{dd}$=1.2V. and SFDR and SNDR versus sampling frequency at $f_{in}$=10MHz and $V_{dd}$=1.2V.

TABLE II: Optimized TIFD Filter Coefficients

| $C_{n,m}$ | $m$=0 | $m$=1 |
|---|---|---|
| $n$=0 | -3.5e-7 (0) | 0.2674 |
| $n$=1 | 4.1e-6 (0) | -1.4923 |
| $n$=2 | 1 | -7.3e-13 (0) |
| $n$=3 | 4.1e-6 (0) | 1.4923 |
| $n$=4 | -3.5e-7 (0) | -0.2674 |

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TABLE III: Comparison of State-of-the-Art GHz ADCs

| | JSSC 2013[3] | JSSC 2014[4] | ISSCC 2014[5] | ISSCC 2014[6] | This Work |
|---|---|---|---|---|---|
| Architecture | TI-SAR | Pipe-line | TI-SAR | Flash+TI-SAR | TI-SAR |
| Time skew calibration | On-chip | No | On-chip | Off-chip | Off-chip |
| Technology (nm) | 65 | 65 | 40 | 65 | 65 |
| Supply voltage(V) | 1.2 | 1.0 | 1.1 | 1.0 | 1.2 |
| Power (mW) | 44.6 | 7.1 | 93 | 18.9 | 15.95* |
| Fs (GS/s) | 2.8 | 1.0 | 1.6 | 1.0 | 1.0 |
| Resolution(bit) | 11 | 9 | 9 | 10 | 10 |
| SNDR@ Nyquist(dB) | 48.2 | 47.7 | 48.0 | 51.4 | 49.6 |
| FoM (fJ/con-step) | 75.8 | 35.6 | 283 | 62.3 | 63 |
| Active Area ($mm^2$) | 1.7 | 0.1 | 0.83 | 0.78 | 0.068* |

* Including estimated power and active area used for the offset and time skew calibrations.