A 5-bit 2 GS/s Binary-Search ADC with Charge-Steering Comparators

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***Abstract*—This paper presents a 5-bit 2GS/s binary-search ADC. The proposed architecture prevents the use of a decoder to avoid the path delay racing between control signals and clock phases; thence the bit latency reduces to 1 single comparator delay only. We also propose a dynamic charge-steering comparator to quantize each bit quickly. Besides, we present well-balanced 1-of-N-to-Binary encoders to transform the output code with low power. This ADC consumes 3.9mW at 2GS/s in 65nm CMOS. It achieves a SNDR of 28 dB at Nyquist rate resulting in a FoM of 95 fJ /conv.-step.**

Keywords—binary-search ADC; asynchronous; charge-steering.

I. INTRODUCTION

Communication systems such as wireless local area networks (WLANs), optical Ethernet, electrical wireline links, etc. require high-speed and low-power ADCs. Flash ADC is often the choice due to its high conversion speed, but it suffers from relatively large power consumption and large area. Binary-search (BS) ADC structure combines the characteristics of the successive approximation register (SAR) and the flash, which is another candidate to operate at high-speed but achieving low power and small area [1]-[4].

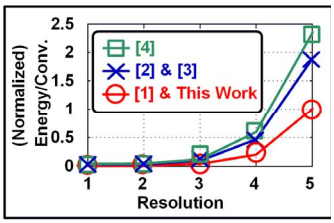
In the primitive BS scheme [1], its energy consumption, for a N-bit resolution, happens only during input sampling, reference charging, and N times the comparator operates in the whole conversion period. Because the common feature of BS ADCs [1]-[4] is that the reference voltages are applied early at the inputs of the comparators. Subsequently, various techniques [1]-[4] were reported to utilize less number of comparators by trading with the cost of a massively increased complexity of the reference pre-charging network and control logic in each bit stage. The extra power from the decoders is inevitable in those schemes [1]-[4]. Nevertheless, the control signal path due to the decoder delay is racing with the clock path of the comparator delay. Thus, the total settling time of the reference switching must be shorter than the comparison time in each bit stage [5]. Evidently, the trade-off penalty would always be the number of comparators versus power and speed.

In this paper, we propose a BS ADC architecture constituted by 2 BS sub-ADCs to reduce the number of comparators to $2^{N-1}+1$ for an N-bit resolution, and without an additional decoder. Fig. 1(a) shows a brief comparison of different BS ADC schemes. When compared with [1], a half number of comparators is saved. This resulted in a compact die size that is advantage to achieve both high-speed and low-power. When compared with [1]-[4], our structure also avoids the delay path racing and power consumption from the decoder. Fig. 1(b) depicts the behavioral model prediction of energy per conversion versus resolution for [1]-[4] and this work, estimated from the decoder with its logic gate count, switching network, and also including the thermal noise of the comparators [6]. It is obvious that this design achieved better energy efficiency when compared with [2]-[4] due to the reduced latency and power consumption.

Ref.	[1] JSCC'08	[2] ISSCC'09	[3] ASSCC'11	[4] ESSCIRC'15	This Work
Comp. Number	2^N-1	2N - 1	N	2N - 1	$2^{N-1}+1$ ≈Half of [1]
Decoder	No	Yes			No
Quantize Power	N Comp.	N Comp. + Decoder + Switch Network			N Comp.
Bit * Latency	$T_{CMP,1}$	$T_{CMP,1} + T_{OR} > T_{AND} + T_{RC,i+1}$			$T_{CMP,1}$

*Based on Analysis in [5]

(a)



(b)

Fig. 1. Different BS ADC schemes (a) Comparison, and (b) Energy per conversion versus resolution (all normalized to [1] & this work at 5-bit).

Since the bit latency is only given by a single comparator delay in this work, the speed of comparator is a significant design consideration. Typically, the latch-type sense amplifier [7] and the double tail latch [8] are the popular topologies for high-speed comparator designs, due to their dynamic operation schemes. Nevertheless, the delay of latch-type sense amplifier is rather dependent on the common-mode voltage [9]. And, the tail path in the double-tail latch allows its dynamic preamplifier outputs both collapsed to ground at clock start, leading to a slow response [10]. Recently, some high-speed comparators have been proposed to employ a slightly static cascaded preamplifier to raise the response speed of the latch in SAR ADCs [11][12]. However, they are not power efficient to applied for BS scheme, due to its operation characteristic.

Here, we propose a dynamic charge-steering comparator to quantize each bit swiftly. Besides, we also utilize well-balanced 1-of-N-to-Binary encoders to transform the binary output code with low power.

II. PROPOSED ADC ARCHITECTURE

Fig. 2 shows the architecture of the proposed 5-bit BS ADC composed by 3 conversion stages, a reference ladder, 1-of-N encoders, and a clock generator. The 1st stage comprises of a passive S/H and a comparator COMP1. The 2nd stage is constituted by an upper comparator COMP2U and a lower comparator COMP2L with their own passive S/Hs. The 3rd stage comprises two 3b BS sub-ADCs CBS1 and CBS2. The proposed BS ADC operates in a fully asynchronous conversion from the 1st to the 3rd stage. The clock generator only produces 3 phases including the sampling phase Φ_S, the hold phase Φ_H, and the 1st stage comparator triggering phase Φ_1, leading to low power dissipation. During the sampling phase (Φ_S=1), the S/Hs of the three stages sample the input signal simultaneously. In the hold phase (Φ_H=1), the S/Hs of the 1st and 2nd stages

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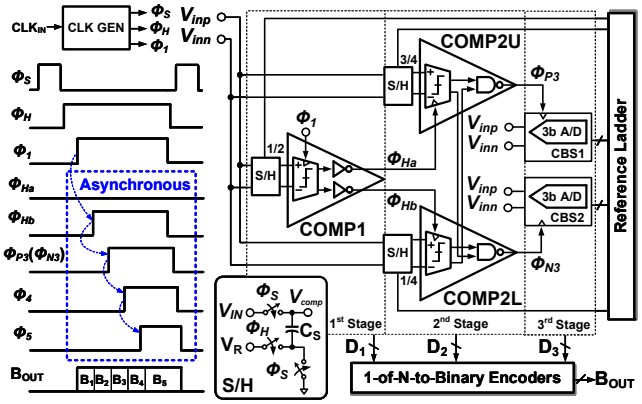


Fig. 2. Proposed ADC architecture with its timing diagram.

generate the residues by subtracting the sampled input signal with fixed references 1/2, 1/4 and 3/4 from the reference ladder. The quantization starts in the first stage at the rising edge of Φ_1. COMP1 is activated to quantize the MSB result. And then, one of the triggering phases Φ_{Ha} or Φ_{Hb} is attained to control COMP2U or COMP2L in the 2nd stage to quantize the 2nd bit output. Further, Φ_{Ha} and Φ_{Hb} are also the hold phases of CBS1 and CBS2 in the 3rd stage. Since the 1st, 2nd and 3rd stages quantize the digital outputs D_1, D_2 and D_3 in 1-of-N format, the 1-of-N-to-Binary encoders transform D_1, D_2, and D_3 to a 5-bit binary code output B_{OUT}.

In the primitive BS scheme [1], 4 comparators with reference voltages of 1/8, 3/8, 5/8 and 7/8 are ready in the 3rd bit step. Apparently, if MSB = 0, only two comparators with reference voltages of 1/8 and 3/8 are useful, and they can anticipate the selection since MSB is known before. In our proposed structure, the reference voltages of the 3rd stage no longer need to be prepared before the whole conversion starts, and they can be produced after the quantization of the 1st stage. Then, we can share 14 comparators with 28 reference voltages in the 3rd stage, consequently saving half of the comparators. Since we share the comparators with different pre-charged reference voltages, the output polarities of the comparison in the 2nd stage should be inverted while MSB = 0. Here, two NAND gates follow the outputs of COMP2U and COMP2L to match the selection principle of the binary-search algorithm. To simplify the logic, we merged two NAND gates into the last stages instead of the inverter pairs in COMP2U and COMP2L. The function of these NAND gates is to select CBS1 or CBS2 from the comparison result and, simultaneously, to provide sufficient driving capability. Here the dimension of the NAND gate is equal to the original inverter pair in the last-stage output of COMP1. Therefore, the bit latencies of the 1st and 2nd stages are almost the same as 1 comparator delay.

Fig. 3 shows the schematic of CBS1/ CBS2. There are 7 comparators connected as a 3-level binary tree. S/Hs are distributed with the comparators, which sampled the input signal during Φ_S=1. While the hold phase Φ_{Ha}/Φ_{Hb} is turned on, the corresponding reference voltages are switched to the S/Hs to be subtracted with the sampled input signal for quantization. The critical path is located at the first comparator of CBS1/CBS2. The voltage settling from the switching of references V_{RP1a}/V_{RP1b} and V_{RN1b}/V_{RN1b} must be faster than the rising edge of Φ_{P3}/Φ_{N3}. Since a single comparator delay from

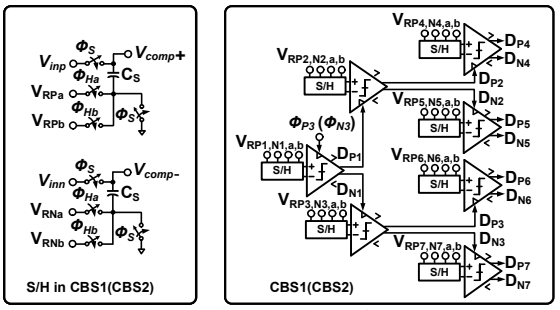


Fig. 3. Schematic of CBS1/CBS2.

COMP2U/COMP2L is occupied in this period, the time constraint can be given as,

$$T_{CMP,2} > T_{RC,1ab} \qquad (1)$$

where $T_{CMP,2}$ is the comparator delay of COMP2U/COMP2L, and the $T_{RC,1ab}$ is the RC settling time of the first S/H in CBS1/CBS2. Because of the distributed S/H, the equivalent settling capacitance is from the top plate parasitic of the sampling capacitance C_S in the S/H as well as the input capacitance of the comparator. In the design this capacitance is less than 2fF to be rapidly charged with a low power resistive ladder. Moreover, the main sampling capacitance C_S does not contribute to the reference settling time constant due to the reference level shifting operation at the high impedance node of the comparator input.

In overall the comparators count is significantly reduced, here, in 5 bit steps is 1, 2, 2, 4, 8, while it is 1, 2, 4, 8, 16 in [1], respectively. When compared to [1]-[4], we only reduce the comparator count at the 3rd-bit step, and thus avoid the extra decoder and massively increased switching network. Moreover, the path delay racing from the decoder is also prevented as well. The energy per conversion of the i-th-bit stage decoder for N-bit BS ADC can be given as [6]:

$$E_{dec} = [\sum_{i=4}^{N}(2^{i-1})\cdot(i-3)]\cdot C_{NAND}\cdot V_{DD}^2 \qquad (2)$$

where C_{NAND} is the parasitic capacitance of NAND gate. Obviously, the number of NAND gates is exponentially increasing with its resolution after the 3rd-bit quantization, leading to large power and delay.

III. Circuit Implementation

A. Charge-steering Comparator

In the proposed BS architecture, the total conversion period after input sampling is around 5 times the comparator delay. Therefore, shortening the comparator delay can further enhance the ADC speed. Since many comparators are not triggered in the BS scheme, dynamic operation of comparator design is the key consideration. On the other hand, the fast response of

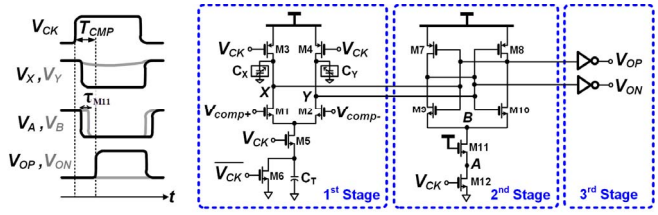


Fig. 4. Proposed charge-steering comparator with its operation waveforms.

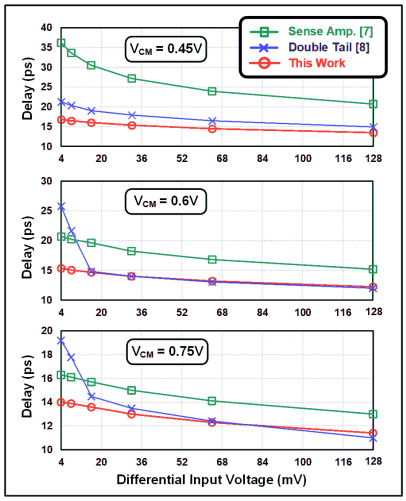


Fig. 5. Simulated comparator delays versus differential input at V_{CM} = 0.45V, 0.6V and 0.75V for different comparator schemes under 1.2V supply voltage.

comparator is not only related to speed, but also related to the metastability impact for the asynchronous clock phase generation.

Fig. 4 shows the proposed charge-steering comparator comprising 3 stages. The 1st stage serves as a charge-steering preamplifier, the 2nd stage works as a cross-coupled regenerative latch, and finally, the 3rd stage is a CMOS inverter pair to provide the driving capability. Differential capacitor banks C_X and C_Y are dedicated to offset voltage foreground calibration [3]. Since the charge source of C_T is equivalent to a tail current source during the amplification status [10], there are two merits for enhancing the comparator speed and reducing delay change with the input common-mode voltage variation. First, the operation current is not decreased by the reduced drain-source voltage of M5. Thus, there is no speed penalty even if the input common-mode voltage is lower. Second, the 1st stage outputs will not collapse to zero together while the clock is triggering on. Consequently, M1 and M2 can sustain in saturation region, providing a fast and robust amplification of comparator input voltage. In addition, we insert an always-on transistor M11 in the 2nd stage between node A and B, and therefore add a transistor delay τ_{M11} in the clock path of M12. This delay postpones slightly the regeneration but reserves more time for the amplification. Thus, the differential signal ΔV_{XY} between V_X and V_Y can reach the logic threshold in the regeneration nodes while the clock is toggled, reducing the metastability. Besides, the clock transition coupling of M12 from V_{CK} is isolated by M11, thus avoiding the glitch coupled to the regeneration nodes directly. In the above configuration, only dynamic power is dissipated.

Fig. 5 shows the simulated comparator delays of [7], [8], and this work versus the differential input at V_{CM} = 0.45V, 0.6V, and 0.75V, respectively. The comparators are operated at 3.3GHz clock frequency under 1.2V supply voltage, and their transistor dimensions are scaled to let them have the same power consumption. From the plots, the delay of [7] is sensitive to the common-mode voltage variations. And the speed of [8] dropped obviously when the input is small. Actually, while the clock turns on, the input-stage outputs drop to zero in succession with different times, depended to the input voltage difference [8]. When the input is small, the input-

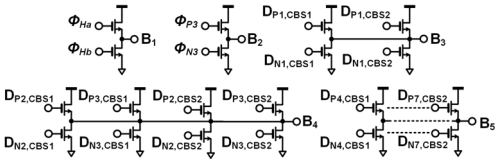


Fig. 6. Proposed 1-of-N-to-Binary encoders.

stage transistors both change from saturation to triode region quickly. The decreased gain also reduces the difference of drop-to-zero voltages, and thus increasing the latch regeneration time and comparator delay. In the proposed scheme, the comparator delays are 16.8ps, 15.3ps and 14ps for a 4mV differential input with different common-mode voltages, respectively. When compared to [7] and [8], the proposed comparator attains shorten delay, less metastability, and is not sensitive to common-mode voltage variations.

B. 1-of-N-to-Binary Encoders

As mentioned before, the comparator gives rise to V_{OP} = 1 and V_{ON}=0 if the input voltages are $V_{comp+} > V_{comp-}$, otherwise the opposite. If the comparator is not triggered, $V_{OP} = V_{ON} = 0$. Due to the characteristics of the BS conversion, there is only 1 comparator activated at each bit quantization. Subsequently, the comparator outputs appear as 1-of-N code format in each bit stage. For example, if Φ_{P3} = 1, the 1st comparator in CBS1 is triggered, and the comparison result is $D_{P1,CBS1}$ = 1 and $D_{N1,CBS1}$ = 0. On the other hand, Φ_{N3} = 0 (since only one of Φ_{P3} and Φ_{N3} can be turned into 1 during BS conversion). Thus, the 1st comparator of CBS2 is not triggered, whose output states are kept as $D_{P1,CBS2}$ = 0 and $D_{N1,CBS2}$ = 0. Consequently, the output code is 1000 in the 3rd bit quantization. Fig. 6 shows the schematics of 1-of-N-to-Binary encoders. In the B_3 encoder, $D_{P1,CBS1}$ ($D_{N1,CBS1}$) and $D_{P1,CBS2}$ ($D_{N1,CBS2}$) each control one NMOS switch connected to V_{DD} (V_{GND}). B_3 becomes logic '1' since only the switch controlled by $D_{P1,CBS1}$ is turned on. Actually, all comparators outputs are connected to the switches with V_{DD} or V_{GND}, depending on their polarity.

Since all asynchronous clock phases are generated by comparator outputs in the BS scheme, the balancing of comparator differential outputs loading is important. In this encoder, the comparator outputs are both connected to a NMOS switch with the same dimension, leading to an output loading well balanced. Although an NMOS switch is not adequate to pass the supply voltage, it is sufficient to process a digital signal. A strong logic '1' can be produced after two small inverters are located at the encoder output. We employ low-threshold NMOS transistors in the encoders to relieve the voltage drop of the logic '1'. Besides, we utilize minimum size transistors to reduce the loading effect to the comparator. Plus, there are only 5 switches turning on for 5-bit code transformation, leading to low-power operation.

IV. Measurement Results

Fig. 7 shows the die photograph of the prototype ADC, fabricated in a standard 1P7M 65nm CMOS, with an active area of 0.0084mm^2 (70μm×120μm). Fig. 8 shows the measured DNL/INL, the DNL is +0.78/-0.71 LSB and the INL is +0.95/-0.59 LSB. Fig. 9 shows the FFT spectrum measured at 2 GS/s with 1.02 GHz input. The measured SNDR and SFDR are 28 dB and 36.8 dB, respectively. Fig. 10 (a) and (b) illustrates the SNDR versus sampling frequency and input frequency,

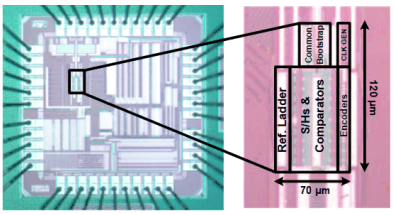


Fig. 7. Chip micrograph

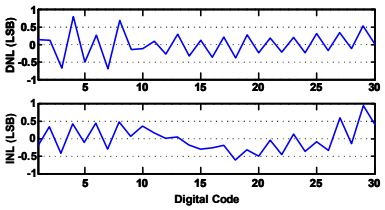


Fig. 8. Measured DNL and INL.

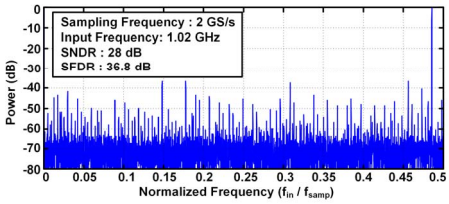
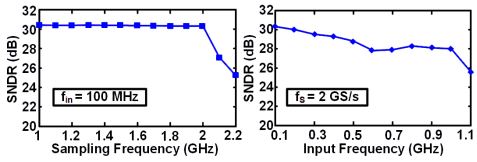


Fig. 9. FFT spectrum (Output decimated by 25).



(a) (b)

Fig. 10. Measured SNDR versus (a) Sampling frequency, (b) Input frequency.

respectively. The drop of the SNDR from f_{in}=0.1–1 GHz is 2.3 dB, resulting in an effective resolution bandwidth (ERBW) over the Nyquist frequency. The effective number of bits (ENOB) is 4.72 bit at 100MHz and 4.36 bit at the Nyquist input. The prototype ADC consumes 3.9mW of power operating at 2 GS/s. The analog power including S/Hs, comparators and reference ladder consumes 78% of the total power, while the digital power is only 22%. This means that most of the power is dissipated in the conversion, and not in the control signal processing. Table I summarizes the performance comparison of this work with previous designs of BS ADCs as well as with the state-of-the-art single-channel ADCs at a speed of 1 to 3.5 GS/s in 5 to 6-bit resolution. The implemented 5-bit 2 GS/s BS ADC achieves a Walden FoM of 74 and 95 fJ/conversion-step for 100 MHz and Nyquist input frequency, respectively, with a very compact design of 0.0084mm^2 only.

V. Conclusions

This paper reported a 5-bit 2GS/s binary-search ADC. The proposed architecture exploits the advantage of the most primitive BS scheme, but reduces the comparator count. In the design, the bit latency is just only a single comparator delay. The proposed charge-steering comparator quantizes each bit rapidly further enhancing the ADC speed. Besides, the proposed 1-of-N-to-Binary encoders can well balance the asynchronous clock phase paths of the BS ADC. Obviously, by shortening the comparator delay of each bit quantization, the BS becomes a good candidate for high-speed and low-power ADC conversion due to its inherent advantages.

TABLE I

Performance Summary & Benchmark with State-of-the-Art

	JSSC'14 [13]	ASSCC'15 [14]	ISSCC'16 [15]	JSCC'08 [1]	ISSCC'09 [2]	ASSCC'11 [3]	ESSCIRC'15 [4]	This Work
Architecture	Subranging	Flash	SAR	BS	BS	BS	Pipelined BS	BS
Process (nm)	65	65	40	90	65	65	40	65
Resolution (bit)	6	6	6	6	5	5	6	5
Speed (GS/s)	1	3.4	1	0.25 *	0.8	0.5	1.6	2
Supply (V)	1.1	1	1	1	1	1.2	0.9	1.2
Power (mW)	9.9	12.6	1.26	0.14	1.97	1.63	3.17	3.9
SNDR (dB) @ DC	33	34.7	35.1	33.7	28.2	29.5	30.5	30.3
SNDR (dB) @ Nyquist	32.8	34.2	34.6	32.1	26.9	27.8	29.2	28
FOM	278	89	28.7	15	116	117	84.1	95
Active Area (mm^2)	0.044	0.034	0.00058	0.05	0.018	0.015	0.017	0.0084
Offset Reduction	On-Chip Calibration	On-Chip Calibration	By Tolerance	Off-Chip Calibration	By Tolerance	On-Chip Calibration	On-Chip Calibration	On-Chip Calibration

* 6-bit Sub-ADC in BS Operation, Speed is 0.25 GS/s

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