20.7 A 72.6dB-SNDR 100MHz-BW 16.36mW CTDSM with Preliminary Sampling and Quantization Scheme in Backend Subranging QTZ

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Driven by great demands for high data transfer rates in mobile communications, ADCs require wide bandwidths with low noise density and power consumption. The continuous-time ΔΣ modulator (CTDSM) is a suitable candidate for such applications as it has a simple slew rate requirement and inherently contains an anti-aliasing function. To satisfy the wide bandwidth (~100MHz for LTE-A) and simultaneously maintain the energy efficiency of the CTDSM, a multi-bit quantizer (QTZ) is often utilized that relaxes the OSR, jitter and loop filter stability. On the other hand, new design issues, such as DAC nonlinearity and high power consumption in the data feedback and QTZ, rise with large numbers of bits in the QTZ. While the DAC mismatch can be suppressed by calibrations [1,2] and the number of feedback DACs can be reduced to just one with feedforward [3] or QTZ-based excess loop delay (ELD) compensation [4], the QTZ design becomes the bottleneck in both the speed and resolution of the modulator. Here, we introduce a preliminary sampling and quantization (PSQ) technique that allows almost full utilization of a clock period for the quantization, thus leading to an extra 30% conversion time or an additional 12dB SQNR contribution when compared with the conventional approach. The modulator runs at 2GHz and attains 72.6dB SNDR and 76.3dB DR over a 100MHz bandwidth, while only consuming 16.36mW.

Conventionally, the ELD compensation limits the available conversion time (T_{av}) of the QTZ because it needs to cover the delays caused by the QTZ latency, DAC feedback and loop filter (LF) settling. Therefore, the available conversion time is highly confined under such circumstances, thus limiting the architectural choice of the QTZ. In this work, rather than squeezing all of the conversion within T_{av}, we manage to reuse the ELD period for quantization. Such an arrangement enables a 2-step operation in the backend QTZ that greatly relieves the timing and architectural constraints in conventional CTDSMs. Figure 20.7.1 illustrates the signal characteristics and timing diagram of the proposed CTDSM. We separate both the sampling and quantization into coarse and fine segments, where the coarse sampling is leading the fine sampling for a period (Δt_{CF}, details of its choice explained next). After the coarse QTZ determines the first two MSB decisions, they are employed by the fine QTZ and convert together with the fine sample. Then, the fine QTZ resolves the rest of the LSBs and finally feeds back both MSB and LSB decisions to the input through the DAC with ELD. ϕ_F and ϕ_C are the sampling instants of the fine and coarse QTZ, respectively, where the stability of the modulator (under a limited ELD compensation ability) determines ϕ_F. In conventional CTDSMs, the time before ϕ_F is squandered as the LF output is considered not yet ready. Here we utilize such an interval with a PSQ. Nevertheless, as the coarse and fine QTZs sample the output of the LF at different instants, they induce a sampling error ε_{SAM} related to Δt_{CF}, which trades off the available conversion time of the coarse QTZ.

Aside from Δt_{CF}, ε_{SAM} is also affected by the out-of-band gain, the order and response of the LF, and the input and the resolution of the QTZ. Figure 20.7.1 (top) shows the signal behavior of the LF output with an ideal and finite frequency response, respectively, with a 100MHz sinusoid input. Its response consists of two parts: bandwidth limited and input tracking. After the DAC feedback, the LF equivalently responds to a step input. While limited by the finite bandwidth of the opamps in the LF, the output deviates from its ideal value but eventually converges when the response becomes moderate during input tracking. Such a characteristic modulates ε_{SAM} diversely at different LF output conditions. At close to the zero crossing, ε_{SAM} decreases when comparing it with the ideal response, as the DAC feedback and the settling directions of the LF output are opposite. On the other hand, when the LF output is close to the peak value, ε_{SAM} rises because of the accumulated settling error. Consequently, with a limited opamp bandwidth of 7GHz, the emergence of the largest ε_{SAM} evolves from the ideal zero crossing case to its peak, while such error can still be corrected together with the first-stage residual offset by 1b overlapping between the coarse and fine QTZ. With 130ps Δt_{CF} in this design, the maximum ε_{SAM} is around 100mV, which is well covered by the 175mV redundancy range in the second stage.

Figure 20.7.2 exhibits the simplified schematic of the QTZ in a single-ended configuration while in the proposed design we utilize a differential structure. The coarse QTZ is a two-step architecture with the MSB resolved directly with the comparator C1 at ϕ_{ST1} after the coarse sampling ϕ_C. The decision from C1 then controls the bottom-plate switch of DAC2-4, which generates the reference voltages for C2-4 with different capacitance sizing ratios. C2-4 triggered together at ϕ_{ST2} resolve 2 more bits and the results from C1-4 are then fed to the segmented DAC of the fine SAR ADC directly without decoding. Finally, the fine SAR ADC resolves the remaining 4 bits after the fine sampling ϕ_F. In this design, the conversion of the coarse QTZ takes about 0.25 Ts (125ps), which benefits from the direct control and the small DACs (3fF). The offset of the comparators (C1-4) in the first stage is calibrated in foreground to a 4b level off-chip where the residual error is corrected by the redundancy. The whole conversion is running in an asynchronous manner where it waits until the validation of all the decisions from C2-4 to trigger the first comparison in the fine SAR ADC. The conversion time of the fine QTZ is close to 0.65 Ts (325ps), as we adopt a small DAC (9.6fF) and dynamic logic. As a result, the 7b subranging ADC can run at 2GHz while only consuming ~1.4mW of power.

Figure 20.7.3 presents the 4th-order CTDSM employing the PSQ scheme. It contains two simple RC integrators, one single amplifier biquad integrator, a 7b QTZ (with 1b redundancy) and a segmented NRZ DAC. We use a two-stage topology with feed-forward path and a Miller compensation amplifier [3] in the integrator, with the capacitors of the LF digitally programmable to cover the process variation on the transfer function. Similar to [1,3,4], we utilize the feedforward architecture to reduce the power from the opamps and realize the ELD compensation with 0.65 Ts ELD, such that only one main feedback DAC is necessary. Further, we design a 3-4b segmented NRZ DAC, which not only matches with the outputs of the QTZ but also helps to reduce the power of the DAC drivers while its mismatch is calibrated in the digital backend [1]. The supply voltage of the current steering DAC is 1.5V, which provides sufficient linearity and noise performance. Only one clock is necessary in this ADC while the others are generated asynchronously from the operation.

The CTDSM prototype fabricated in 28nm CMOS attains a 100MHz bandwidth with 2GHz sampling frequency. Figure 20.7.4 plots the spectrum of the modulator with -2dBFs input at 18MHz and an input common mode of 0.5V. The measured peak SNDR, SNR and SFDR are 72.6dB, 73.2dB and 83.6dB, respectively. The measured IMD3 is -72.4dB with two -15dBFS inputs at 83MHz and 87MHz. Figure 20.7.5 shows the SNR and SNDR versus the input amplitude and power breakdown. The measured dynamic range (DR) is 76.3dB. The modulator consumes 16.3mW from a 1.1V/1.5V supply, with 2mW drawn by the digital part, and 14.3mW by the analog part, where the QTZ only consumes ~1.4mW. Figure 20.7.6 summarizes the measured performance of this work and compares it with state-of-the-art CTDSMs having similar bandwidths. The proposed modulator achieves a Walden FOM_W of 23.4fJ/conv-step and a Schreier FOM_S of 170.5dB, revealing a CTDSM with excellent energy efficiency and a bandwidth ≥ 45MHz. The outstanding energy efficiency is derived mainly from the PSQ with 1-feedback DAC and simple clocking. Figure 20.7.7 exhibits the chip microphotograph with an active area of 0.019mm^2.

Acknowledgements:
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References:
[1] B. Wu, et al., "A 24.7mW 45MHz-BW 75.3dB-SNDR SAR-assisted CT ΔΣ modulator with 2nd-order noise coupling in 65nm CMOS," *ISSCC*, pp. 270-271, Feb. 2016.
[2] Y. Dong, et al., "A 930mW 69dB-DR 465MHz-BW CT 1-2 MASH ADC in 28nm CMOS," *ISSCC*, pp. 278-279, Feb. 2016.
[3] C. Ho, et al., "A 4.5mW CT self-coupled ΔΣ modulator with 2.2MHz BW and 90.4dB SNDR using residual ELD compensation," *IEEE JSSC*, vol. 50, no. 12, pp. 2870-2879, Dec. 2015.
[4] S. Huang, et al., "A 125MHz-BW 71.9dB-SNDR VCO-based CT ΔΣ ADC with segmented phase-domain ELD compensation in 16nm CMOS," *ISSCC*, pp. 470-471, Feb. 2017.

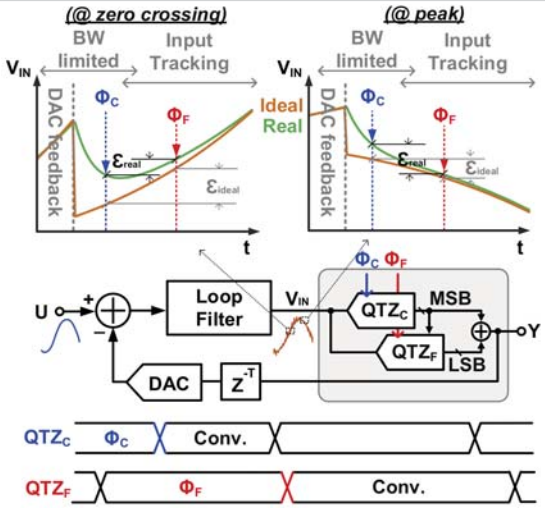


Figure 20.7.1: The conceptual block diagram and timing of the proposed CTDSM with preliminary sampling and quantization, including sampling error illustration (top).

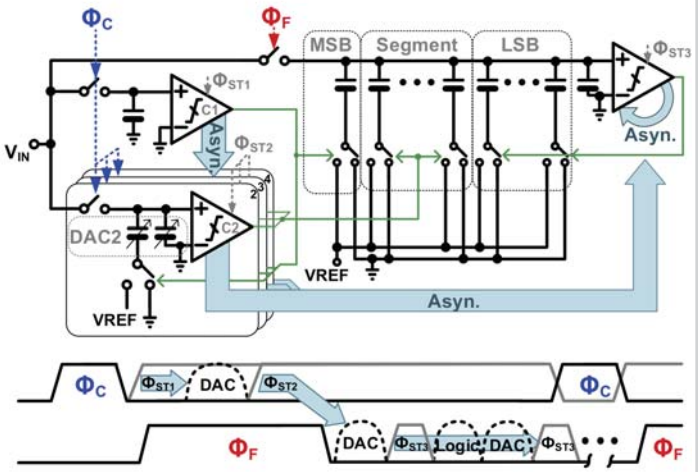


Figure 20.7.2: The simplified circuit schematic of the QTZ with asynchronous clocking path highlighted.

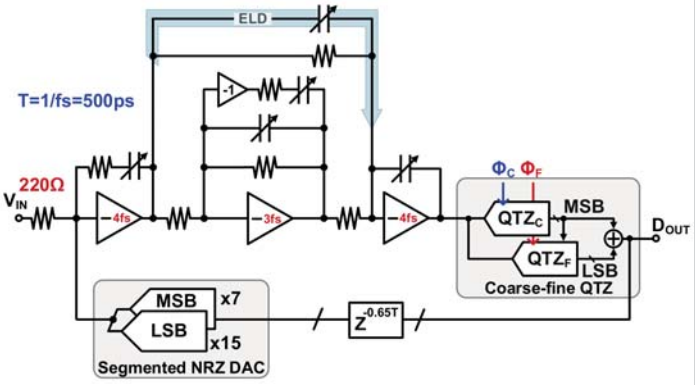


Figure 20.7.3: The block diagram of the modulator with the ELD path highlighted.

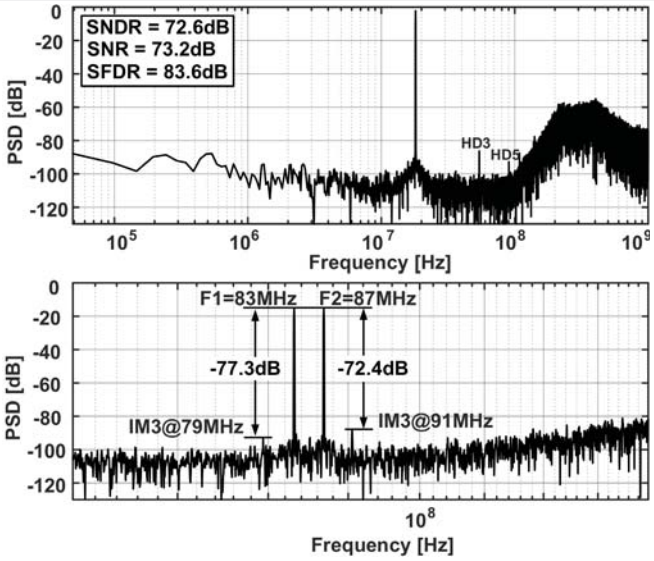


Figure 20.7.4: Measured 41k-point single-tone and two-tone output spectra.

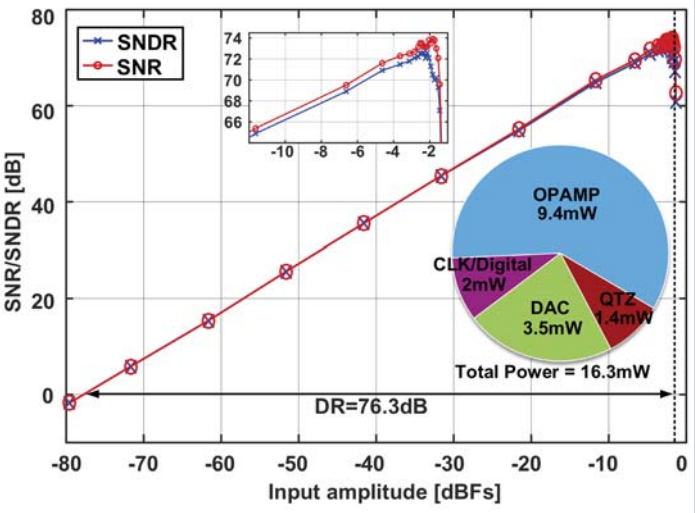
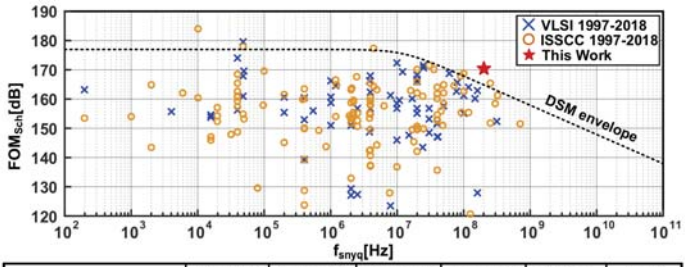


Figure 20.7.5: SNR/SNDR versus input amplitude (Fin = 18MHz) and power breakdown.



	ISSCC17 [4]	ISSCC16 [1]	ISSCC16 Wu	ISSCC11 Bolatkale	VLSI14 Ho	This work
Area (mm^2)	0.217	0.16	0.155	0.9	0.1	0.019
Technology (nm)	16	65	16	45	20	28
OSR	8.6	10	9	16	13.7	10
Fs (GHz)	2.15	0.9	2.88	4	2.184	2
Bandwidth (MHz)	125	45	160	125	80	100
Power (mW)	54	24.7	40	256	23	16.3
Peak SNDR (dB)	71.9	75.3	65.33	65	67.5	72.6
DR (dB)	74.8	82.5	72.1	70	73	76.3
FOMSch/SNDR (dB)	165.7	167.9	161.4	151.9	162.9	170.5
FOMSch/DR (dB)	168.4	175.1	168.1	156.9	168.4	174.2
FoMWa (fJ/conv.step)	67.2	57.7	82.8	704.7	74.2	23.4

Figure 20.7.6: Comparison with state-of-the-art ADCs and summary of measurement results.

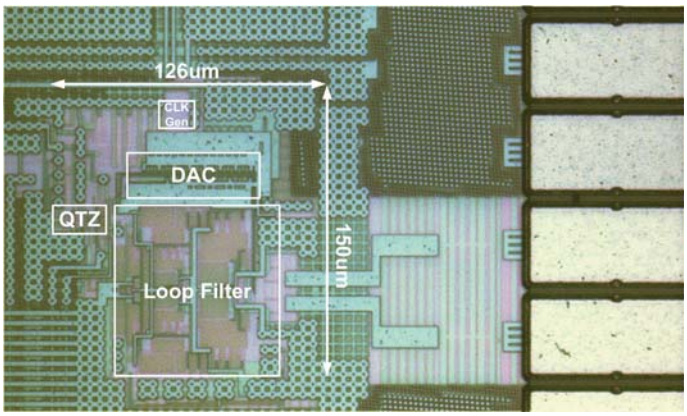


Figure 20.7.7: The chip micrograph.

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