Using EDA Tools to Push the Performance Boundaries of an Ultralow-Power IoT-VCO at 65nm

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***Abstract*—Voltage-controlled oscillators (VCOs) embedded in state-of-the-art radio-frequency (RF) integrated circuit (IC) multi-standard transceivers must comply with extreme ultralow power requirements for modern IoT applications. However, due to the countless tradeoffs that must be considered, their manual design hardly approaches the full potential that a certain topology can achieve at advanced integration nodes. In this paper, the design and optimization of a complex IoT-VCO for a 65 nm process design kit (PDK) is fully supported by electronic design automation (EDA) tools. Firstly, a 108-dimensional performance space is optimized, providing 48 sizing solutions where the power consumption varies from 0.145 mW to 0.329 mW on the worst-case corner performance of the worst-case tuning range. Afterwards, the layout-versus-schematic (LVS) correct layout of each solution is automatically generated using a hierarchical Placer and group-based Router. Post-layout validation is carried in all solutions, and, a promising solution with 0.348 mW of worst-case post-layout power consumption is proposed for fabrication.**

I. Introduction

VCOs are essential in modern RF ICs multi-standard transceivers, and, are subject to continuous research efforts that push the boundaries of their multifaceted performance/power efficiency in state-of-the-art applications and integration technologies [1, 2]. However, the proper analysis of the design tradeoffs is impractical, as a large amount of conflicting performance figures obtained from multiple modes, test benches and/or analysis are weighted simultaneously. Their performance inflation in the presence of process variations turns the problem to proportions beyond human capabilities, which can only be solved with the support of optimization-based tools [3–5]. Moreover, due to the severe impact of layout parasitics at gigahertz frequencies, layout-aware sizing methodologies were proposed to shorten the gap between electrical and physical design steps, by generating the complete layout during the optimization flow [6–8]. Nonetheless, as the complexity of state-of-the-art RF circuits increases, the enormous simulation and layout generation times hamper the generalized application of these EDA tools, and, are still pushing the computational capabilities of modern workstations to its limits.

In this paper, the role of EDA frameworks in the design and optimization of complex RF topologies is shown, by adapting an established tool and applying it to a VCO topology for state-of-the-art IoT specifications at a 65 nm PDK. Firstly, the sizes of its devices are optimized in a performance space obtained from 14 time-consuming steady-state (SST)/SST noise analysis. Afterwards, the complete layout of each solution is generated using instances of the parametric cells provided by the foundry, and, routed using a group-based scheme. The obtained layouts are verified and extracted in most established off-the-shelf CAD tools, and, the obtained insights on the post-layout performance space are used to re-iterate and devise a solution for fabrication. The remainder document is organized as follows. In section II, the sizing optimization of the IoT-VCO is presented. Afterwards, section III addresses the automatic layout, and, section IV, the conclusions and future research directions.

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II. Sizing Optimization Setup & Results

Fig. 1 introduces the schematic of the IoT-VCO [9] where the proposed method was applied. A supply voltage of 800 mV and an I_B of 10 µA was used for a 65 nm CMOS PDK.

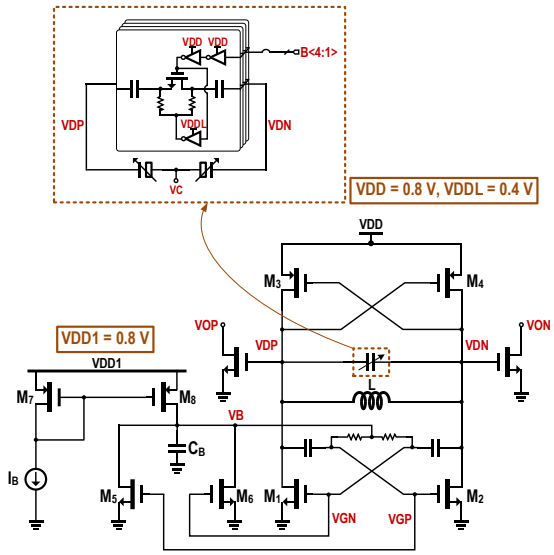

Fig. 1. IoT-VCO with a 4-bit binary-sized switched-capacitor array for increased tunning range.

This IoT-VCO topology aims to achieve an ultralow power while still keep good phase noise performance. To reduce the power consumption, the NMOS-PMOS complementary cross-coupled pair (M_1 and M_2, M_3 and M_4) are used in the class-C mode. To guarantee the robust start-up under different process corners, a dynamic biasing scheme is used to generate VB by M_5 and M_6 [10, 11]. A 4-bit binary-sized switched-capacitor array (SCA) together with A-MOS varactors are employed to tune the

VCO frequency from 4.5 to 5.4 GHz continuously [4]. The SCA biasing voltage V_{DDH} and V_{DDL} are 800 mV and 400 mV. The inductor topology adopted is an octagonal spiral inductor in ultra-thick metal and the inductor model provided by the foundry supports the change of different dimension parameters.

A. Design Variables

The netlist of the IoT-VCO was parameterized, and, Table I details the limits and ranges of each of the 22 variables used for optimization. Note that the sizes of the *n*-type transistors and the poly resistors from the 4-bit SCA, the digital control of SCA, moscap varactor, and, output buffers, were imposed by the circuit designer and kept fixed during optimization.

TABLE I. OPTIMIZATION VARIABLES & DESCRIPTION

Variable	Units	Min.	Grid	Max.
radius[1]	µm	15	5	90
turns[1]	-	1	1	6
spacing[1]	µm	2	1	4
width[1]	µm	3	1	30
nccl[2,7], **pccl**[3]	nm	60	20	240
nccnf[2], **pccnf**[3], **m56nf**[7], **m78nf**[8]	-	1	1	32
nccw[2], **pccw**[3], **m56w**[7]	µm	0.6	0.2	6
m78l[8]	nm	130	20	6000
m78w[8]	nm	120	20	6000
rccl[5]	µm	0.8	0.2	30
ccpnv[4], **ccpnh**[4], **vbnv**[6], **vbnh**[6], **scanv**[9]	-	6	2	100
scanh[9]	-	6	2	50

[1]**radius**, **turns**, **spacing** and **width** are the inner radius, number of turns, spacing between conductors and conductor width of the inductor L; [2]**nccl**, **nccw** and **nccnf** are the length, width per finger and number of fingers of the cross-coupled M_1/M_2 RF transistors; [3]**pccl**, **pccw** and **pccnf** are the length, width per finger and number of fingers of the cross-coupled M_3/M_4 RF transistors; [4]**ccpnv** and **ccpnh** are the number of vertical and horizontal fingers for a width/spacing of 100 nm of the MOM capacitors from the VCO core; [5]**rccl** is the segment length for a segment width of 0.5 µm of the poly resistors from the VCO core; [6]**vbnv** and **vbnh** are the number of vertical and horizontal fingers for a width/spacing of 100 nm of the C_B MOM capacitor; [7]**nccl**, **m56w** and **m56nf** are the length, width per finger and number of fingers of the M_5/M_6 RF transistors; [8]**m78l**, **m78w** and **m78nf** are the length, width per finger and number of fingers of the M_7/M_8 transistor (the width of M_7 is **m78w**/2); [9]**scanv** and **scanh** are the number of vertical and horizontal fingers for a width/spacing of 100 nm of the MOM capacitors from the SCA, using device multiplier ratio of 8:4:2:1.

B. Test benches and Measurements

For each different tuning frequency of the SCA control, B<4:1>, a SST analysis is configured to extract the oscillation frequencies at standard supply voltage, f_{osc}, phase noises, *PN,* power consumption, and, compute the figure-of-merit, FOM:

$$FOM = -10\,log\left[\frac{P_{dc}}{1mW}\cdot\left(\frac{\Delta\omega}{\omega_0}\right)^2\right] - PN(\Delta\omega) \quad [dBc/Hz] \qquad (1)$$

where ω_0 is the oscillation frequency, P_{dc} the power consumption, $\Delta\omega$ is the offset from the output frequency and $PN(\Delta\omega)$ is the oscillator phase noise. Additionally, two SST analysis are performed to extract the f_{osc} for a supply voltage of 750 mV and 850 mV, used to compute the frequency sensitivity due to a supply voltage variation, *fssv*, of 50 mV:

$$fssv = \left|\frac{f_{osc}@Vdd_2 - f_{osc}@800mV}{Vdd_2 - 800mV}\right| \quad [Hz/V] \qquad (2)$$

where $f_{osc}@Vdd_2$ is the oscillation frequency at the different supply voltage Vdd_2. These three test benches are designated in Table II by $SST@800_{bxxxx}$, $SST@750_{bxxxx}$ and $SST@850_{bxxxx}$, respectively. The following process corners were considered: slow N/slow P (SS), slow N/fast P (SF), fast N/slow P (FS), and, fast N/fast P (FF). Therefore, 8 additional testbenches were added to the previous typical (TT) setup. This resulted in a 108-dimensional performance space spread through two different modes (b_{0000} and b_{1111}), resultant from 14 different testbenches simulated with the same 22-dimensional design variable space *x*. Note that only b_{1111} and b_{0000} tunings are verified since the continuous tuning between 4.5 GHz and 5.4 GHz is guaranteed by a device multiplier ratio of 8:4:2:1 on the 4-bit SCA.

TABLE II. 64 MEASURES OBTAINED FROM 14 DIFFERENT TESTBENCHES, AND, 44 EXPRESSIONS AS FUNCTIONS OF THE SIMULATIONS' OUTPUT. {CORNER} MEASURES ARE OBTAINED FOR TT, SS, SF, FS AND FF.

Measure	Units	Measured from
$f_{osc}[b_{0000}]$@800mV{corner}	GHz	$SST@800_{b0000}${corner}
$f_{osc}[b_{1111}]$@800mV{corner}	GHz	$SST@800_{b1111}${corner}
$f_{osc}[b_{0000}]$@750mV{TT}	GHz	$SST@750_{b0000}${TT}
$f_{osc}[b_{1111}]$@750mV{TT}	GHz	$SST@750_{b1111}${TT}
$f_{osc}[b_{0000}]$@850mV{TT}	GHz	$SST@850_{b0000}${TT}
$f_{osc}[b_{1111}]$@850mV{TT}	GHz	$SST@850_{b1111}${TT}
PN[b_{0000}]@10kHz/100kHz/1MHz/10MHz{corner}	dBc/Hz	$SST@800_{b0000}${corner}
PN[b_{1111}]@10kHz/100kHz/1MHz/10MHz{corner}	dBc/Hz	$SST@800_{b1111}${corner}
power[b_{0000}]{corner}	mW	$SST@800_{b0000}${corner}
power[b_{1111}]{corner}	mW	$SST@800_{b1111}${corner}
Expressions	**Units**	**Computed from**
fssv[b_{0000}]@750mV/850mV{TT}	MHz/V	Equation (2)
fssv[b_{1111}]@750mV/850mV{TT}	MHz/V	Equation (2)
FOM[b_{0000}]@10kHz/100kHz/1MHz/10MHz{corner}	dBc/Hz	Equation (1)
FOM[b_{1111}]@10kHz/100kHz/1MHz/10MHz{corner}	dBc/Hz	Equation (1)

C. Optimization Objectives and Constraints

According to Table III, three optimization objectives were set to improve the worst-case corner performance from the worst-case mode, and, therefore, obtain the global optimum solutions. This is, minimize the largest power measured, minimize the worst value of phase noise at 10 MHz measured, and, minimize the highest *fssv* value measured. With this configuration the FOM is inherently optimized. Moreover, the third column of Table IV details the optimization constraints, which are set on the f_{osc} to meet the desired 200 MHz range, at phase noises, and, FOMs. These optimization constraints were set for all corners. Additionally, only solutions with *fssv*s below 100 MHz/V were accepted.

TABLE III. OPTIMIZATION OBJECTIVES

Target	Metric	Units
Min	Max(power[b_{0000}]{TT}, power[b_{1111}]{TT}, power[b_{0000}]{SS}, power[b_{1111}]{SS}, power[b_{0000}]{SF}, power[b_{1111}]{SF}, power[b_{0000}]{FS}, power[b_{1111}]{FS}, power[b_{0000}]{FF}, power[b_{1111}]{FF})	mW
Min	Max(PN[b_{0000}]@10MHz{TT}, PN[b_{1111}]@10MHz{TT}, PN[b_{0000}]@10MHz{SS}, PN[b_{1111}]@10MHz{SS}, PN[b_{0000}]@10MHz{SF}, PN[b_{1111}]@10MHz{SF}, PN[b_{0000}]@10MHz{FS}, PN[b_{1111}]@10MHz{FS}, PN[b_{0000}]@10MHz{FF}, PN[b_{1111}]@10MHz{FF})	dBc/Hz
Min	Max(fssv[b_{0000}]@750mV, fssv[b_{0000}]@850mV, fssv[b_{1111}]@750mV, fssv[b_{1111}]@850mV)	MHz/V

D. Sizing Optimization: Results and Analysis

The circuit simulator adopted was the Mentor Graphics' Eldo RF. The optimization was carried with a population of 256 elements through 100 generations using the sizing optimization framework from [4]. Due to the time required to completely evaluate a candidate solution by 14 expensive SST analysis, even in a modern Intel-Xeon-CPU E5-2630-v3@2.40GHz workstation with 64GB of RAM, using 8 cores for parallel simulation, the optimization took approximately 367 hours. The maximum time allowed for each SST execution was 10 minutes. The worst-case corner of worst-case mode optimization provided 48 sizing solutions, drawn in Fig. 2.

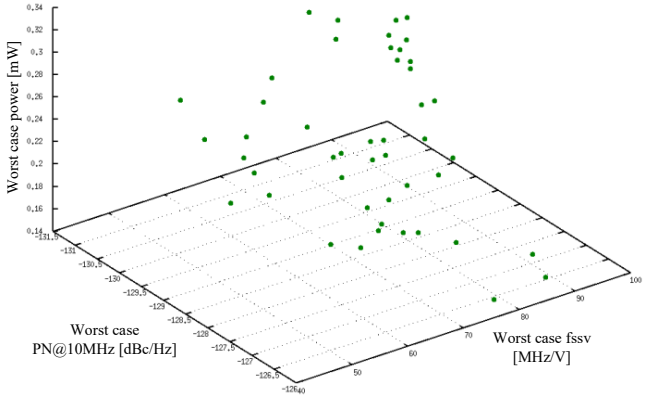

Fig. 2. Pareto front with the tradeoff of Table III with 48 sizing solutions. The solutions spread from 0.145 mW to 0.329 mW power, -126.31 dBc/Hz to -131.11 dBc/Hz PN@10MHz, and, 40 MHz/V to 100 MHz/V *fssv*. The performances shown are the worst possible for each corner/mode of the design.

III. Automatic Layout Generation & Results

This section details the automatic layout generation.

A. Hierarchichal Template-based Placer

In this PDK, compact models used for simulation of RF devices contain complete layout parasitic information. Thus, the extraction of RF devices must be performed at gate-level, and, the layout instances used within automatic procedures should be identical to the ones provided by the foundry. In this revised version of the template-based approach for analog and RF IC blocks proposed in [8], to bypass the expensive development of custom generators for RF cells, the layout of all devices is imported as GDSII files. The designer is responsible for providing the high-level floorplan guidelines such as the ones presented in Fig. 3, capitalizing his expertise and layout preferences, e.g., aligned signal-flows, minimal wiring topology, guard-rings, dummies, etc. The hierarchical floorplan is built automatically, as the sub-partitions are generated first and combined at top partitions, given any set of device sizes.

B. Group-based Routing

While the placement is controlled by the circuit designer using the specification-independent template, all routing tasks are performed automatically. Preliminarily, each terminal of each GSDII cell instantiated is parsed by the tool and made available for the routing procedure. Afterwards, three steps are performed sequentially: (1) the terminal-to-terminal connections are determined from the circuit netlist; (2) a global routing solution that incorporates symmetry information is devised; (3) and finally, a detailed optimization process is used to solve all design-rule and LVS errors [8]. Due to the high number of shapes laid out in the previous placement step and nets requiring to be routed, the detailed routing is particularly time-consuming, as built-in algorithms check the design-rules and short-circuits in every shape of the layout every time the optimization kernel performs a layer or structural change. To speed up this process, the 3-step routing procedure was separated into five independent processes exploiting the hierarchy of the placement template. This is, firstly, the sub-partitions *SCA N* and *SCA P* are internally routed, after, the *SCA Top* and *VCO Core & VB-Gen*, and finally, the routing of the top-partition, that interconnects the routed *SCA Top*, the routed *VCO Core & VB-Gen*, output buffers and decoupling capacitors.

C. Post-layout Performance

The automatic layout generation of each of the 48 solutions of Fig. 2 took over 2 hours. The layouts were saved as GDSII files, validated in Mentor Graphics' Calibre nmLVS®, extracted in Calibre xRC®, and, the post-layout performances simulated. The simulation times of the extracted netlists increase exponentially with respect to the pre-layout. In every design, at least one of the 14 testbenches failed convergence post-layout, making it impossible to evaluate its overall performance. In some cases, the extracted layout parasitics make the design stop oscillation as the simulator is unable to converge to the guessed oscillation frequency, whereas in others the simulation attempts to converge infinitely. The post-layout performances of one solution, corresponding to the pre-layout solution with worst case values of 0.267 mW power, -130.66 dBc/Hz PN@10MHz and 76 MHz/V *fssv*, are outlined in columns 4 to 8 of Table IV. The converging testbenches of this and each other 47 designs allowed to take valuable insights on the post-layout performance space, as the deviation from the desired oscillation frequency and drop on PNs[b_{1111}] are the most recurrent problems.

D. Design Tuning

Since the computational times required by the automatic layout generation procedure and simulation of extracted netlist of 14 testbenches are still prohibitive for full layout-aware optimization, the highlighted solution was re-iterated by tuning the inductor and bias current. For that purpose, EDA tools were resorted again. The extracted netlist of the design was kept, and, an optimization that changes only the inductor dimensions (*radius*, *turns*, *spacing* and *width*) and I_B current was carried with a population of 16 elements. The objectives and constraints of Section II. D were kept, and, the optimization was stopped when feasibility (i.e., all constraints satisfied) was achieved. In the last columns of Table IV, the post-layout performances of the re-iterated design are outlined. The proposed solution achieved extremely low post-layout power consumption, 0.348 mW worst case, and, frequency pushing figures, 84 MHz/V worst case. The latest being extremely relevant as it is a critical issue in the design of VCOs for real-life product. The prototype was sent for fabrication as its post-layout performance compete in the forefront with most-recently published VCOs (Table I of [1]).

TABLE IV. MEASURES, OPTIMIZATION CONSTRAINTS AND POST-LAYOUT PERFORMANCES

Measure	Units	Target	Post-layout					After Post-Layout Tuning				
			I_B 10µA, *radius* 75µA, *turns* 3, *spacing* 2µA, *width* 15µA					I_B **13µA**, *radius* **70µA**, *turns* 3, *spacing* 2µA, *width* **14µA**				
			TT	SS	FS	SF	FF	TT	SS	FS	SF	FF
$f_{osc}[b_{0000}]$@800mV	GHz	≥ 5.3 ≤ 5.5	**5.078**[f]	**5.089**[f]	**5.089**[f]	**5.067**[f]	**5.067**[f]	5.316	5.305	5.327	5.305	5.328
$f_{osc}[b_{1111}]$@800mV	GHz	≥ 4.4 ≤ 4.6	**4.390**[f]	**n/c**	**4.393**[f]	**4.387**[f]	**4.387**[f]	4.588	4.578	4.592	4.584	4.598
fssv[b_{0000}]@750mV	MHz/V	≤ 100	88	n/d	n/d	n/d	n/d	80	n/d	n/d	n/d	n/d
fssv[b_{0000}]@850mV	MHz/V	≤ 100	76	n/d	n/d	n/d	n/d	72	n/d	n/d	n/d	n/d
fssv[b_{1111}]@750mV	MHz/V	≤ 100	78	n/d	n/d	n/d	n/d	**84**[w]	n/d	n/d	n/d	n/d
fssv[b_{1111}]@850mV	MHz/V	≤ 100	62	n/d	n/d	n/d	n/d	**72**	n/d	n/d	n/d	n/d
PN[b_{0000}]@10kHz	dBc/Hz	≤ -55	-62.8	-63.6	-62.7	-63.2	-61.8	-66.1	-66.5	-64.7	-65.4	-63.7
PN[b_{0000}]@100kHz	dBc/Hz	≤ -80	-88.0	-88.2	-88.0	-88.1	-87.6	-89.7	-90.0	-89.2	-89.4	-88.6
PN[b_{0000}]@1MHz	dBc/Hz	≤ -100	-109.3	-109.2	-109.4	-109.3	-109.4	-110.3	-110.6	-110.1	-110.2	-109.7
PN[b_{0000}]@10MHz	dBc/Hz	≤ -120	-129.5	-129.3	-129.5	-129.5	-129.7	-130.4	-130.6	-130.2	-130.3	-129.8
PN[b_{1111}]@10kHz	dBc/Hz	≤ -60	-60.4	**n/c**	**-59.2**[f]	-61.9	-62.2	-61.4	-61.7	-60.9	-62.1	-61.2
PN[b_{1111}]@100kHz	dBc/Hz	≤ -80	-85.5	**n/c**	-84.8	-86.3	-86.9	-86.8	-87.3	-86.5	-87.2	-86.3
PN[b_{1111}]@1MHz	dBc/Hz	≤ -100	-106.9	**n/c**	-106.4	-107.3	-108.1	-108.3	-109.0	-108.1	-108.5	-107.6
PN[b_{1111}]@10MHz	dBc/Hz	≤ -120	-127.0	**n/c**	-126.6	-127.4	**-128.3**	-128.5	-129.2	-128.2	-128.6	**-127.6**[w]
power[b_{0000}]	mW	n/d	0.246	0.291	2.415	0.250	0.267	0.302	0.325	0.295	0.309	0.286
power[b_{1111}]	mW	n/d	0.251	**n/c**	2.451	0.257	0.274	0.322	**0.348**[w]	0.314	0.329	0.305
FOM[b_{0000}]@10kHz	dBc/Hz	≥ 170	183.0	184.1	183.0	183.3	181.6	185.8	185.9	184.6	185.0	183.7
FOM[b_{0000}]@100kHz	dBc/Hz	≥ 180	188.2	188.7	188.3	188.3	187.5	189.4	189.4	189.0	189.0	188.5
FOM[b_{0000}]@1MHz	dBc/Hz	≥ 180	189.5	189.7	189.7	189.4	189.2	190.0	190.0	189.9	189.8	189.6
FOM[b_{0000}]@10MHz	dBc/Hz	≥ 180	189.7	189.8	189.9	189.6	189.5	190.1	190.0	190.0	189.9	189.7
FOM[b_{1111}]@10kHz	dBc/Hz	≥ 170	179.2	**n/c**	178.2	180.7	180.6	179.5	179.5	179.1	180.2	179.6
FOM[b_{1111}]@100kHz	dBc/Hz	≥ 180	184.3	**n/c**	183.8	185.0	185.4	184.9	185.1	184.7	185.2	184.7
FOM[b_{1111}]@1MHz	dBc/Hz	≥ 180	185.7	**n/c**	185.4	186.0	186.6	186.4	186.8	186.3	186.5	186.0
FOM[b_{1111}]@10MHz	dBc/Hz	≥ 180	185.9	**n/c**	185.6	186.1	186.7	186.6	187.0	186.5	186.6	186.0

[f] Performances failing specification; [w] Worst-case performances; **n/c** the simulation did not converged;

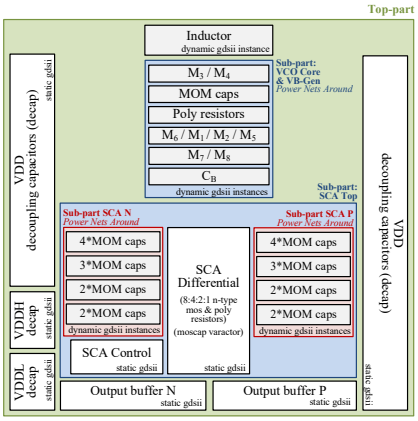

Fig. 3. Graphical representation of the template hierarchy used for the placement generation.

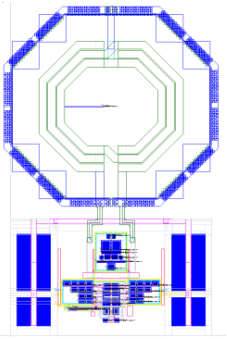

Fig. 4. Automatically generated layout.

IV. CONCLUSION & FUTURE RESEARCH DIRECTIONS

EDA tools are long-known for dealing with problems beyond human capabilities, such as considering simultaneously a large amount of conflicting pre-/post-layout performance in the design of RF circuits. In this paper, the IoT-VCO proposed for a 65 nm PDK still hinders the straightforward application of layout-aware sizing tools, as it is pushing the computational capabilities of modern workstations to its limits. Nonetheless, the extensive use of automatic sizing and layout methodologies allowed to take a realistic insight of the post-layout potential of a several candidate sizing solutions, and, eased the process of obtaining a competitive design, that fulfills all specification, for further fabrication. As future research directions, it is desired to use accurate electromagnetic-simulated [12] inductor performances in-the-loop, as well as performing full layout-aware optimization. However, before committing to the latter, it is important to understand several aspects: (1) deciding when to stop simulator convergence attempts is a delicate decision. If stopped earlier, a promising solution may be lost. If a lot of CPU time is allowed without success, it may represent days/months of computational time lost; (2) the guessed oscillation frequencies in the SSTs have a direct effect in their output, as the same solution may converge or not by similar guessed frequencies. A possible work around is to optimize the guess frequency too or simulate multiple guesses; and (3), similarly, the layout generation may attain a solution with short-circuits, not necessarily meaning that the sizing solution was bad, but that the layout generation need to be re-optimized.

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