23.5 An Inverse-Class-F CMOS VCO with Intrinsic-High-Q 1st- and 2nd-Harmonic Resonances for 1/f²-to-1/f³ Phase-Noise Suppression Achieving 196.2dBc/Hz FOM

Chee-Cheow Lim[1,2], Jun Yin[1], Pui-In Mak[1], Harikrishnan Ramiah[2], Rui P. Martins[1,3]

[1]University of Macau, Macau, China
[2]University of Malaya, Kuala Lumpur, Malaysia
[3]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

Second-harmonic common-mode (CM) resonance has been explored for LC oscillators to improve their phase noise (PN) in the past. Its implementation evolves from an explicit design [1] that relies on an extra tail tank, to a recent implicit design [2], where the resonator itself offers a CM impedance peak at 2× the oscillation frequency (F_{LO}):

Explicit design (Fig. 23.5.1-upper): a high-Q tail tank (Q_{TAIL}) is desirable to raise its impedance $|Z_{TAIL}|$ at $2F_{LO}$ and to prevent the loss of L_{TAIL} from penalizing the PN in the 1/f² region [3]. To compare with the theoretical limit (FOM_{MAX}), the FOM in the 1/f² PN region is plotted against L_{TAIL} at different Q_{TAIL}. Closing the gap between FOM_{MAX} and FOM imposes an excessive Q_{TAIL} of 20 or beyond, which can hardly be achieved and maintained over a wide tuning range.

Implicit design (Fig. 23.5.1-lower): a CM resonance at $2F_{LO}$ can avoid the physical area and loss of the tail tank. Besides, if the 2nd-harmonic current is trapped in the resistive impedance at $2F_{LO}$ due to the CM resonance, the flicker-noise upconversion can be suppressed [4]. Yet, its practical effectiveness is limited by the presence of PN, which renders both F_{LO} and $2F_{LO}$ to drift randomly around their resonances. If the 2nd-harmonic current spends more time "trapped" in the resistive part of the tank, the effect of flicker-noise upconversion can be further reduced, but it demands a high-Q impedance at $2F_{LO}$. Unfortunately, the implicit CM impedance $|Z_{CM}|$ is relatively low for two reasons: 1) CM inductance $L_{CM}=L(1-k)$ is small due to magnetic-flux cancellation and 2) the CM resonance has a low Q at $2F_{LO}$ up to ~1/4 of its differential-mode counterpart [4] (i.e. $Q_2/Q_1\approx0.25$). Although lowering k returns a higher Z_{CM}, more die area is sacrificed, and the required CM capacitance becomes exceedingly small.

This paper proposes an inverse-Class-F CMOS VCO free of CM resonance. A transformer-based dual-band LC resonator generates two intrinsic-high-Q resonances at F_{LO} (denoted Q_1) and $2F_{LO}$ (denoted Q_2). A high Q_2 corresponds to low PN in both 1/f² to 1/f³ regions, while the transformer voltage gain aids suppressing the thermal noise contributed by the $-g_m$ transistors. The high-Q resonances lead to high FOMs at both 100kHz offset (191-to-192.5dBc/Hz) and 10MHz offset (195.6-to-196.2dBc/Hz) over 3.49 to 4.51GHz, while showing low frequency pushing (4.5 to 15MHz/V).

Let us consider a single-ended NMOS VCO using a 1:n transformer (Fig. 23.5.2) to satisfy Barkhausen's criterion. The transformer model [5] reveals that two impedance peaks can be produced despite the VCO being single-ended. To map them at F_{LO} and $2F_{LO}$, we have to satisfy $16\xi^2-68\xi+100\xi k_m^2+16=0$ for a mutual coupling factor $0.3\le k_m\le0.6$, where ξ is the product of the transformer inductance ratio (L_S/L_P) and capacitance ratio (C_S/C_P), arriving at the inverse-Class-F operation. It implies that the effective inductance at F_{LO} ($2F_{LO}$) is determined not only by L_p (L_s), but also ξ and k_m. Increasing the tank impedance at $2F_{LO}$ is feasible by sizing $\xi>1$. Based on Fig. 23.5.2, a small k_m (0.34) is desired to raise ξ (3.2), leading to a higher Q_2/Q_1 ratio (0.8) than that of [2] by 3.2× and a large transformer voltage gain (A_V) resulting in a low-PN VCO design. For a low-power VCO design, a moderate ξ is desired for a high impedance at F_{LO}, without disproportionately degrading A_V and Q_2.

By stacking such a single-ended NMOS (M_N) VCO with its PMOS (M_P) counterpart, and merging their respective tanks as a single transformer, an inverse-Class-F CMOS VCO is developed with V_{GP} and V_{GN} as the differential outputs (Fig. 23.5.3). Shorting the center taps of the two coils (L_s and L_P) realizes self-biasing at $V_{DD}/2$, provided that M_P and M_N have a matched large-signal transconductance (G_M). The VCO can also be viewed as a 2-port resonator. By ensuring $M_{P,N}$ are under positive feedback, oscillation only occurs at F_{LO} even if there is a higher impedance at $2F_{LO}$ than F_{LO}. C_S (5 bits, LSB: 20fF) mainly responds for F_{LO}, such that C_P (6 bits, LSB: 11fF) can be tuned for F_{LO} and $2F_{LO}$ alignment.

Unlike the differential VCO where the $-g_m$ transistors are switched on-and-off alternately, here they are switched on (first ½ period) and off (another ½ period) simultaneously. Since the fundamental and 2nd harmonic currents are in-phase here (Fig. 23.5.3), when they see their respective resistive paths at F_{LO} and $2F_{LO}$ resonances, they result in an asymmetric voltage waveform at the drain, showing a flat span at $V_{DD}/2$. A large voltage gain at the gate provided by the transformer drives both M_P and M_N into the deep triode region, clipping their drain voltage close to V_{DD} and 0V, respectively. Using the linear time-variant model [6], the Impulse Sensitivity Function (ISF, Γ) is around zero at these aforesaid two regions. Hence, the noise factor induced by the tank ($2\Gamma^2_{RMS}$) is lowered from 1 (Class-B & C) to 0.37 (inverse-Class-F). Specifically, the falling and rising times at the drain voltage exhibit different maximum derivatives, resulting in asymmetric ISF between the upper and lower regions. Besides, since channel-length modulation dominates in deep sub-micron CMOS, a harmonically shaped drain voltage gives rise to asymmetric G_M. Interestingly, the product of a higher G_M and a lower ISF (and vice versa) in the vicinity of 0 (π) phase yields a zero DC value for the effective ISF of G_M and thereby prevents the flicker-noise upconversion.

Due to the presence of harmonic voltages, the FOM of a VCO can be expressed as

$$FOM=10\log_{10}\left(\frac{2Q_1^2\alpha_I\alpha_V}{10^3kT\sum F}\right)$$

where T is the absolute temperature, k is Boltzmann constant, $\alpha_I=I_{FLO}/I_{DC}$ is the current efficiency, α_V is the voltage efficiency defined as a ratio of the oscillation amplitude at the drain ($V_{DP,DN}$) to V_{DD}, and ΣF is the total noise factor of the VCO contributed by the resonator and transistors (Fig. 23.5.3). If F_{LO} and $2F_{LO}$ can be perfectly aligned at an optimum point of C_P=0.57pF and assuming Q_1=12, the calculated FOM (196.3dBc/Hz) of this work is beyond that of Class-F_3 (192.7dBc/Hz at α_I=0.63, α_V=0.8 and ΣF=1.88) and Class-C (192.5dBc/Hz at α_I=0.9, α_V=0.7 and ΣF=2.46). At this point, α_I=1.35 and α_V=0.47, and ΣF is as low as 1.04 by taking the ISF into account. When C_P increases slightly, the FOM at 1/f² region goes up to 196.8dBc/Hz because Q_1 raises before ΣF dominates the degradation. Since A_V and Q_1 are both function of ξ [5], FOM_{MAX} varies with C_P. A high Q_2 also benefits the frequency pushing from V_{DD} caused by the Groszkowski effect. Thus, the frequency pushing of our VCO is only dominated by the inevitable nonlinear capacitances (varactor and parasitic).

The VCO occupies 0.14mm² in 65nm CMOS. It utilizes a 2-to-4-turn transformer with L_P=2.2nH and L_S=4.2nH. The simulated Q_1 is 11.5 and Q_2 is 9.2. Figure 23.5.4 shows the measured PN at 3.49GHz (f_{MIN}) and 4.51GHz (f_{MAX}). Consistent FOMs at 100kHz offset (191 to 192.5dBc/Hz) and 10MHz offset (195.6 to 196.2dBc/Hz) are achieved. The 1/f³ corner is 100kHz at f_{MIN} and up to 300kHz at f_{MAX} due to the AM-PM conversion when the varactor and parasitic capacitance dominate. Figure 23.5.5 shows the PN and FOM plots across the frequency tuning range and its pushing by V_{DD}. The FOM at 1/f² region varies within ±0.5dB and peaks to 196.2dBc/Hz. The frequency pushing is 4.5MHz/V at f_{MIN} dominated by the varactor capacitance and -15MHz/V at f_{MAX} dominated by the capacitor-bank parasitics. The latter is still 2× lower than that of [2] that is up to 30MHz/V.

Benchmarking with the prior art (Fig. 23.5.6), our inverse-Class-F CMOS VCO exhibits the highest FOMs at both 100kHz and 10MHz offsets over a comparable tuning range, while achieving low frequency pushing, which is among the best reported in Fig. 23.5.6. The die micrograph of the VCO is depicted in Fig. 23.5.7.

Acknowledgements:
The authors thank Macau Science and Technology Development Fund (FDCT) - SKL Fund and University of Macau - MYRG2017-00185-AMSV for financial support.

References:

[1] E. Hegazi, et al., "A Filtering Technique to Lower LC Oscillator Phase Noise," *IEEE JSSC*, vol. 36, no. 12, pp. 1921-1930, Dec. 2001.
[2] D. Murphy, et al., "Implicit Common-Mode Resonance in *LC* Oscillators," *IEEE JSSC*, vol. 52, no. 3, pp. 812-821, Mar. 2017.
[3] M. Garampazzi, et al., "Analysis and Design of a 195.6 dBc/Hz Peak FoM P-N Class-B oscillator with Transformer-Based Tail Filtering." *IEEE JSSC*, vol. 50, no. 7, pp. 1657-1668, July 2015.
[4] M. Shahmohammadi, et al., "A 1/f Noise Upconversion Reduction Technique Applied to Class-D and Class-F Oscillators," *ISSCC*, pp. 444-445, Feb. 2015.
[5] A. Mazzanti and A. Bevilacqua, "On the Phase Noise Performance of Transformer-Based CMOS Differential-Pair Harmonic Oscillators," *IEEE TCAS-I*, vol. 62, no. 9, pp. 2334-2341, Sept. 2015.
[6] A. Hajimiri and T. Lee, "A General Theory of Phase Noise in Electrical Oscillators," *IEEE JSSC*, vol. 33, no. 2, pp. 179-194, Feb. 1998.

 978-1-5090-4940-0/18/$31.00 ©2018 IEEE

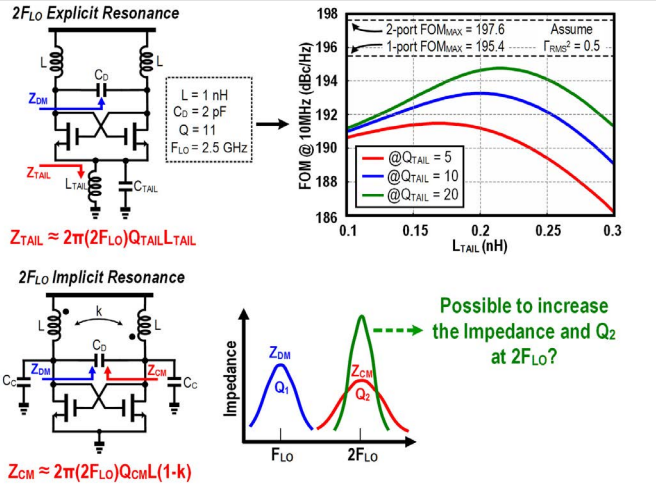

Figure 23.5.1: Upper: VCO with explicit $2F_{LO}$ resonance [1] and its FOM dependence on Q_{TAIL}. Lower: VCO with implicit $2F_{LO}$ resonance [2] to avoid an extra LC tank, but the implicit CM resonance has low impedance and low Q at $2F_{LO}$.

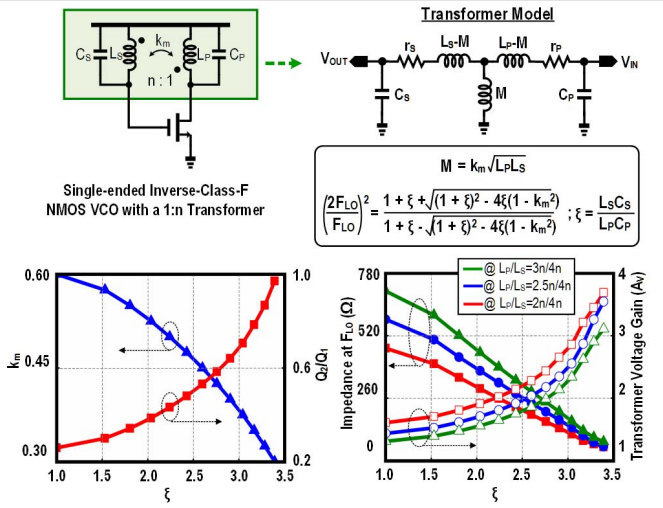

Figure 23.5.2: A single-ended NMOS VCO using a 1:n transformer; the transformer model reveals that 2 impedance peaks can be generated at F_{LO} and $2F_{LO}$. ξ=3.2 and k_m=0.34 yield high Q_2/Q_1 ratio (0.8) and A_V.

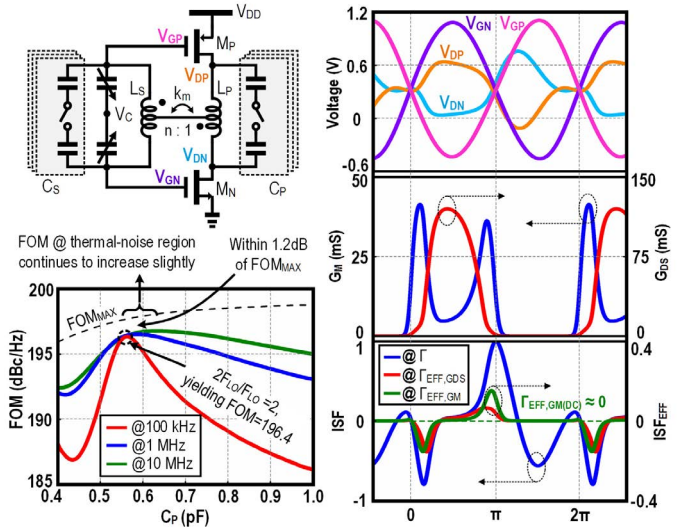

Figure 23.5.3: Proposed inverse-Class-F CMOS VCO. By varying C_P and C_S, F_{LO} and $2F_{LO}$ can be aligned to suppress the flicker-noise upconversion.

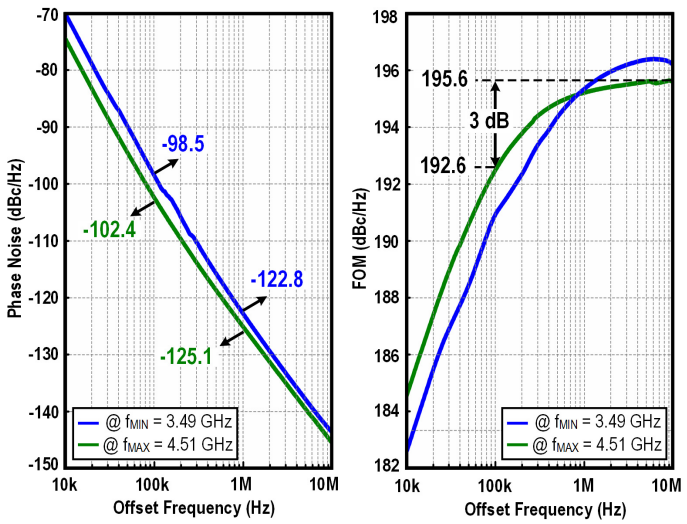

Figure 23.5.4: Measured phase noise and FOM at different offset frequencies.

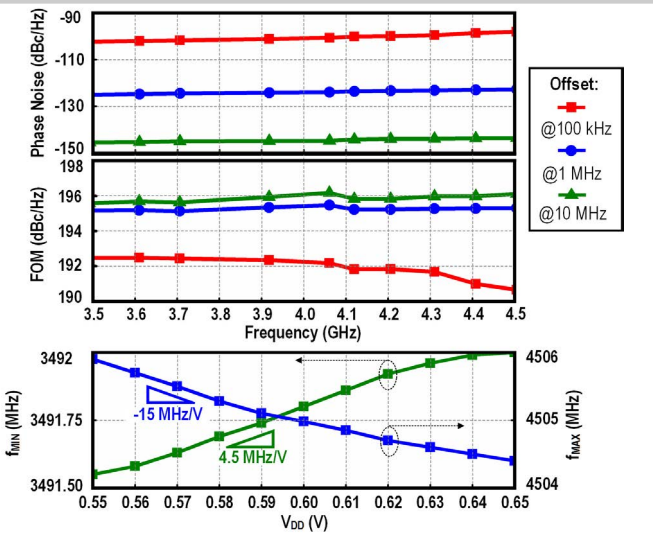

Figure 23.5.5: Upper: Measured phase noise and FOM vs. the oscillation frequency. Lower: Measured frequency pushing at f_{MIN} and f_{MAX}.

	This Work		ISSSC'17 [C-C. Li et al.]	JSSC'17 [2]	ISSCC'15 [4]	JSSC'13 [M. Babaie et al.]	JSSC'08 [A. Mazzanti et al.]	JSSC'01 [1]
Topology	CMOS Inverse-Class-F		Trifilar Coil	NMOS CM resonance	Class-$F_{2,3}$	Class-F	Class-C	NMOS+2F_{LO} tail inductor
CMOS Tech.	65nm		16nm	28nm	40nm	65nm	130nm	0.35μm
Tuning Range	3.49-4.51 (25.5%)		3.2-4.0 (22%)	2.85-3.75 (27.2)	5.4-7 (25%)	2.95-3.8 & (25%)	4.9-5.65 (14%)	1-1.2 (18%)
V_{DD} (V)	0.6		0.4	0.9	1	1.25	1	2.5
Freq. (GHz)	3.49	4.51	3.23	2.89	5.4	3.7	4.9	1.2
Power (mW)	1.2	1.14	3.8	6.8	12	15	1.4	9.1
PN (dBc/Hz) @ 100k/10MHz	-102.4/ -145.6	-98.5/ -143.7	-99 */ -145	-108.1/ -152	-105.3/ -146.7	-103.6/ -152.8	-99 */ -142 #	-117 */ -162.5 #
FOM (dBc/Hz) @ 100k/10MHz	**192.5/ 195.6**	**191/ 196.2**	183.3/ 190	188/ 192.5	189.1/ 190.5	183.2/ 192.4	191.3/ 194.4	189/ 195
Freq. Pushing (MHz/V)	**4.5**	**15**	3.6-27.3	6-30	12-23	18-50	N/A	N/A
1/f³ Corner (kHz)	100	300	120	200	60	700	200	N/A
Die Area (mm²)	0.14		0.11	0.19	0.13	0.12	N/A	N/A

*Estimated from PN plot #Normalized from 1 MHz offset &After on-chip div-by-2

$$FOM = -PN + 20\log_{10}(f_0/\Delta f) - 10\log_{10}(P_{DC}/1mW)$$

Figure 23.5.6: Performance benchmark with the previously published VCOs.

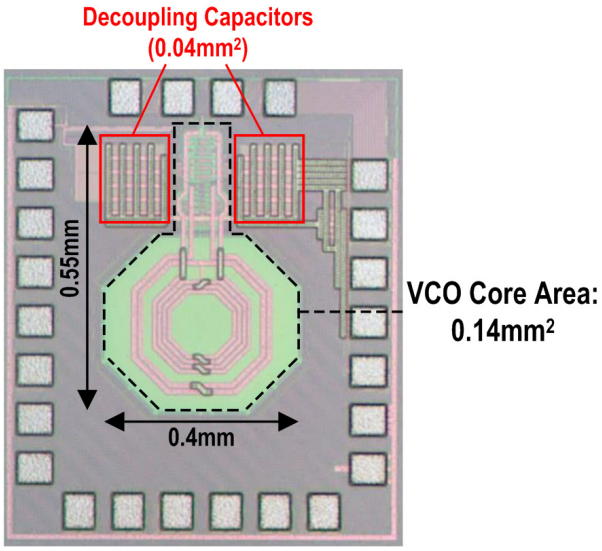

Figure 23.5.7: Die micrograph of the fabricated VCO in 65nm CMOS.

978-1-5090-4940-0/18/$31.00 ©2018 IEEE