A GENERALIZED TIMING-SKEW-FREE, MULTI-PHASE CLOCK GENERATION PLATFORM FOR PARALLEL SAMPLED-DATA SYSTEMS

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ABSTRACT

This paper presents a comprehensive analysis of mismatch-insensitive clock generation techniques for general parallel sampled-data systems. Two jitter-insensitive clock generation schemes are described, and a novel class of multi-purpose, low-jitter, multi-phase clock generator platform will be proposed. The platform can provide clock phases for the two pre-described clock generation schemes and has the advantages of being insensitive to timing mismatches, having a simple and highly robust architecture such that the clock generator can be generalized not only for an arbitrary number N of time-interleaved (TI) paths, but also can be applied to general TI sampled data systems including ADCs, DACs and N-path filters.

1. INTRODUCTION

High-speed sampled-data systems are experiencing an increasingly demand from the present telecommunication systems, as well as, from other signal processing applications, like for example, the single-chip CMOS receiver [1], the digital oscilloscope and RGB-LCD display conversion [2]. Time-Interleaved (TI) architectures are one of the effective solutions to the high-speed sampled-data systems, but they suffer from periodic timing skew that produces modulation images at frequency locations of multiples of f_s/M (f_s-overall sampling rate, M-period of timing skew), which are caused by timing mismatches in different time-interleaved paths [3]. These images will severely affect, especially, the dynamic range of TI-sampled data systems in very high-speed applications. As the sampling frequency increases beyond 100MHz, the design of a low-jitter, non-overlapping clock generator becomes a critical task to ensure a satisfactory performance of such high-speed systems.

Various techniques had been reported in the literature to produce low-jitter sampling clocks. One of such techniques uses delay lock loop (DLL) to compensate the timing-jitter [4], but it suffers from complex control and delay sensing circuitry, and the clock de-skew performance is also limited by the speed of the DLL. A more accurate technique comprises the utilization of precise clock edges, such as those from master clock [2-7], to reduce the timing skew, which can be classified in two main categories according to the nature of the assignment, and designated as edge-driven clocking or edge-driven switching. In this paper, both schemes of low-jitter clock generation techniques are described, and a novel class of multi-purpose, low-jitter multi-phase non-overlapping clock generation platform will be proposed. This new platform is generalized for different applications, including TI ADCs, DACs and N-path sampled-data filtering, and it also provides the clock signals for both the clocking and switching schemes. It presents significant advantages due to the simple circuit architecture and the high robustness that allows its extended operation to multi-phase with a low hardware cost.

2. CLOCK EDGES REQUIREMENTS

The sampling instants of sampled-data systems are defined either at the rising or falling edges of the sampling clock, thus implying that the clock edges inaccuracy would be directly related to the timing jitter. Considering, for example, an SC TI sample-and-hold (S/H) circuit from an A/D conversion path [8], as shown in Fig. 1(a), that is a typical example of a TI sampled-data system with N paths. As it is common in SC circuits, they usually require multi-phase non-overlapping clock signals $\phi_1 \ldots \phi_N$ and $\phi_{1'} \ldots \phi_{N'}$ to control the analog switches. Thus, in order to minimize the effect of signal-dependent charge injection and clock feedthrough errors [2] in the sampling capacitors $C_1 \ldots C_N$, the switches controlled by pre-phases $\phi_{1p} \ldots \phi_{Np}$ will be opened slightly earlier than the post-phases $\phi_1 \ldots \phi_N$, which means that the falling edges of the pre-phases should appear slightly earlier than that of the post-phases as shown in Fig. 2(a). On the other hand, for certain applications with higher accuracy, the rising edges of the pre-phases could be placed also slightly earlier than that of post-phases to further suppress the charge injection errors (with small loss on the available settling time of the opamp) [9]. However, for better settling of the opamps, both phases can rise together as shown in all edges, in gray-color, in Fig. 2(a). Inaccurate sampling clock edges produce periodic timing skew with period M=N and, consequently through this arrangement, the **falling edges** of the **pre-phases** would become the critical edges to be controlled for avoiding timing skew in **A/D conversion paths** [2].

Similarly, for the TI D/A conversion path an output multiplexer is typically utilized, as shown in Fig. 1(b), to produce high-speed output [6]. Since the charges in the capacitors are transferred to the outputs once the switches $\phi_1 \ldots \phi_N$ are turned on, the critical edges are the **rising edges** of the **post-phases** (or both-phases if they rise together) in the **D/A conversion path**, as presented in Fig. 2(b) [6].

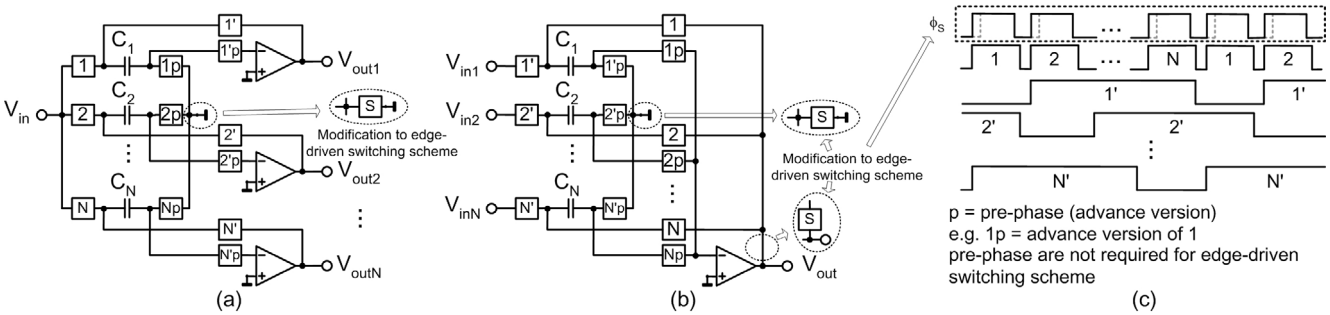

Fig. 1: SC sampled-and-hold and multiplexer circuits used in time-interleaved sampled-data systems (modifications to edge-driven switching scheme are also shown): (a) Input S/H circuit; (b) Output multiplexer circuit; (c) Timing-diagram of both circuits

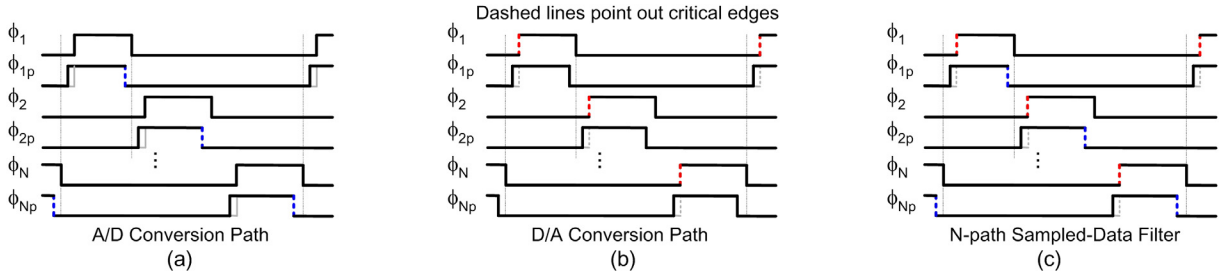

Fig. 2: Timing diagram to illustrate the critical clock edges: (a) A/D, (b) D/A conversion & (c) N-path sampled-data filtering

Finally, for **general sampled data systems** such as *N*-path filters, both S/H and multiplexer are utilized for input sampling and output play-out, implying that **both edges** described previously will become critical edges. Fig. 2 summarizes the clock waveforms and critical sampling edges for these three different cases.

3. JITTER-INSENSITIVE CLOCK GENERATION TECHNIQUES

The timing skew effects can be greatly reduced by using a method called "Clock Edge Reassignment", in which all the critical sampling edges are assigned by only one of the accurate master clock edges (either falling or rising). According to the nature of the assignment of clock edges, this technique can be classified into two categories: edge-driven clocking or edge-driven switching.

A. Edge-Driven Clocking

This scheme imposes the reduction of the effect of timing skew by accurate control of the clock edge timing. Previously [2-6], such concept has been utilized, and the critical sampling edges of the clock are "reassigned" by another clock signal that possesses an accurate edging time. Such accurate clock sampling will considerably reduce the timing skew and it allows the use (without any modifications) of traditional S/H or multiplexer circuits, as in Fig. 1.

B. Edge-Driven Switching

In addition to the generation of low-jitter multi-phase clock signals by controlling the accuracy of the clock edges, an alternative approach that uses common sampling switches to avoid the timing skew was described in [7], and designated as "Edge-Driven Switching".

The method utilizes a common sampling switch between various paths that is controlled by the common sampling clock ϕ_S operated at full sampling rate, as shown in the modifications presented in Fig. 1. The clock ϕ_S possesses a series of short negative pulses, controlling the common sampling switch to be closed slightly earlier than the regular clock phases $\phi_1 \ldots \phi_N$, thus the sampling instants are determined by ϕ_S for A/D conversion which implies that the sampling circuit in Fig. 1(a), even without a set of pre-phases, is free from timing skew influence. For D/A conversion and N-path filters, the multiplexer circuits can be modified with an additional switch S added in the output (Fig. 1(b)). The switch S in the sampling part of the multiplexer is still required to avoid charge injection errors. In this scheme, all clock phases of the multiplexer are identical to those of Fig. 1(a).

4. A NOVEL GENERALIZED LOW-JITTER CLOCK GENERATION PLATFORM

Using the previous mentioned techniques a novel, multi-purpose platform for generation of low-jitter, multi-phase non-overlapping clock phases has been developed. This platform is generalized for applications of A/D Conversion (including decimators), D/A Conversion (including interpolators) and N-path sampled-data filtering. Fig. 3 shows the block and timing diagrams of the three proposed clock generators, whereas in Figs. 3(a) and 3(b) Edge-Driven Clocking is presented (relying on accurate control of application-specific clock edges to reduce timing-skew errors) for A/D conversion and D/A conversion or N-path filtering, respectively, and in Fig. 3(c) Edge-Driven Switching is addressed. On the other hand, Fig. 4 exhibits the clock generator platform containing the following building blocks:

A. Master-slave D-flip-flop with master output

Fig. 4(a) shows a master-slave D-flip-flop (DFF) with an additional master output that is extracted from the master latch. With such arrangement the master (M) output signal always leads the slave (Q) quadraturely.

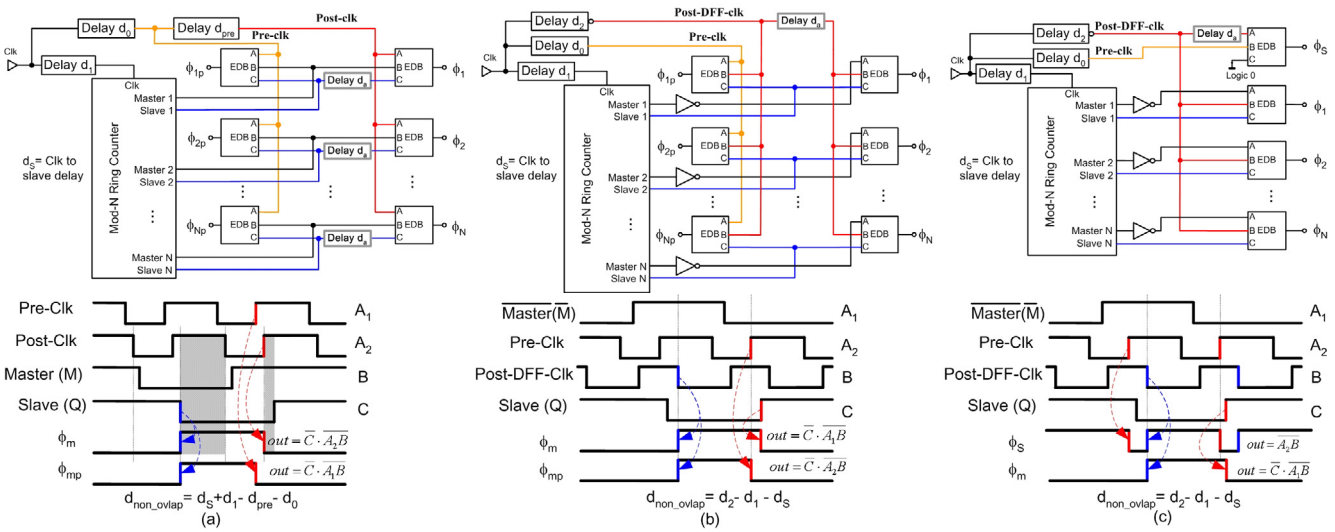

Fig. 3: Proposed block and timing diagrams of the low-jitter multi-phase clock generation platform for (a) A/D conversion; (b) D/A conversion and N-path filtering (Edge-Driven Clocking) and (c) Edge-Driven Switching.

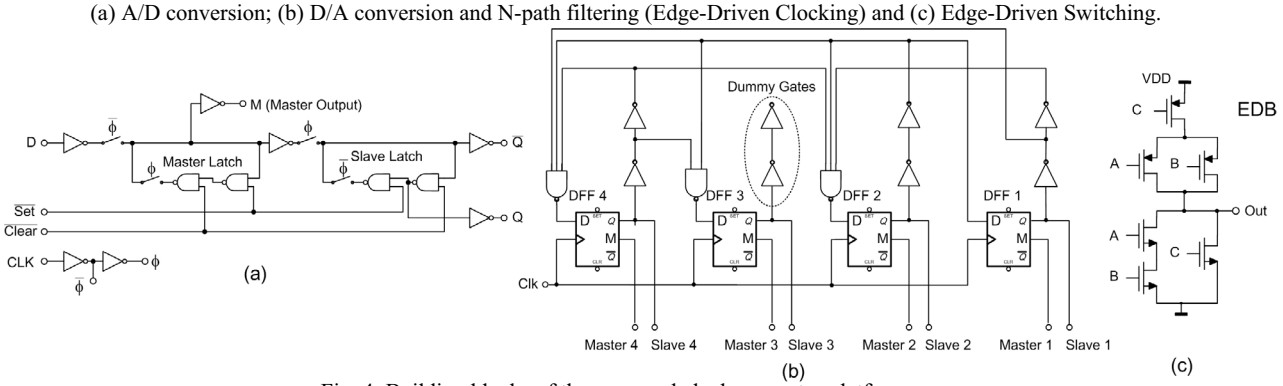

Fig. 4: Building blocks of the proposed clock generator platform: (a) Master-slave DFF with master output; (b) Self-starting mod-4 ring counter; (c) Edge Decision Block (EDB)

B. Self-starting mod-N ring counter

The self-starting mod-N ring counter is designed to provide shifted negative pulses, which serve as envelopes of various multi-phase clock signals to ensure a non-overlapping operation. Fig. 4(b) shows an example of self-starting mod-4 ring counter, where dummy gates are used to balance the loading conditions of Q and M outputs.

C. Edge Decision Block (EDB)

Since for A/D converters (or decimators) the critical sampling edges are on the falling edges of the pre-phases, these falling edges will be "assigned" by the rising edges of an accurate clock (pre/post-clk, delay version of master clock by d_0 and d_0+d_{pre} respectively), as it is presented in Fig. 3(a) together with the resulting clock phase outputs ϕ_{mp}/ϕ_m (m=1…N). However, this assignment is not possible, as it can be verified for example in the shaded area of the figure, where the post-clk signal is equal to 1 and the slave (Q) is 0 in both areas while the output ϕ_m is dissimilar. In order to identify separately these two regions a master output M from the DFF serves as a boundary between the shaded areas. According to the assignment of alphabetic letters shown in the figure, the logic function that implements the desired output is given by

$$out = \overline{C} \cdot \overline{AB} \qquad (1)$$

and the circuit diagram shown in Fig. 4(c), called "Edge Decision Block" (EDB), can be used to implement such a logic function. Also, the function of all shaded delay block d_a in Fig. 3 is used to provide a delay between the rising edges of pre- and post-phases to further reduce charge injection errors. The amount of non-overlapping time delay is also shown in Fig. 3.

In the second circuit used with D/A converters (or interpolators) or *N*-path filters, both the rising edges of the post-phases (or both phases) and the falling edges of the pre-phases become vital. These two critical edges can be controlled simultaneously by the use of identical EDB blocks as previously mentioned, but with different signals routing as shown in Fig. 3(b). The rising edges of both phases are determined by the falling edges of the post-DFF-clk, while the falling edges of the pre-phases are assigned by the rising edges of pre-clk. Since both the pre-clk and post-DFF-clk are delayed versions (by d_0 and d_2 respectively) of the master clock, the *N*-phases produced are accurate in the rising edges of both phases and in the falling edges of the pre-phases, thus suitable in DAC applications, interpolating filters, and *N*-path sampled-data filters. The bubble on the delay d_2 indicates a logic inversion of the delay output.

Finally for the Edge-Driven Switching of Fig. 3(c), since all the pre-phase functions are replaced by a common sampling clock ϕ_S, the corresponding blocks that are responsible for generation of the pre-phases have been removed. Moreover, the blocks that generate various multi-phase non-overlapping clocks

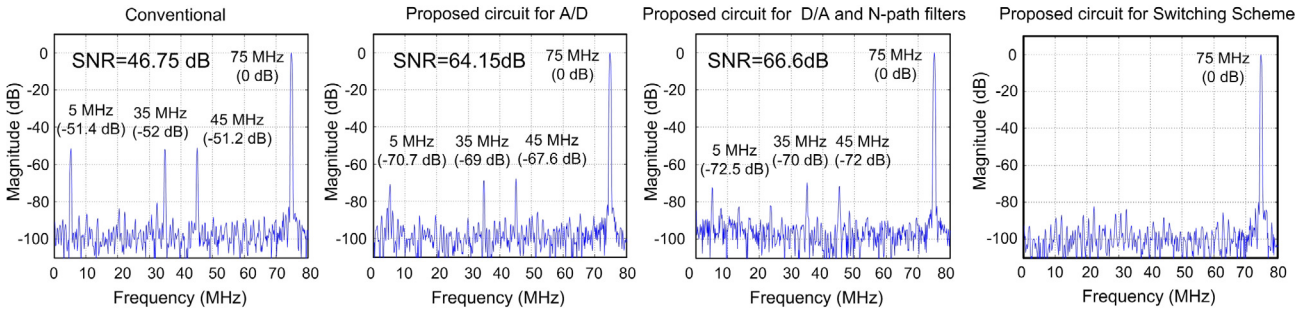

Fig. 5: Hspice FFT simulation results for the various clock generators: (a) conventional; (b) proposed circuits for A/D conversion; (c) for D/A and N-path filters (Edge-Driven Clocking) and (d) for Edge-Driven Switching

$\phi_1,\ldots\phi_N$ are exactly identical to their corresponding parts in the D/A conversion circuit of Fig. 3(b), and only the common sampling clock ϕ_S needs to be determined. The falling and rising edges of phase ϕ_S are determined by the rising edges of "pre-clk" and the falling edges of "post-DFF-clk", respectively, producing ϕ_S that has the same period T_{clk} of the master clock. As shown in the timing diagram of Fig. 3(c), the falling edges of phases $\phi_1 \sim \phi_N$ are always enclosed in the negative pulse of ϕ_S due to the various delays presented in Fig. 3(c), thus all the clock signals required by the Edge-Driven Switching scheme can be produced. Such assignment of ϕ_S can be achieved by a simple NAND function. However, to maximize the delay matching, the EDB with the C terminal connected to logic 0 is used instead.

5. SIMULATION RESULTS

In order to verify the effectiveness of the proposed clock generation platform, a 4-phase version of the clock generators were simulated with Hspice with the master clock frequency set at 160 MHz (also the overall sampling rate).

The designed clock generators are used to drive the switches in the TI S/H or multiplexer circuits, to sample or play out a 75 MHz sinusoidal signal with the overall sampling frequency of 160 MHz. Fig. 5(a) shows the FFT output spectrum for the S/H circuits that are driven by the 4-phase version of the conventional clock generator from [10] that has no control over clock edge accuracies. The spectrum shows 3 mismatch-induced image tones appearing at frequency 5, 35, 45 MHz, respectively, and only 46.75 dB SNR is achieved, corresponding to 13 ps timing mismatches by the formula derived in [3]. Fig. 5(b) and (c) shows the corresponding spectrum with the proposed clock generator (used in A/D and D/A conversion) and the image tones are effectively reduced with an SNR of 64.15 dB and 66.6 dB respectively (less than 2 ps timing mismatches), corresponding to 17~19 dB improvement. Finally, the third proposed circuit from Fig. 3(c) (Edge-Driven Switching) by its nature doesn't produce any mismatch-induced image tones in the spectrum of Fig. 5(d).

6. CONCLUSIONS

A thorough and generalized analysis on multi-phase clock generation techniques to reduce timing skew effects in parallel or time-interleaved sampled-data systems has been presented, and two approaches are described to reduce the effects of timing skew: Edge-Driven Clocking and Edge-Driven Switching. Then, a novel multi-purpose, low-jitter, multi-phase non-overlapping clock generation platform is proposed. The platform is generalized to provide clocking phases for the two pre-described schemes, and also to all three classes of TI sampled-data systems including A/D conversion, D/A conversion and a complete sampled data system (*N* path filters). Simulations with Hspice are performed to verify the effectiveness of the proposed clock generation techniques. Hspice simulation results shows 17 dB improvement in SNR compared with the conventional clock generator as verified by the FFT analysis of the simulated results.

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