A 29mW 5GS/s Time-interleaved SAR ADC achieving 48.5dB SNDR With Fully-Digital Timing-Skew Calibration Based on Digital-Mixing

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Abstract

This paper presents a 5GS/s 16-way Time-Interleaved SAR ADC in 28nm CMOS, proposing a fully-digital background timing-skew calibration based on digital mixing, without adding any extra analog circuits. We implement the sub-channel SAR with a splitting-combined monotonic switching procedure. The prototype ADC achieves 48.5dB SNDR at Nyquist rate, while the power consumption is 29mW leading to a Walden FOM of 26.7fJ/conv-step.

Introduction

Generic high-speed applications with excellent power efficiency usually prefer in their architectures a Time-interleaved (TI) SAR ADC. However, additional interleaved ADC slices to reach higher speeds normally impose more complicated mismatch corrections, especially the timing-skew calibration. Therefore, a simple skew calibration and a high-speed low-power single-channel SAR are the two critical issues in the TI SAR. Digital mixing [1-3] is an effective way to detect the skew error, by utilizing the difference of the input autocorrelation function induced by timing skew, which is faster than [4] that is based on the orthogonal property of the input signal and its derivative. However, [1-2] made the correction by analog-tuning the variable-delay line that suffers from poor feedback stability and additional clock jitter, while [3] corrects the skew error in the digital domain but requiring auxiliary converters.

In this paper, we present a fully digital method to detect and correct the timing mismatch, achieving -69.3dB mismatch spur at Nyquist rate with only 16k samples. Here, we'll also demonstrate a capacitive DAC splitting-combined monotonic switching method, which not only maintains the advantages of the simple switch and SAR logic implementation but also significantly reduces the variation of the comparator common mode voltage.

Calibration Method and the ADC Architecture

Fig.1 illustrates the concept of the overall fully digital calibration method (example with 2-channel), with the calibration part following the generic in [4]. Channel 1 and 2 sample the odd and even samples, respectively, with the even having a timing skew from its ideal value of ΔT, as shown in Fig. 1(a). We calculate the estimated timing error of channel 2 as the product between the derivative y_2' and timing skew ΔT, which is then subtracted from the channel 2 output to recover the ideal sample $y_{2,cal}$. As presented in Fig. 1(b), we obtain the even samples' derivative y_2' through a 25-tap differentiating

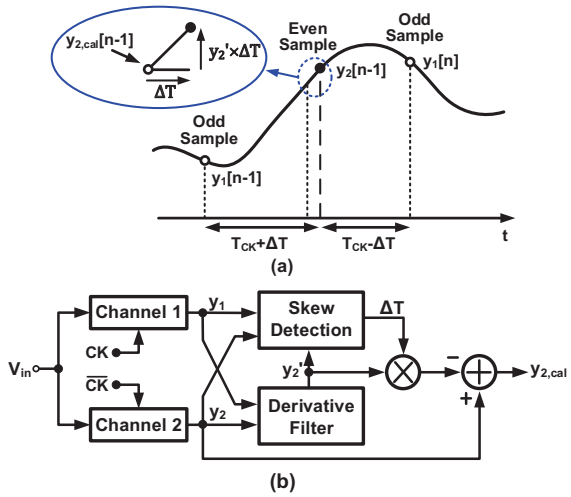

Fig. 1 (a)Waveform illustrating the effect of timing mismatch (b) Fully digital timing skew calibration diagram

FIR filter [4]. Moreover, implementing a Hilbert transform filter inside the derivative filter (Fig. 1), it allows the computation of the input's derivative over the Nyquist Band (NB).

To detect the timing-skew, [1] proposed a digital-mixing method presented in Fig. 2 as the bottom-left block. However, it can only obtain $\overline{D_{\Delta T}}$ which is the difference between $R_x(T_{CK}+\Delta T)$ and $R_x(T_{CK}-\Delta T)$, where R_x is the input autocorrelation function. So $\overline{D_{\Delta T}} = 2\Delta T \cdot \frac{dR_x}{d\tau}|_{\tau=T_{CK}}$ includes not only the timing skew ΔT, but also the signal-dependent information. As a result, we can only extract the polarity of the timing-skew from [1] for the analog-tuning of the delay line.

In this work, we require an explicit number for the value of the time skew to facilitate the fully-digital background calibration. We propose the additional algorithm as shown in the blue boxes highlighted in Fig. 2, which use the Moving Average (MA) to extract the derivative of the autocorrelation function $\frac{dR_x}{d\tau}|_{\tau=T_{CK}} = \frac{1}{n}\sum_n y_2'[k]\,y_1[k]$, by averaging the product of y_2' and y_1 (Fig. 2, as well). Then, the explicit amount of timing skew ΔT can be extracted by $2\Delta T = \overline{D_{\Delta T}}/(\frac{dR_x}{d\tau}|_{\tau=T_{CK}})$, which can be used to calibrate the timing-skew errors fully in digital and background (Fig. 1).

Fig. 3 shows the timing skew calibration sequence for the 16-way ADC. First, channel 1 serves as reference to calibrate channel 9, obtaining ΔT_9 from $R_x'(8T_{CK})$. After channel 9 is skew-free, channel 1 and 9 as references to calibrate channel 5 and 13, and it obtains ΔT_5 and ΔT_{13} from $R_x'(4T_{CK})$. The 16-channel ADC needs 4 calibration steps.

Fig.4 shows the circuit diagrams of the implemented capacitive DAC of the single-channel SAR ADC, using the

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splitting-combined monotonic switching procedure. To overcome the DAC incomplete settling error, it uses 11-cycle to obtain 10-b accuracy [5]. Two MSB DAC splitting reduce the variation of the comparator input common-mode voltage by ~72% when compared with the pure monotonic switching. We obtain the remaining 9 LSBs in the conventional monotonic way. Therefore, the proposed DAC not only maintains the advantage of simple switches and SAR logic, but also significantly reduces the signal-dependent offset induced by the variation of the comparator common-mode voltage.

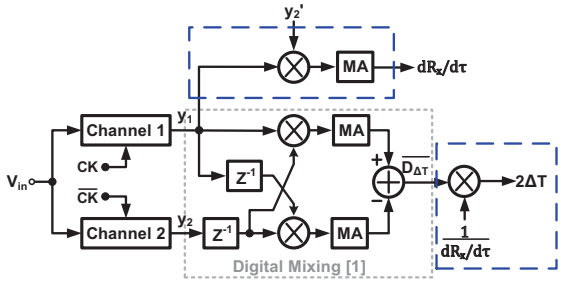

Fig. 2 Proposed timing skew detection block diagram

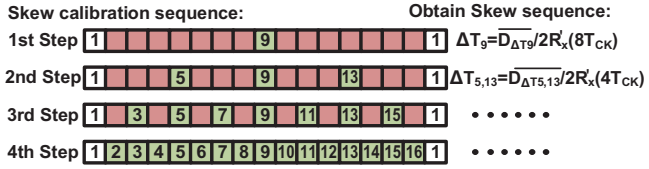

Fig. 3 The calibration sequence in a 16-channel TI-ADC

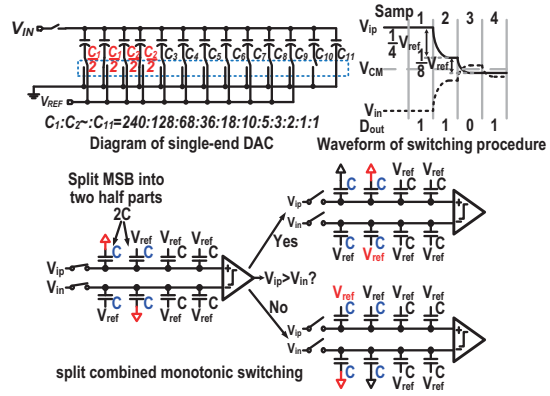

Fig. 4 Circuit implementation of a single-channel SAR ADC

Measurement Results

The 16-way TI-SAR ADC fabricated in 28nm CMOS occupies a core area of 380 ×270μm^2, with Fig. 5(a) presenting the chip micrograph. The SAR logic supply is 0.85V while the analog and clock supply are 1.0V, with total power consumption is 29.0mW (Fig. 5(b)). We implement the mismatch calibration algorithm off-chip. Fig. 6 plots the measured dynamic performance for a 2.38GHz input at 5GS/s, and the largest image tone produced by mismatch is -69.3dB. Fig. 7 shows the measured SNDR with a 2.38GHz input at 5GS/s versus the no. of skew calibration samples. The proposed calibration method improves the SNDR from 43.5 to 48.5dB with only 16k samples for the overall TI-ADC. Fig. 8 displays SNDR versus the input frequency at 5GS/s, with less than 2.5dB variations over the 4GHz bandwidth. The measured SNDR are 48.5dB/47.8dB@fin=2.38GHz/4GHz, respectively. Table I shows the performance summary and a comparison with state-of-the-art TI-ADCs. It achieves at least 5.1x lower FOM$_W$ among ADCs with (f_s>2.8GS/s, SNDR>40dB), as well as 1.9x higher f_s than the closest design with the similar FOM$_W$ (Fig. 9).

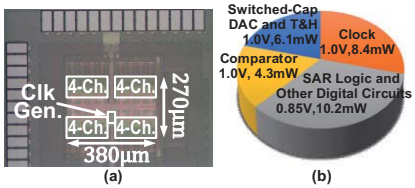

Fig. 5 (a) Chip micrograph (b) power breakdown

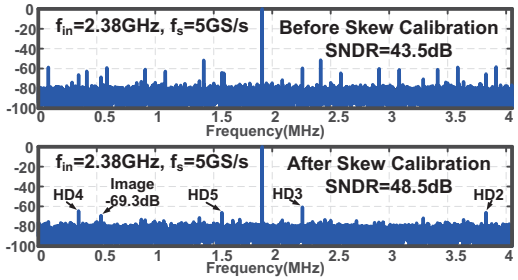

Fig. 6 Measured output spectrum before/after timing skew calibration

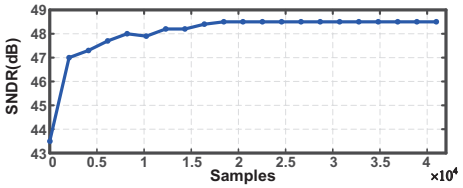

Fig. 7 Measured SNDR versus the samples of timing skew calibration.

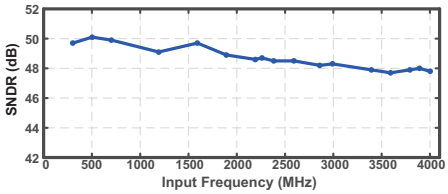

Fig. 8 Measured SNDR at 5GS/s versus input frequency.

Table I Performance summary and comparison with the state-of-the-art

	This Work	ISSCC-15 Brandolini	CICC-15 Fang	ISSCC-16 Lin	ISSCC-17 Keane
Technology	28nm	28nm	28nm	40nm	28nm SOI
Architecture	TI-SAR	TI-Pipe-SAR	TI-SAR	TI-SAR	TI-SAR
Resolution(bit)	10	10	10	10	10
Speed(GS/s)	5.0	5.0	5.0	2.6	8.0
Supply(V)	1.0/0.85	1.8/1.0	1.0	0.95	1.9/1.1/0.9
Power(mw)	29.0	150	76	18.4	300
Area(mm)^2	0.103	0.45	0.57	0.825	0.184
SFDR@Nyq.(dB)	59.6	58	54.4	57.8	60.3
SNDR@Nyq.(dB)	48.5	46.1	41.7	50.6	49.0
SNDR>Nyq.(dB)	47.8@4GHz	N/A	N/A	N/A	N/A
FOM$_W$@Nyq.(fJ-)	26.7	192.5	165	25.6	162.9
FOM$_S$@Nyq.(dB)	157.9	148.1	147.2	159.1	150.2

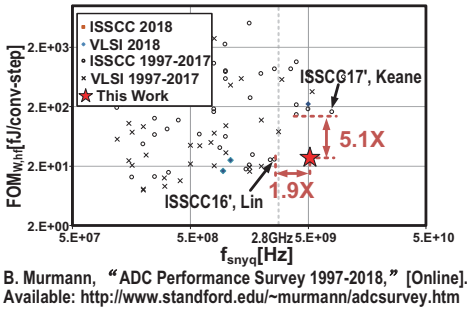

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Fig. 9 Compared to similar works published in ISSCC/VLSI (SNDR>40dB).

References

[1] B. Razavi, *JSSC*, 2013. [2] H. Wei, et al., *JSSC*, 2014. [3] C. Lin, et al., *ISSCC*, 2016. [4] N. L. Dortz, et al., *ISSCC*, 2014. [5] C. Liu, et al. *JSSC*, 2015.