A 1.83 μW, 0.78 μV_{rms} Input Referred Noise Neural Recording Front End

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***Abstract*—This paper describes a neural recording front end for both Local Field Potential (LFP) and Spike Potential (SP) recordings, which range from 0.1 Hz ~ 200 Hz and 200 Hz ~ 10 kHz, respectively. Based on the capacitively-coupled chopper instrumentation amplifier (CCIA) topology, a ripple reduction loop (RRL) is used to suppress the chopping ripple. A DC servo loop (DSL) that utilizes pseudo-feedback to achieve a very small unity gain bandwidth with reduced capacitor size while consuming only 12 nA is proposed. The proposed CCIA is implemented in a standard 0.18 μm CMOS process. Simulation results show that with a total power consumption of 1.525 μA from a 1.2 V supply, a NEF of 2.73 (LFP) and 2.6 (SP) can be achieved.**

I. Introduction

Neurons communicate with each other using electrical signals, which can be classified into Local Field Potential (LFP) and Spike Potential (SP), having a signal bandwidth from 0.1 Hz ~ 200 Hz and 200 Hz ~ 10 kHz, respectively [1]. These neuron communication activities play an important role in various functions, including memory, attention, neurological disorders, and so on. Real-time monitoring of these bio-signals for clinical diagnostics can be accomplished by using implantable neural recording devices. As such portable devices are often powered by either batteries or energy harvesters, the available power budget is quite limited. The main challenge is therefore the design of a low-noise neural interface that can accurately record such weak bio-signals (typically from several microvolts to millivolts) while achieving low-power consumption.

Traditionally, neural recording amplifiers can be implemented by either the current feedback instrumentation amplifier (CFIA) or the CCIA. CFIA requires an input as well as a feedback transconductor, resulting in high power consumption and increased input referred noise. Alternatively, CCIA can achieve better power efficiency and gain accuracy as only one input transconductor is required, being therefore preferred in bio-signal acquisition systems. Due to the use of choppers, ripples at the chopping frequency will appear at the output, which can be effectively suppressed by using a RRL [2].

One major problem in bio-signal acquisitions is the electrode offset that may saturate the neural recording front end. Recently, various bio-signal acquisition amplifiers that employ DSL for electrode offset cancellation have been reported. In [3], a capacitive coupled instrumentation amplifier was proposed for measuring neural field potentials. Although the design achieves good power efficiency, a large capacitor is required to form the DSL high pass corner, occupying a large chip area. The design in [4] overcomes this drawback by employing a very large time constant SC integrator to shape the DSL high pass corner. However, the DSL requires relatively high power consumption, which occupies 15% of the total power. In [5], a tunable pseudo-resistor for DC offset cancellation was proposed, with the tradeoff of increased signal distortion.

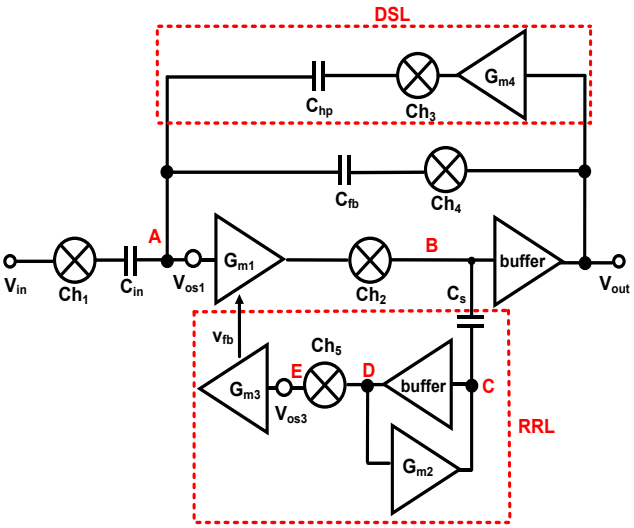

Fig. 1 Structure of the neural recording front end.

This paper describes a low power, low noise neural recording front end that is suitable for both LFP and SP measurements. A CCIA topology is employed for improved power efficiency as well as gain accuracy. A single stage amplifier is utilized to trade off between stability and power consumption. This single stage amplifier achieves larger bandwidth when compared with [4] at the same power budget. A RRL is implemented to suppress the chopping ripple. A DSL utilizing the pseudo-feedback technique is proposed to achieve reduced capacitor size requirement (a high pass corner down to 250 μHz with only a 15 pF capacitor), while having a current consumption of only 12 nA.

II. Topology and Implementation

Fig. 1 shows the structure of the neural recording front end, which consists of a chopped stabilized amplifier, a RRL and a

DSL. Since the input capacitor blocks the DC voltage, this topology can achieve a rail-to-rail input common mode range. The equivalent resistance seen from the chopper and feedback capacitor is $1/(2\pi f_{chop} \cdot C_{fb})$, which directly loads the output of the main amplifier and may imply a large decrease of the DC gain. Thus, a buffer follows the main amplifier to provide isolation between its output and the feedback capacitor load. The detailed analysis of the individual building blocks will be discussed next.

A. Chopped stabilized amplifier

For the main amplifier implementation, a two-stage instrumentation amplifier can be used to achieve the DC gain requirement [4]. The power consumption in the second stage can be minimized to achieve low power. However, this can lead to system instability. As the power consumption in the second stage is negligible when compared with the first stage, the second dominant pole located at the output of the second stage is comparable to the dominant pole at the first stage. It is therefore hard to compensate the amplifier even using a large capacitor (e.g. the design in [4] is still not unity gain stable after using a 30 pF capacitor). Moreover, the use of a large capacitor will limit the bandwidth of the main amplifier. Consequently, a single-stage folded cascade amplifier is utilized to achieve large bandwidth and low power consumption.

The topology of the first amplifier is shown in Fig. 2. PMOS transistors are utilized in the input differential pair for better matching, when compared with their NMOS counterparts. The input pair $M_{1,2}$ is biased in the sub-threshold region to achieve high power efficiency. A large input pair size is critical to reduce flicker noise. $M_{3,4}$ and $M_{9,10}$ should be biased in the saturation region to minimize thermal noise. V_{fb} is the feedback signal from the ripple reduction loop. The output signals are sensed by $M_{11,12}$, which act as the input of the error amplifier and forms a CMFB loop. To avoid signal aliasing, a chopping frequency of 20 kHz, which is twice the bandwidth of SP, has been selected .

B. Ripple Reduction loop

As shown in Fig.1, the ripple reduction loop consists of a capacitor C_s, an active high pass filter (formed by a buffer and G_{m2}), a chopper Ch_5 and G_{m3}. The basic idea is to amplify the AC ripple at the output and feedback it to the main amplifier for ripple cancellation. Offset and flicker noise at node A are first converted to current by G_{m1}, and modulated by Ch_2 to the chopping frequency. The AC current and signal of interest at node B is sensed by the capacitor C_s and converted into voltage at node C, which will subsequently pass through the active high pass filter. Furthermore, the noise and offset voltage will arrive at node D, but, the signal of interest will be blocked by the filter. The AC voltage at node D will be modulated back to DC by Ch_5 to node E. Finally, the DC offset at node E is amplified by G_{m3} and feedback to G_{m1} at the gate of $M_{3,4}$ for ripple reduction.

The original purpose of the RRL is to suppress the AC ripple at the output. However, the RRL also generates ripples

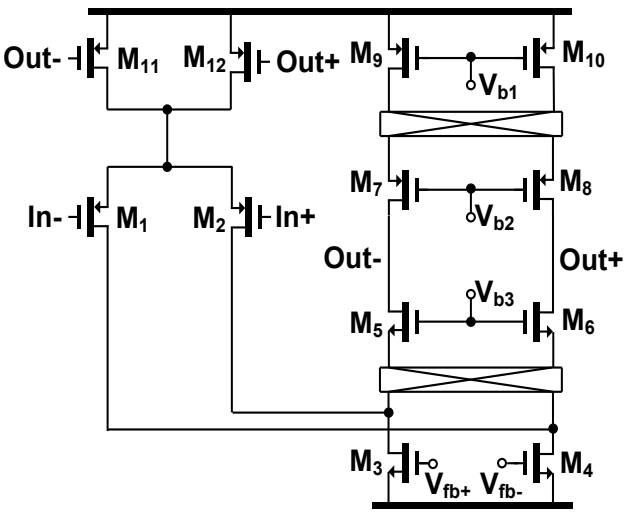

Fig. 2 Chopped stabilized amplifier G_{m1}.

itself that should also be taken into consideration. First, the offset from the buffer and G_{m2} is blocked by the sensing capacitor C_s and will not cause ripple at the output. Second, the offset voltage V_{os3} from G_{m3} is modulated by Ch_5, introducing AC ripple at the output of the amplifier. This output ripple is roughly equal to $\frac{C_p}{Cs} \cdot V_{os3}$, where C_p is the parasitic capacitor at node D. As C_p can be designed (through careful layout) to be much smaller than C_s, the ripple caused by V_{os3} becomes negligible.

C. DC servo loop

The high pass corner frequency f_{hp} is related to the unity gain bandwidth f_{0DSL} of G_{m4}, given by [3]

$$f_{hp} = \frac{C_{hp}}{C_{fb}} \cdot f_{0DSL} \quad (1)$$

As shown in (1), by decreasing the value of f_{0DSL}, the requirement for a large value C_{hp} can be alleviated, thus saving area. In this design, G_{m4} utilizes a pseudo-feedback technique to achieve a very small unity bandwidth. As shown in Fig. 3, G_{m4} is a 4-terminal differential amplifier with the output of the first branch connected back to the input terminal. The second branch, which is identical to the first, is the actual DSL output. In this pseudo-feedback configuration [6], the output of the second branch exhibits the same system level specifications (i.e. gain, bandwidth) as the output of the first. As a result of the unity feedback configuration, the DC gains of both branches are approximately 0dB, because they are identical. However, the output impedance of the second branch is very large due to the open-loop configuration. For the second branch, $f_{3dB}=1/(2\pi R_{out}C)$, which is proportional to the branch current. As a consequence, this current can be designed to be small in order to achieve a very low value of f_{3dB}. On the other hand, the output stage will provide enough gain to suppress the electrode offset. In this design, a second branch current of 12 nA has been allocated, resulting in a high pass corner of 250 μHz at the cost of a 15 pF capacitor.

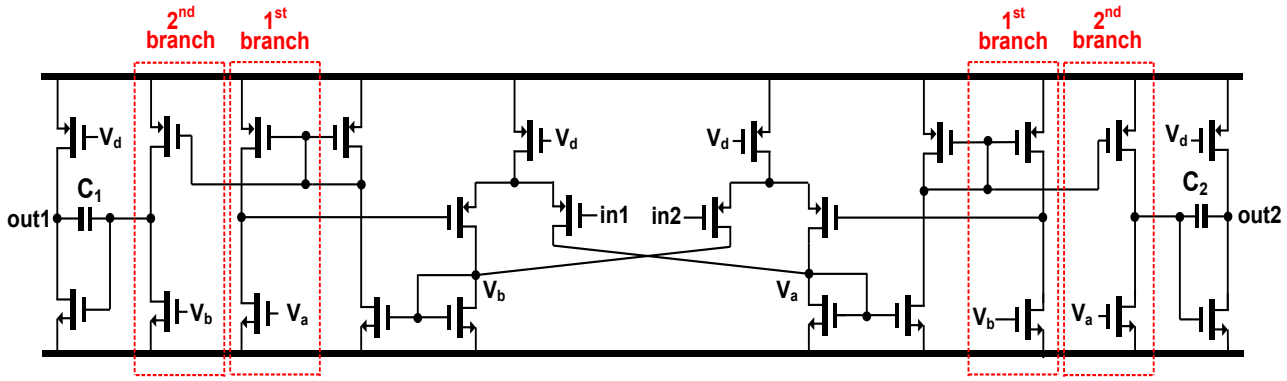

Fig. 3 Implementation of Gm4.

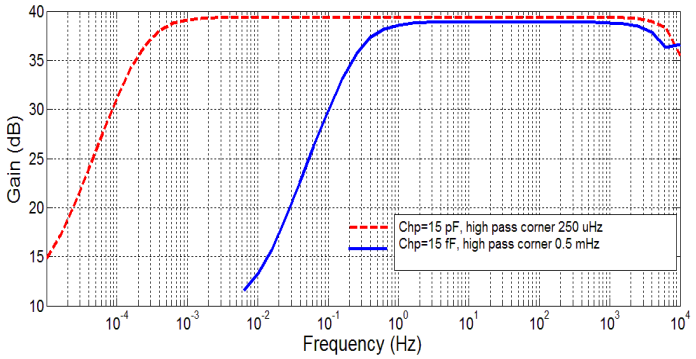

Fig. 4 Simulated AC response of the neural amplifier.

III. Simulation Results

The neural recording front end is designed in a standard 0.18µm 1P6M CMOS process. By using a supply voltage of 1.2V, a differential closed-loop gain of 39.4 dB has been achieved, which is sufficient to amplify a µV signal to meet subsequent ADC resolution requirements which will depend on the SNR and amplitude of the acquired signal. The simulated AC response of this neural recording amplifier is shown in Fig. 4. The high pass corner can be tuned according to different applications. When $C_{1,2}$ are 15 pF, the high pass corner can be moved down to 250 µHz. As a comparison, in order to achieve a high pass corner of around 0.5 Hz, the design in [3] and [4] requires a capacitor of 1 nF and 15 pF, respectively, while our design only requires a 15 fF capacitor.

Fig. 5 shows the output ripple with and without RRL by assuming an input offset of 5 mV for G_{m1}. When RRL is off, the chopping ripple amplitude is -16.81 dB, which may saturate the whole system in ultra-low power supply. When RRL is on, the chopping ripple will be suppressed to -89.94 dB. Fig. 6 shows a Monte Carlo simulation of the magnitude of the first-order harmonic from 100 runs using the same simulation setup (i.e. with an input offset of 5 mV for G_{m1}). It varies from -91.5 dB to -88 dB, which should have a minimal impact on the operation of the neural recording front end.

The simulated input-referred noise with and without DSL is shown in Fig. 7. It is clear that the addition of the DSL mainly impacts on the low frequency noise band. This is due to the very small unity gain bandwidth of G_{m4}. As the thermal noise contributed by the DSL is filtered out by G_{m4}, the overall thermal noise level remains the same. The high flicker noise level

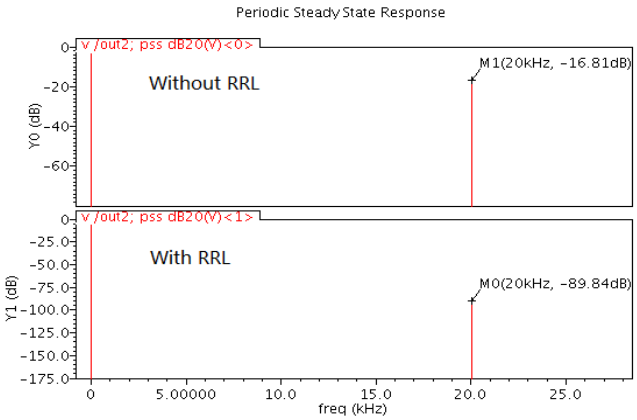

Fig. 5 Simulated output ripple with and without RRL.

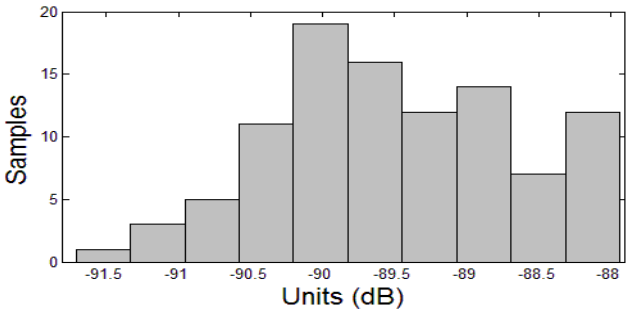

Fig. 6 Monte Carlo simulation of chopping ripple (100 runs).

contributed by the DSL can be solved by allocating less power on G_{m4}, which results in an even smaller unity gain bandwidth.

For LFP (SP) application, the integrated input referred noise from 0.1 Hz to 200 Hz (200 Hz to 10 kHz) is 0.78 μV_{rms} (5.7 μV_{rms}) ; Noise Efficiency Factor (NEF), which is a key figure-of-merit to evaluate different designs, is defined as follows:

$$NEF = V_{ni,rms}\sqrt{\frac{2 \cdot I_{Tot}}{\pi \cdot V_T \cdot 4kT \cdot BW}} \qquad (2)$$

In this work, the total current consumption (including the bias current) is 1.525 µA. According to (2), the corresponding NEF for LFP and SP are 2.73 and 2.6, respectively. Both are comparable with state-of-the-art designs.

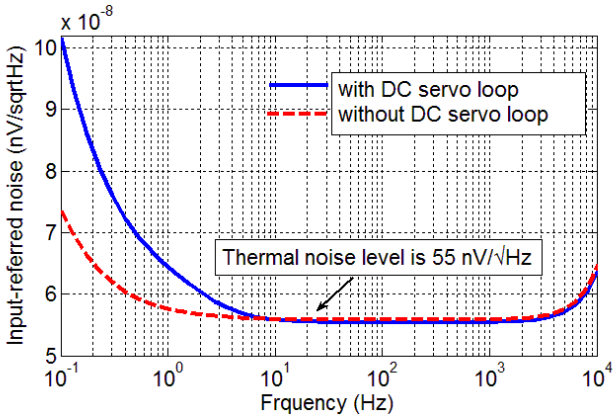

Fig. 7 Simulated input referred noise with and without DC servo loop.

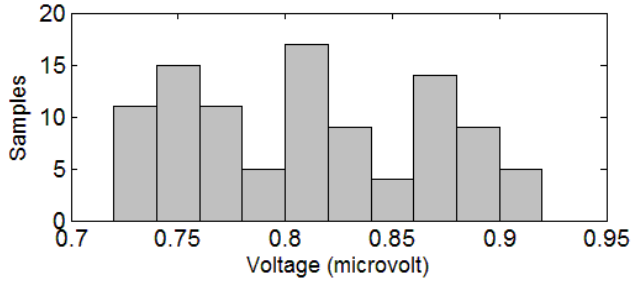

Fig .8 Monte Carlo simulation of integrated noise for LFP application (100 runs).

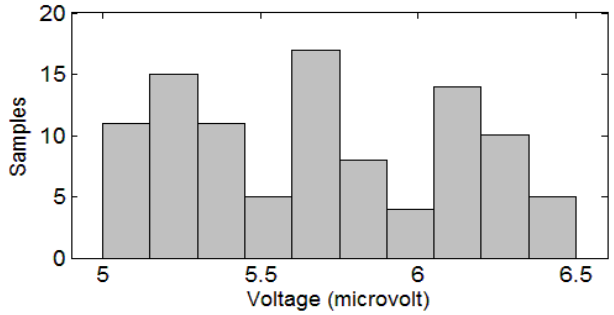

Fig . 9 Monte Carlo simulation of integrated noise for SP application (100 runs).

Fig. 8 and Fig. 9 present the Monte Carlo integrated input referred noise simulations for LFP and SP applications from 100 samples. It can be seen that the integrated input referred noise ranges from 0.72 μV_{rms} to 0.92 μV_{rms} for LFP application, yielding a NEF from 2.52 to 3.22. For SP applications, the integrated input referred noise ranges from 5 μV_{rms} to 6.4 μV_{rms}, corresponding to a NEF from 2.28 to 2.9.

Table I shows the comparison of different acquisition front ends published in recent years. This work achieves a designed bandwidth of 7.5 kHz while only consuming 1.525 µA of current. The input referred thermal noise density is about 55 nV√Hz. This work achieves a competitive NEF performance when compared with other state-of-the-art designs.

TABLE I. COMPARISON OF DIFFERENT ACQUISITION FRONT ENDS

Parameter	[4]	[7]*	[1]	This work*
Tech.	65 nm	0.13 µm	0.35 µm	0.18 µm
Supply (V)	1	1.2	3.3	1.2
Current (µA)	2.1	0.902	12.1	1.525
Bandwidth (Hz)	100	337	10k	7.5k
Input-referred noise(nV/√Hz)	60	64.9	32.9	55
NEF	3.3	4.1	4.5 for LFP (0.1-200Hz) 7.6 for SP (200-10kHz)	2.73 for LFP (0.1-200Hz) 2.6 for SP (200-10kHz)
Unity Gain Stable	No	Yes	Yes	Yes

* Simulation results

IV. CONCLUSIONS

A neural acquisition front end suitable for LPF and SP acquisition is presented. A CCIA using RRL for ripple reduction and DSL with pseudo-feedback for improved power and area efficiencies is proposed and designed in a standard 0.18µm CMOS process. Simulation results show that with a total current consumption of 1.525 µA, from a 1.2 V supply, NEF values of 2.73 (LFP) and 2.6 (SP) can be achieved.

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