A 5.35 mW 10 MHz Bandwidth CT Third-Order ΔΣ Modulator with Single Opamp Achieving 79.6/84.5 dB SNDR/DR in 65 nm CMOS

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***Abstract* - This paper presents a power-efficient single-loop continuous-time (CT) third-order sigma delta (ΔΣ) modulator that achieves a SNDR of 79.6 dB over a 10 MHz signal bandwidth. The modulator uses a feedforward-feedback (CIFF-FB) architecture which incorporates a single amplifier biquad (SAB) and a passive integrator to realize a third-order noise shaping. We also propose a continuous-time complementary (CTC) approach for the amplifier to improve the power efficiency. To alleviate the switch driver mismatch and jitter, we introduce an adaptive latch in the DAC driver. The modulator operates at a sampling rate of 640 MHz and consumes 5.35 mW from 1.2 V and 1.8 V power supplies. It achieves a DR of 84.5 dB and a SNDR of 79.6 dB with 10 MHz signal bandwidth, resulting in a Schreier FOM of 172.3 dB or 177.2 dB based on SNDR or DR, respectively.**

I. INTRODUCTION

The increasing call for a low power CT ΔΣ modulator in high-resolution and wideband applications imposes a considerable research effort in the design of optimized structures. Although a CT ΔΣ modulator benefits from both power efficiency and anti-alias filtering when compared with its discrete-time counterpart, it remains a challenge to target for high energy efficiency due to the power hungry integrators.

Conventional loop filters of CT ΔΣ modulators are often implemented with active integrators, such as active-RC and Gm-C. An N-order filter needs a number of N active integrators which not only leads to a large power and area but also increases design complexity. As shown in the power breakdown of several designs [1] [2], the amplifiers typically occupy around 40% of the total power consumption, where the 1st amplifier consumes ~20% determined by the thermal noise requirement of the modulator. Other amplifiers use the remaining 20% due to noise and driving capability requirements. Consequently, the amplifiers in the integrators become the modulator's bottleneck towards a better energy efficiency. Besides, the finite gain-bandwidth (GBW) of the amplifiers causes phase delay where the series connection of multiple amplifiers leads to a large phase shift, causing instability in the modulator [3].

To reduce the number of amplifiers in the loop filter, a noise-coupling (NC) technique for CT ΔΣ modulators was reported in [4], which is suitable for the modulators with an SAR ADC as the multi-bit quantizer. Noise-shaping quantizers, such as the voltage-controlled oscillator (VCO) quantizer [5], the noise-shaped integrating quantizer (NSIQ) [6], and the incorporation of both the VCO and the NSIQ [7] are also other possible alternatives. However, the bandwidth in [4], [6] and [7] is limited either by the speed of the SAR or the NSIQ quantizers, whereas the linearity of the VCO limits the input swing of the quantizer.

This paper proposes a third-order CT ΔΣ modulator with only one amplifier in the loop filter, achieved by incorporating a SAB and a passive integrator. The passive integrator also facilitates the excess loop delay (ELD) compensation without the active adder. We present a CTC approach and an adaptive latch to further improve the efficiency of the modulator. The prototype, fabricated in 65 nm CMOS, exhibits 79.6 dB signal-to-noise and distortion ratio (SNDR) and 84.5 dB dynamic range (DR) over a 10 MHz bandwidth, consuming only 5.35 mW. The Schreier figure-of-merit (FOM) is 172.3 dB or 177.2 dB based on SNDR or DR, respectively.

II. PROPOSED CT ΔΣ ADC ARCHITECTURE

Fig. 1 depicts the proposed CT CIFF-FB ΔΣ modulator topology with a 4-bit quantizer. We obtain the first and second integrators, as well as the feedforward path, with an improved version of SAB integrator. On the other hand, the last integrator

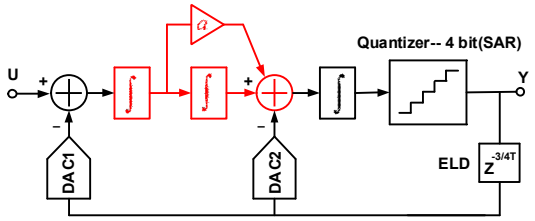

Fig.1. Proposed CT ΔΣ Modulator architecture.

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is passive to save power. The SAR architecture is utilized in the multi-bit quantizer due to its outstanding efficiency and to avoid handling the mismatch from multiple comparators. DAC1 is the main feedback DAC and DAC2 compensates the ELD introduced by the quantizer and feedback path. This design implements a 3rd-order CT $\Delta\sum$ modulator with only one amplifier and 4-bit quantizer which results in an ADC with 79.6 dB SNDR and 10 MHz bandwidth. The sampling frequency is 640 MHz with an oversampling ratio (OSR) of 32 leading to a signal-to-quantization noise ratio (SQNR) of 99 dB. In this design with an 80 dB targeting SNR, we reserve a margin around 17 dB SQNR for other noise sources, such as the thermal noise, DAC mismatch and CLK jitter.

III. Implementation

A. Modulator

Fig. 2 shows the block diagram of the CT $\Delta\sum$ modulator. It achieves a 3rd-order noise-shaping by incorporating a SAB and a passive integrator, which allow single opamp implementation for low power and low design complexity. Besides, the passive integrator enables ELD compensation without the active adder. The only overheads are the DAC2 and its digital driving buffers which are relatively small as the error in the DAC2 can be attenuated by the 2nd-order noise shaping.

The main noise contributor of this design is the thermal noise of the input resistor (R1) as it cannot be shaped. Nevertheless, the current of the DAC and the capacitor load are determined by R1, implying that its value induces a tradeoff between the noise budget and power of the DAC and the opamp. We choose R1 to be 1k Ω to balance such tradeoff for the target specifications. In [2] and [3], a feedback resistor is introduced to improve the SQNR by optimizing the zero in the NTF, but its induced non-shapeable thermal noise indeed yields a diminishing return on the overall SNDR. Our SAB integrator removes the feedback resistor in the RC biquad which alleviates a non-shapeable noise source thus improving the overall SNDR of the modulator.

Even though the passive integrator does not induce significant inband noise, it imposes that the transfer function (TF) of the loop filter is non-ideal which can be shown by the follow TF of the modulator:

$$H(s)=\left(\underbrace{\frac{\frac{1}{R_1C_1}s+\frac{1}{R_1R_2C_1C_2}}{s^2}}_{1^{st}\ \text{term}}+k_{DAC2}\right)\times\frac{\frac{R_4}{R_3+R_4}s+\frac{1}{C_3(R_3+R_4)}}{s+\frac{1}{C_7(R_3+R_4)}} \quad (1)$$

where k_{DAC2} is the feedback coefficient of the DAC2 used to compensate the ELD. Further, the passive filter moves the pole to $p=1/C_7(R_3+R_4)$. It changes the NTF of the modulator and causes the SQNR to drop from 106 to 99 dB based on the simulations, and since we are targeting for a value around 80 dB, such influence is negligible. Nevertheless, the non-idealities of the SAB integrator greatly affect the performance of the modulator since they do not experience any noise-shaping effect. Its design considerations and non-ideal errors will be discussed next.

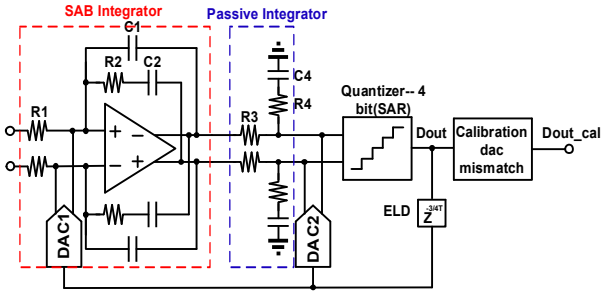

Fig.2. Block diagram of the proposed 3th-order $\Delta\sum$ ADC.

B. The load of SAB

In the SAB integrator, we introduce an extra RC network (R2 and C2) to realize a 2nd-order denominator with an extra zero in the 1st term of (1), which induces extra load to the amplifier when compared with a standard approach. The load of the SAB integrator can be analyzed by its equivalent impedance in the s-domain as:

$$Load=\frac{1}{Z_L}=sC_1+\frac{1}{R_2+\frac{1}{sC_2}}. \quad (2)$$

Obviously, the load is inversely proportional to R2 and directly proportional to C2. The extra load induced by R2 and C2 will become significant with a small R2 or a large C2. Here, the R2 is about 600 Ω, and both C1 and C2 are about 3 pF. Based on (2), the C_2-R_2 loop only increases the load by 2.7% at f_S which is a very small overhead in the modulator.

C. Finite opamp bandwidth in the loop filter

Unlike the conventional integrator, the finite *GBW* in the SAB integrator not only introduces a gain error and an additional pole [8], but also moves the poles from the origin to the left-half plane on the s-domain. The TF of the SAB integrator under the influence of the finite *GBW* can be expressed as:

$$H_{SAB}(s)=\frac{\frac{1}{CR_1}s+\frac{1}{C^2R_1R_2}}{s^2+\frac{s}{GBW}\left(s^2+\left(\frac{2}{CR_2}+\frac{1}{CR_1}\right)s+\frac{1}{C^2R_1R_2}\right)}. \quad (3)$$

Based on (3), Fig. 3 (a) and (b) plot the pole/zero map and the NTF, respectively, to analyze the influence of the finite *GBW* in the opamp. With the decrease of the *GBW*, the location of the zero is pushed away from DC and the poles are placed at a lower frequency which worsens the inband attenuation of the modulator. Moreover, the NTF only experiences a little deviation when the *GBW* is above 1.5 f_S, implying that the improvement of the inband attenuation is almost saturated. Based on the model from (3), when the *GBW* increases from 0.5 to 1.5 f_S, the SQNR improves by 13 dB. Plus, when the *GBW* is larger than 1.5 f_S, the improvements stay around only 2-3 dB. Such tradeoff between the GBW and SQNR is also similar in

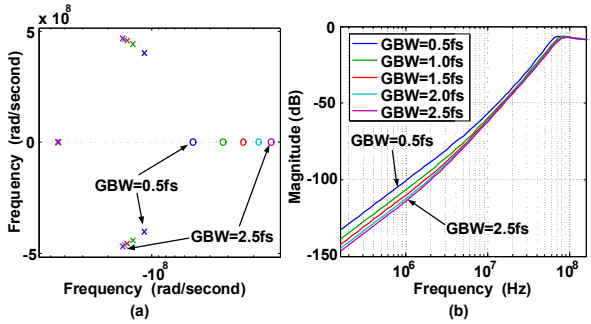

Fig.3. (a) NTF and (b) pole-zero plot for different amplifier's bandwidths.

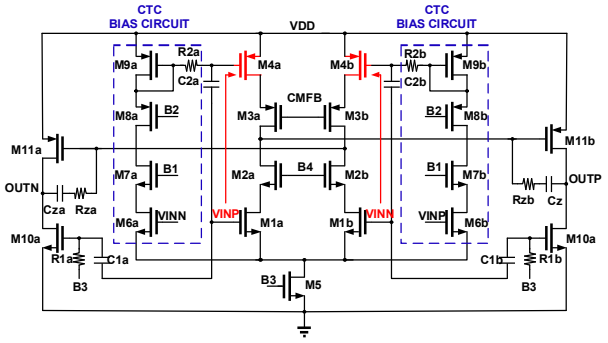

Fig.4. Two-stage CTC feed-forward amplifier.

the conventional integrator [8] which indicates that our SAB integrator does not induce extra burden on the 1st opamp. Consequently, we select a GBW of 1.5 f_S for a good energy efficiency and design margin.

D. Op-Amp

Fig. 4 shows the circuit-level schematic of the proposed CTC amplifier utilized in the SAB integrator. A two-stage topology, feed-forward path and Miller frequency compensation is adopted to improve the power efficiency. In [9], the complementary switched-capacitor technique is presented to double the g_m of the 1st stage based on a discrete-time operation. However, it is not applicable in the CT domain. As if M4a, b is supported by a DC biasing resistor, it introduces a pole-zero doublet, leading to a 6 dB loss before the zero location. In this amplifier, we introduce a CTC biasing circuit to place the zero close to the pole for cancelling the effect of the pole-zero doublet and avoiding gain loss, which only consumes about 1/35 of the power of the amplifier. Simulations show that the CTC structure can double the g_m of the 1st stage and improve the open loop gain by 6 dB. The amplifier consumes 1.6 mW at 1.2 V and achieves a 72 dB DC gain with a 1.5 f_S GBW.

E. DAC driver and feedback timing

We adopt a current steering DAC with a 1.8V power supply to obtain good noise and PSRR performances. The switch driver mismatch and jitter caused by the DAC driver directly affect the SNDR of the modulator without any attenuation. Such issues are critical in wideband designs because of their high sampling frequency. In order to alleviate these influences, the number of devices in the feedback path should be minimized. Fig. 5 shows the proposed adaptive latches in the DAC driver and the feedback timing of the DAC. Unlike other DAC drivers [1], [10], the one now proposed propagates the logic feedback without involving the latch operation. During the critical signal propagation (CLKd=0), the latch is disconnected from the feedback path and the CLK signal enables the propagation after the LSB decision from the quantizer is ready. The latch circuit resumes at CLKd=1 after the feedback is at a steady stage. The DAC control signals (Q_{nP}-Q_P and Q_{nN}-Q_N) have a high and a low cross point, respectively, which are adjusted through the sizing ratio of PMOS and NMOS in the transmission gate (TGF). They are optimized

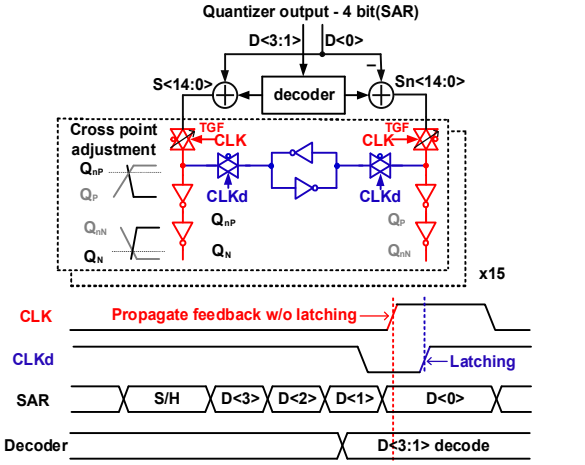

Fig.5. Adaptive latch in the DAC driver and feedback timing.

separately to avoid the DAC dynamic error induced by glitches at the rising edge of the CLK signal. With only three gates and no latch in the critical path, simulations indicate that the mismatch and jitter from the switch driver are reduced by 75%, 50% when compared with [1] or [10], respectively, with only 2/3 of power consumption in the latch.

Since we adopt the SAR quantizer in the design, it leads to a relatively long conversion time and metastability issue. In this design, we ensure a low error probability by assigning enough time for the comparator regeneration. Besides, its outputs need to be decoded from the binary to the thermometer to avoid inter-symbol-interference (ISI) in the feedback DACs. These imply that the feedback timing is very critical. In order to reduce the decoding time, we decode the SAR output D<1:3> in advance, and LSB D<0> directly feeds to the DAC without any decoding.

IV. Measurement Results

The prototype, fabricated in 65 nm CMOS, has an active area of 0.033 mm^2 as illustrated by the die photo from Fig. 6. The modulator is clocked at 640 MHz and its signal bandwidth is 10 MHz with an OSR of 32. Fig. 7 shows the output spectrums of the modulator for a single-tone signal at a frequency of 1.4 MHz. The measured SNDR and SNR improve from 54.2 dB to 79.6

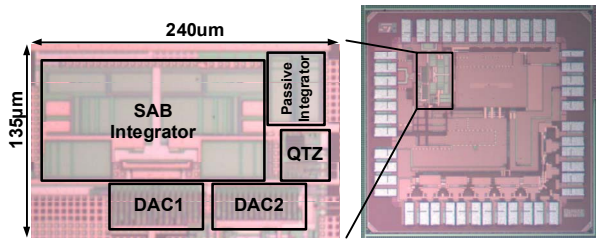

Fig.6. Die photograph.

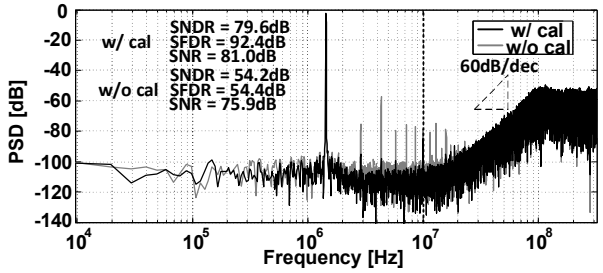

Fig.7. Measured single-ton FFT spectrum.

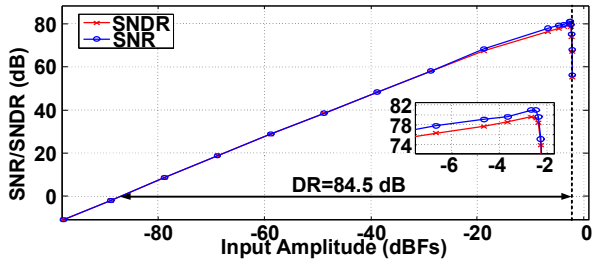

Fig.8.Measured SNDR and SNR vs. input amplitude.

dB and 75.9 dB to 81 dB with DAC mismatch calibration [11], respectively. The spurious-free dynamic range (SFDR) of 92.4 dB is dominated by the 2nd harmonic caused by the mismatch between the different current mirrors of the differential DAC. This error may also be stimulated by unsymmetrical coupling from the input, clock and output signals to the bias of the differential DAC. The 60 dB/decade spectral slope validates the 3rd-order noise-shaping by using the SAB and the passive integrator.

Fig. 8 shows the SNR and SNDR vs. input amplitude at 1.4 MHz which confirms that the proposed design achieves a DR of 84.5 dB. The total power consumption is 5.35 mW including 3.43 mW and 1.92 mW from analog and digital, respectively. The analog part includes the amplifier, DAC and comparator, and the digital part includes the logic buffer, SAR logic, DAC driver and CLK generator. TABLE I summarizes the measured performance of this work and compares it with the state-of-art CT ΔΣ designs with similar BW. The good power efficiency is benefited from the single amplifier modulator, the CTC approach and the adaptive latch DAC driver.

V. Conclusions

This paper presented a power-efficient CT ΔΣ modulator by incorporating a SAB and a passive integrator. It facilitates a small area and power efficient modulator architecture with single amplifier. The SAB realizes a 2nd-order integrator which provides 40 dB/decade slopes with little power overhead. The passive integrator implements 20 dB/decade slopes and enables ELD compensation without active adder. Moreover, to improve the power efficiency of the amplifier and address the jitter and switch driver mismatch in the DAC drivers, we proposed a CTC amplifier and an adaptive latch circuit, respectively. These techniques implemented in a CT ΔΣ modulator achieve a SNDR of 79.6 dB and a Schreier FOM of 172.3 dB with 10 MHz signal bandwidth.

TABLE I. SUMMARY OF PERFORMANCE AND BENCHMARK WITH STATE-OF-THE-ART

	T.Kim ISSCC 2017	T.Kim VLSI 2015	B.N ISSCC 2016	Y.Shu ISSCC 2013	G.Wei VLSI 2015	This work
Area (mm^2)	0.17	0.08	0.027	0.08	0.066	0.033
Technology (nm)	130	130	65	28	28	65
Supply Voltage (V)	1.2	1.2	1.0	1.2/1.5	0.9/1.8	1.2/1.8
Fs (MHz)	640	640	1000	640	432	640
Bandwidth (MHz)	15	10	10	18	5	10
Power (mW)	11.4	7.19	1.57	3.9	3.16	5.35
Peak SNDR (dB)	80.4	75.3	72.2	73.6	80.5	79.6
DR (dB)	82.9	78.5	77	78.1	83.9	84.5
FOMSch/SNDR (dB)	171.6	166.7	170.2	170.2	172.5	172.3
FOMSch/DR (dB)	174.1	169.9	172.0	174.7	175.9	177.2
FoMWa (fJ/conv.step)	44.1	75.9	23.6	27.7	36.5	36.5

References

[1] C. Y. Ho, et al., "A 4.5 mW CT Self-Coupled ΔΣ Modulator With 2.2 MHz BW and 90.4 dB SNDR Using Residual ELD Compensation," in *IEEE JSSC*, vol. 50, no. 12, pp. 2870-2879, Dec. 2015.

[2] L. Breems *et al*., "A 2.2 GHz Continuous-Time ΔΣ ADC With −102 dBc THD and 25 MHz Bandwidth," in *IEEE JSSC*, vol. 51, no. 12, pp. 2906-2916, Dec. 2016.

[3] R. Zanbaghi, et al., "An 80-dB DR, 7.2-MHz Bandwidth Single Opamp Biquad Based CT Delta Sigma Modulator Dissipating 13.7-mW," in *IEEE JSSC*, vol. 48, no. 2, pp. 487-501, Feb. 2013.

[4] B. Wu, et al., "15.1 A 24.7mW 45MHz-BW 75.3dB-SNDR SAR-assisted CT ΔΣ modulator with 2nd-order noise coupling in 65nm CMOS," in *IEEE ISSCC*, pp. 270-271, Feb. 2016.

[5] K. Reddy et al., "A 16-mW 78-dB SNDR 10-MHz BW CT ΔΣ ADC Using Residue-Cancelling VCO-Based Quantizer," in *IEEE JSSC*, vol. 47, no. 12, pp. 2916-2927, Dec. 2012.

[6] N. Maghari et al., "A Third-Order DT ΔΣ Modulator Using Noise-Shaped Bi-Directional Single-Slope Quantizer," in *IEEE JSSC*, vol. 46, no. 12, pp. 2882-2891, Dec. 2011.

[7] T. Kim, et al., "28.2 An 11.4mW 80.4dB-SNDR 15MHz-BW CT delta-sigma modulator using 6b double-noise-shaped quantizer," in *IEEE ISSCC*, pp. 468-469, 2017.

[8] F. Gerfers, et al., "A 1.5-V 12-bit power-efficient continuous-time third-order ΔΣ modulator," in *IEEE JSSC*, vol. 38, no. 8, pp. 1343-1352, Aug. 2003.

[9] J. Wu et al., "A 5.4GS/s 12b 500mW pipeline ADC in 28nm CMOS," in IEEE *VLSI*, pp. C92-C93, Jun. 2013.

[10] C. H. Lin et al., "A 12 bit 2.9 GS/s DAC With IM3 ≪ -60 dBc Beyond 1 GHz in 65 nm CMOS," in *IEEE JSSC*, vol. 44, no. 12, pp. 3285-3293, Dec. 2009.

[11] M. Bock et al., "Calibration of DAC Mismatch Errors in ΣΔ ADCs Based on a Sine-Wave Measurement," in *IEEE TCAS. II*, vol. 60, no. 9, pp. 567-571, Sep. 2013.