A 6.78 MHz Active Voltage Doubler with Near-Optimal On/Off Delay Compensation for Wireless Power Transfer Systems

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***Abstract*—This paper presents a fully integrated 6.78 MHz active voltage doubler with a near-optimal on/off delay compensation scheme, achieving the maximized AC to DC power conversion efficiency (PCE) and voltage conversion ratio (VCR) for implantable medical devices (IMDs). In the proposed active voltage doubler design, we build sampling-based feedback loops for the real-time active diode on/off delay compensation. The proposed active voltage doubler was designed with a standard CMOS 0.35 µm process. It achieves a peak PCE of 92.2% with a 500 Ω load, and a peak VCR of 1.92 with a 2 kΩ load, improved by 10% and 33%, respectively, when compared with the voltage doubler without the delay compensation scheme. The input range of this design is from 1 V to 1.7 V with a load range from 200 Ω to 2 kΩ.**

Keywords—voltage doubler; wireless power transfer; implantable medical devices; feedback loop; real time; delay compensation

I. INTRODUCTION

Wireless power transfer (WPT) is widely used to eliminate the bulky batteries or to reduce the size of the battery in implantable medical devices (IMDs), such as the brain-machine interfaces (BMI), the cochlear implant, and the retinal prosthesis [1-2]. In these applications, high power conversion efficiency (PCE) of the WPT receiver (RX) is very important to prevent the tissue surrounding the IMDs from the potential temperature increase due to power losses. Due to the coupling coefficient k variation between the power transmitter (TX) and the RX, the voltage received by the RX varies. Thus, active rectifiers were commonly used to cater for the low voltage operation [3-6]. To obtain a higher voltage and ensure the proper operation of IMDs, high voltage conversion ratio (VCR) is also favorable. Therefore, an active voltage doubler with low voltage drop could be more suitable than an active rectifier in certain cases, for example, under loosely coupled conditions and/or low power scenarios [7-11]. In addition, the equivalent input impedance of the active voltage doubler ideally is only 1/4 of that of the active rectifier, and thus is closer to the peak efficiency optimum load resistance point, R_{OPT}, of the power link, considering that the equivalent impedance of the IMD is much larger than R_{OPT}. Therefore, active voltage doubler has advantages over the active rectifier in the terms of VCR and power link efficiency for IMDs.

Fig. 1 shows the block diagram of a typical biomedical WPT system with an active voltage doubler. The inductively coupled wireless power link consists of a series-resonant tank L_1C_1 on the primary side and a parallel-resonant tank L_2C_2 on the secondary side. The unregulated AC voltages V_{AC1} and V_{AC2} received by the secondary side are rectified and doubled by the voltage doubler to a DC voltage V_{OUT}. Then, it is regulated to supply the functional implantable device.

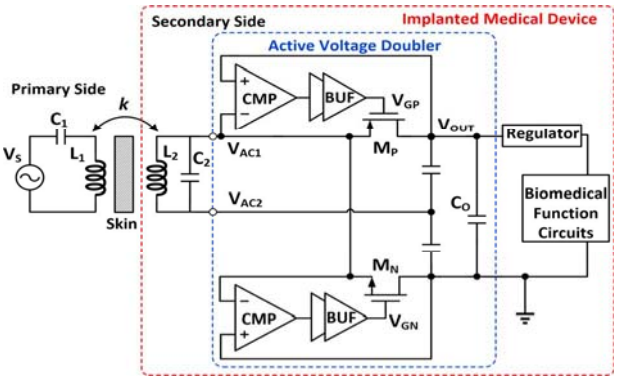

FIGURE 1. A typical biomedical WPT system with an active voltage doubler.

In the active voltage doubler, the power transistors are turned on/off by a dedicated buffered comparator, forming the active diodes. Due to the circuit delays introduced by the comparators and the buffers, the problems of reverse current and reduced conduction time will occur for the active diodes, both of which degrade the PCE and VCR.

To compensate the circuit delays, several offset-control schemes have been proposed for the active rectifiers [3-6] and the active voltage doublers [7]. In [3-4], a fixed offset was introduced to the comparators to compensate the delay. However, as the delays caused by comparators and drivers are very sensitive to PVT and load variations [6], the circuit delays cannot be accurately compensated. A switched-offset biasing scheme proposed in [5] successfully improves the compensation accuracy over a wide input voltage range. However, the compensation accuracy is highly dependent on the accuracy of the process models and is still sensitive to the process, temperature and load variations. In [6], sampling based negative feedback loops were introduced to the active rectifiers, which compensate for both the on and off delays, thus making the compensation accuracy insensitive to the PVT and load variations. However, the accuracy of the sample-and-hold (S/H) circuits used in [6] is low due to the charge injection effect of the switches, which degrades the accuracy of the on-/off-delay compensation. For the active voltage doubler, only the open-loop comparator offset-control scheme similar to [4] was proposed in [7], which suffers from the PVT variations.

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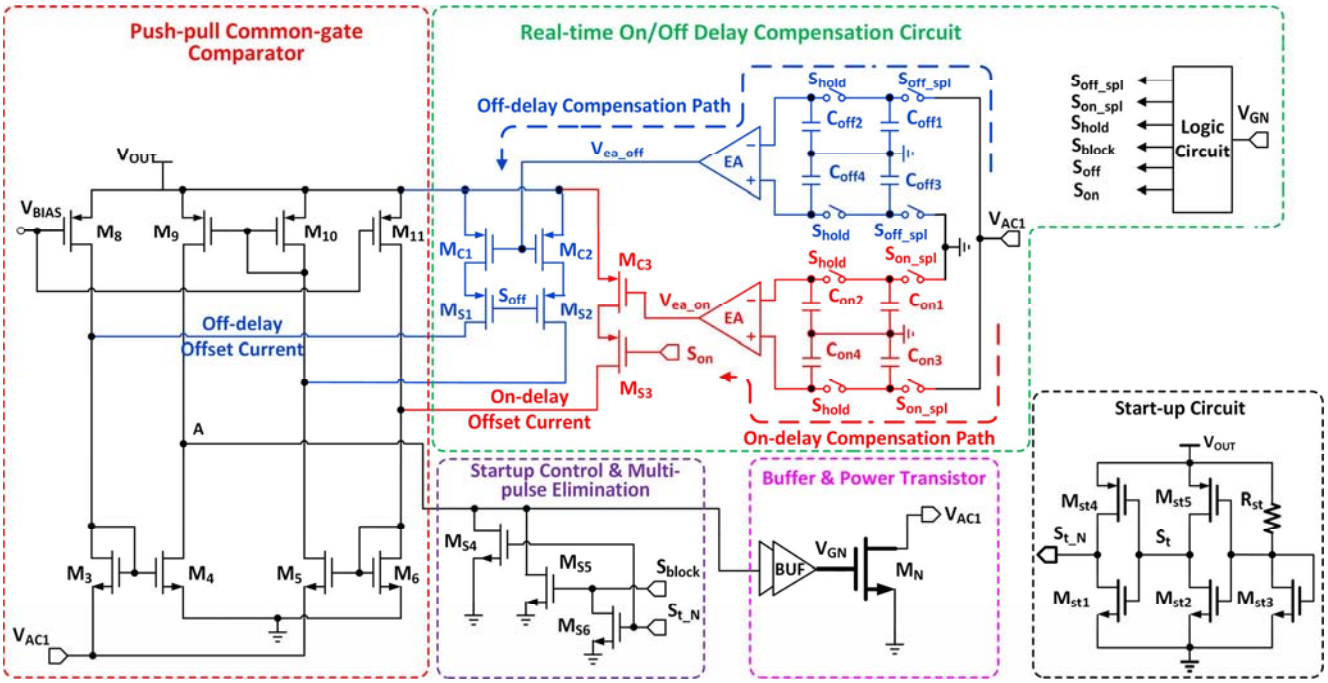

FIGURE 2. Schematic of the NMOS active diode with the real-time on/off delay compensation technique.

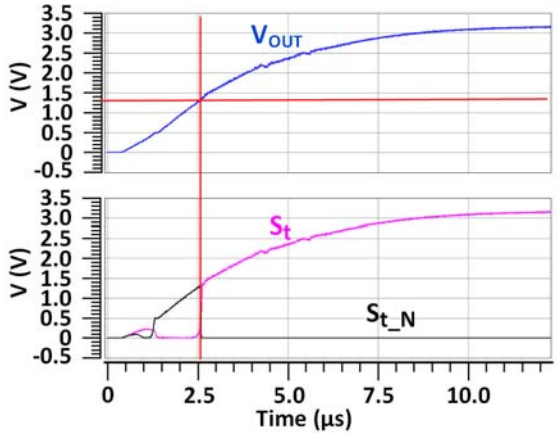

FIGURE 3. Simulated waveforms of the start-up circuit.

To achieve high VCR and PCE, here we design an active voltage doubler delay-compensation scheme with four negative-feedback loops, reducing the circuit delays to be zero and being insensitive to the PVT and load variations.

In this paper, we have designed an active voltage doubler with a real-time on/off delay -compensation technique for both NMOS and PMOS active diodes. Each comparator is equipped with two feedback loops providing proper offset currents to compensate the on/off delays under different PVT and load conditions. In our work, a differential sample-and-hold (S/H) circuit is adopted to improve the compensation accuracy. In addition, a start-up circuit is added to guarantee the active voltage doubler a smooth start-up. Section II introduces the proposed voltage doubler in detail. Simulation results are provided in Section III. Finally, Section IV draws the conclusions.

II. DESIGN OF THE PROPOSED ACTIVE VOLTAGE DOUBLER

A. Real-Time On/Off Delay Compensation Technique

Fig. 2 shows the detailed schematic of the NMOS active diode with the real-time on/off delay compensation technique. The active diode consists of a conventional active diode (which includes the push-pull common-gate comparator, the buffer and the power transistor M_N), a start-up circuit, and an additional real-time on/off delay compensation circuit. In the active diode, we use two separate feedback loops to generate accurate on/off offset current for reverse current control. Considering, as an example, the off-delay compensation at the falling edge of V_{GN}, S_{off_spl} turns on and V_{AC1} and ground are differentially sampled by C_{off1} and C_{off3}. Then, both sampled voltages pass to C_{off2} and C_{off4}, respectively, when S_{hold} is on. If M_N turns off too late/early which means V_{AC1} is larger/smaller than ground-level, V_{ea_off} will be decreased/increased to provide more/less off-delay offset current to turn off M_N earlier/later. With this negative feedback, the sampled V_{AC1} will finally be pulled to be equal to ground, which indicates that M_N turned off at an optimal timing. The same mechanism can be applied to the on-delay compensation as well. The on/off delay offset current is switched on/off according to V_{GN}. When V_{GN} is low, only the on-delay offset current turns on (S_{on} = "0" and S_{off} = "1") and when V_{GN} is high only the off-delay offset current is on (S_{on} = "1" and S_{off} = "0"). To eliminate the multi-pulsing problem, we apply S_{block} to the gate of M_{S5}. With a short duration right after V_{GN} becomes low, S_{block} goes high and shorts V_{GN} to ground, assuring that M_N only switches once per cycle. The schematic and the working principle of both PMOS and CMOS active diodes are similar.

B. Self-Startup Capability

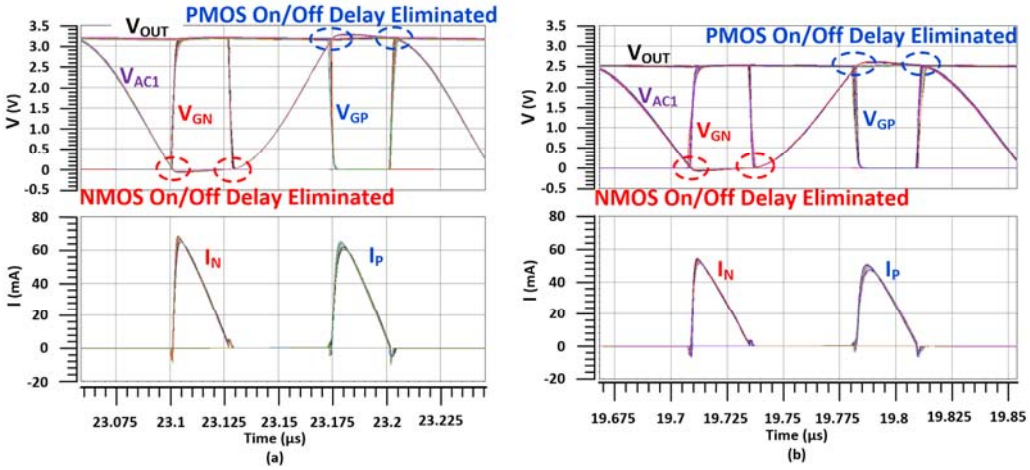

FIGURE 4. PVT corner simulation results at (a) V_{OUT} = 3.1 V and (b) V_{OUT} = 2.5 V.

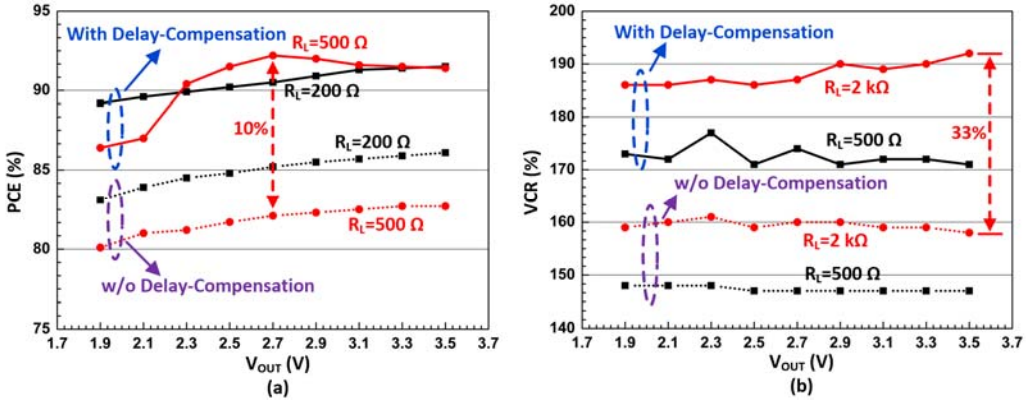

FIGURE 5. Simulated (a) PCE and (b) VCR under different V_{OUT}.

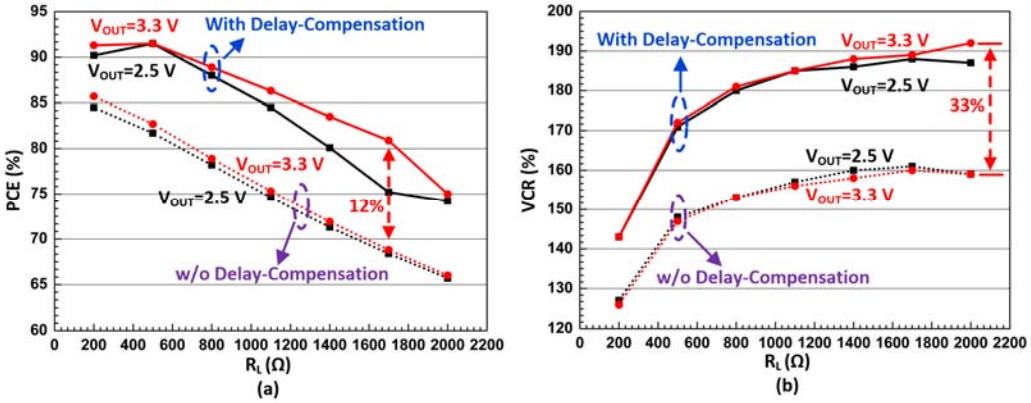

FIGURE 6. Simulated (a) PCE and (b) VCR under different R_L.

Since V_{OUT} supplies the comparators and logic control circuits, we add a start-up circuit to ensure that the output capacitor Co can be charged up to the level needed for the comparators and logic control circuits to work [12]. As shown in Fig. 2, when $V_{OUT} < V_{thp} + V_{thn}$, S_t = "0" and S_{t_N} = "1". Thus, the gate of M_N connects directly to the ground. As a result, M_N operates as a diode-connected transistor. With a similar principle, the PMOS power transistor is also diode-connected. Then output capacitor Co charges up. At the same time, M_{S5} is forced to turn off. When $V_{OUT} > V_{thp} + V_{thn}$, S_t become s "1" and the active voltage doubler starts to work normally. Fig. 3 shows the waveforms of V_{OUT}, S_t and S_{t_N} during the start-up process with a load resistor of 500 Ω.

III. SIMULATION RESULTS

This section shows the simulated results of the proposed active voltage doubler obtained with a standard CMOS 0.35 μm process under different load resistances and output voltages.

Fig. 4 shows the waveforms under different process corners and temperature (0 °C, 27 °C and 85 °C) conditions with a load resistor of 500 Ω. There, we observe the elimination of the on/off delay of both the power NMOS and PMOS when $V_{OUT} \approx 3.1$ V or $V_{OUT} \approx 2.5$ V. As shown in Fig. 5(a), the PCEs with delay compensation are higher than 86% over the whole output voltage range when R_L = 200 Ω or 500 Ω, improving by at least 6% when compared to the case with no

TABLE I. Comparison with Prior Arts

	[3] JSSC 2009	[4] TCAS-I 2011	[7] TBCAS 2013	[9] ISSCC 2013	[8] TCAS-II 2012	[10] TVLSI 2016	[11] TPE 2016	**This Work**
Technology	0.35 μm	0.5 μm	0.5 μm	0.35 μm	0.5 μm	0.35 μm	0.35 μm	**0.35 μm**
Topology	Full-wave	Full-wave	Doubler	1X/2X	1X/2X	2X/4X	2X+3-level SIMO	**Doubler**
Frequency	200 kHz-1.5 MHz	13.56 MHz	13.56 MHz	13.56 MHz	13.56 MHz	1 MHz	6.78 MHz	**6.78 MHz**
Input Range	1.2 V-2.4 V	> 3.2 V > 2.9 V**	1.46 V	1.25V-2.5V	2.15 V	4.65 V	N/A	**1 V-1.7 V (R_L=2 kΩ)**
Load Range*	100 Ω-2 kΩ	100 Ω-1 kΩ	300 Ω-1.2 kΩ	500 Ω	500 Ω	3.5 kΩ-15 kΩ	N/A	**200 Ω-2 kΩ**
VCR	94%-95% (R_L= 2 kΩ) 82%-84% (R_L=100 Ω)	76%-81% (R_L=500 Ω)	164.4%	130%-161%	144% (R_L= 500 Ω V_{OUT}= 3.1 V)	N/A	N/A	**186%-192% (R_L=2 kΩ) 170%-176% (R_L=500 Ω)**
PCE	82%-87%** (R_L=100 Ω)	68%-80.2% (R_L=500 Ω)	79% (80%**)	61%-76% (2X mode)	70% (75%**) (R_L=500 Ω)	92.7%	80.5%	**86%-92.2%** (R_L=500 Ω)**

*For PCE higher than 70% ** Simulation results

compensation. R_L = 500 Ω and V_{OUT} = 2.7 V lead to a peak PCE of 92.2% with the highest PCE improvement of 10%. Fig. 5(b) compares the VCRs obtained with and without the delay compensation. We observe more than 24% enhancement over the whole output voltage range when R_L = 500Ω or 2kΩ. The peak VCR of 192% and the highest VCR enhancement of 33% are both obtained when R_L = 2 kΩ and V_{OUT} = 3.3 V. Fig. 6 exhibits the PCEs and VCRs versus R_L (varying from 200 Ω to 2 kΩ). Fig. 6(a) shows the PCEs higher than 85% for both V_{OUT} = 2.5 V and 3.3 V, when R_L < 1 kΩ. On the other hand, when R_L > 500 Ω, the VCRs are higher than 170% for both V_{OUT} = 2.5 V and 3.3 V. Table I shows the comparison with prior works. The proposed active voltage doubler can provide both higher VCR and PCE benefiting from the real-time on/off delay compensation.

IV. Conclusions

In this paper, we presented an active voltage doubler with a real-time on/off delay compensation scheme for IMDs. Based on four feedback loops, we obtained the compensation of the circuit delays under various PVT and load conditions. The simulation results show 10% and 33% improvements on the peak PCE and VCR, respectively. The peak PCE is 92.2% with a 500 Ω load, and the peak VCR 192% with a 2 kΩ load.

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