An Analog-Proportional Digital-Integral Multi-Loop Digital LDO with Fast Response, Improved PSR and Zero Minimum Load Current

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***Abstract*—This work presents a multi-loop digital low dropout regulator (DLDO), with analog-proportional (AP) and digital-integral (DI) controls. The DI part is implemented with shift-register-based coarse-fine tuning for good output DC accuracy and fast recovery. Meanwhile, the AP part, based on an improved low-supply flipped-voltage-follower (FVF), can response fast to the load step and supply ripple. A replica loop is used to adaptively control the AP current for a sufficient dynamic current to against supply ripple, and thus further enhances the power supply rejection (PSR). When the load current is smaller than the digital least significant bit (LSB) current, the AP part takes over the LDO control. In such case, the limit cycle oscillation (LCO) is eliminated, and no longer limits the minimum load current to be zero. Implemented in a 65nm CMOS process, a 0.38ps figure of merit (FoM) and −22dB PSR at 1MHz are measured at 0.6V supply.**

Keywords—low dropout regulator (LDO); proportional-integral (PI) control; power supply rejection (PSR); fast response.

I. Introduction

In granular power management for digital ICs, a low central supply is generated by a switching converter first, and then distributed to fine-grained voltage domains using low-dropout regulators (LDOs). In this sense, a small dropout voltage of LDOs, e.g. <100mV, is favorable for high power efficiency. Moreover, power supply rejection (PSR) to the ripple (typically up to several MHz) from the pre-stage switching converter is required. Good PSR can be achieved by analog LDO (ALDO) over a wide frequency range, but will be degraded due to the reduced loop gain under low supply and small dropout voltages. Also, ALDO output accuracy reduces at low supply. By contrast, digital LDO (DLDO) [1] is suitable for low voltage operation which is more favorable in digital ICs. But the conventional designs only response fast with a high sampling frequency (f_{CLK}) and thus a high quiescent current (I_Q). Therefore, it suffers from poor PSR and load transient response with a low I_Q. In addition, the minimum load current ($I_{LOAD,min}$) of DLDO is constrained by the large limit cycle oscillation (LCO) at the light load condition.

Proportional-integral (PI) control [2-7] is commonly used in LDO for simultaneous fast response and high dc accuracy. [2]-[4] implemented both the P and I paths in digital ways, while [5] used analog circuits as the I path. But a fast sampling circuit is still needed to activate the digital P paths for these schemes. [6] fed the output spike (ΔV_{OUT}) back through an analog high-pass filter (HPF), but it is effective only with a certain number of power transistors turned on. [7] utilizes the intrinsic fast response property of source follower, but requires a charge pump to drive the N-type power switches.

We notice that a fast analog loop can be designed at a low supply voltage (V_{IN}), while the resulting low loop gain of this analog loop can be compensated by a digital integrator, e.g. shift register (SR), for a high DC gain. Therefore, this work incorporates both schemes and proposes a multi-loop DLDO with analog-P and digital-I (AP-DI) controls for a fast response at a low supply voltage. Meanwhile, improved PSR, zero minimum load current, and reduced LCO can be fulfilled with the AP.

II. Working Principle and Implemenation of the Proposed DLDO

A. General Structure

Fig. 1 shows the schematic of the proposed DLDO, comprising both the AP and DI controls. For the AP part, a flipped-voltage-follower (FVF) and its replica is designed. The power transistor M_{PA} and the common-gate (CG) amplifier M_2 compose the fastest loop (Loop-1) to deal with fast load transient and MHz supply ripples. C_1 is added to couple the AC variation to M_{10} for a further output overshoot reduction. A shared error amplifier (EA) (M_3 through M_9) is implemented as Loop-2, achieving a decent gain at a low V_{IN} for certain regulation in all loading conditions. This will be especially useful for the light load condition when the load current (I_{LOAD}) is smaller than the least significant bit (LSB) current of DI ($I_{D\text{-}LSB}$), and all the I_{LOAD} is provided by the AP output current I_A. However, I_A cannot be defined by Loop-2 when $I_{LOAD} > I_{D\text{-}LSB}$ and V_{OUT} is regulated to V_{REF}. To prevent $I_A < 0$ and then AP offers little help to transient response and PSR, Loop-3 is added to define the DC value of I_A ($I_{A\text{-}DC}$), using a replica path (M_{Pr} and M_{2r}) and the shared EA. Additionally, Loop-3 further enhances PSR by about 6dB, to be discussed in Section II.C. The Bode plots in Fig. 2 show good stability of these three analog loops.

For the DI part, it consists of 3 sub-sections (L, M, H), with 16-bit, 8-bit, and 8-bit SR-controlled power switch arrays, respectively. The power switches in these sub-sections are sized to enable equivalent 16×8×8=1024 current steps for a high V_{OUT} DC accuracy, with carry/borrow operations between the

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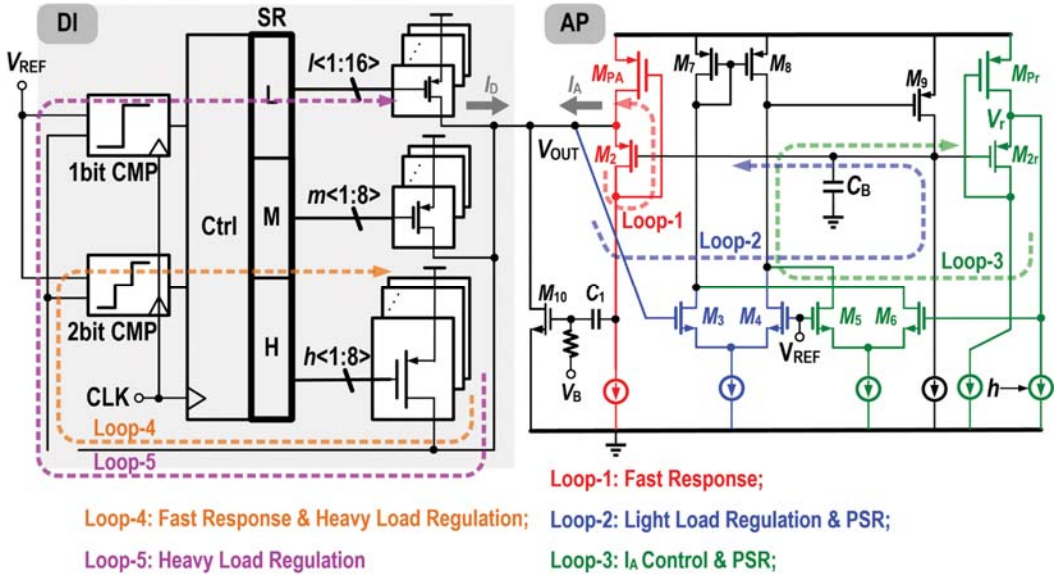

Fig. 1. The full schematic of the proposed DLDO with five control loops, and the function of each loop.

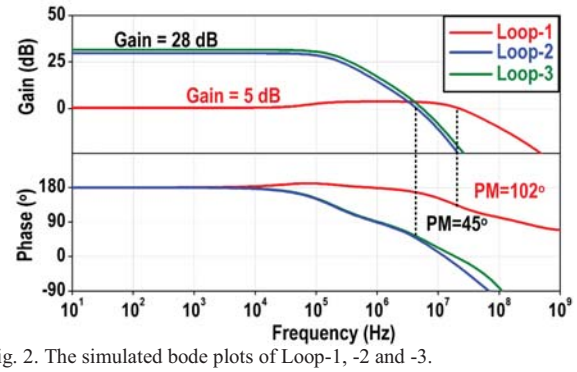

Fig. 2. The simulated bode plots of Loop-1, -2 and -3.

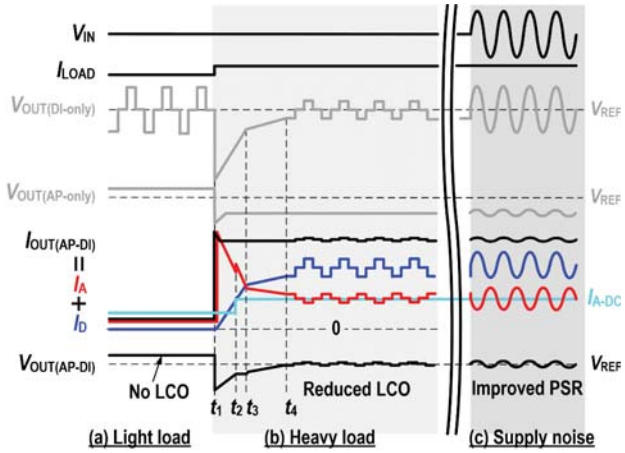

Fig. 3. The working principle of the proposed DLDO in the (a) light load, (b) heavy load, and (c) with supply noise conditions, and its comparison to the AP- and DI-only LDOs.

adjacent sub-sections. A coarse-tuning (Loop-4) triggers the M and H sub-sections for fast recovery, when V_{OUT} exceeds the preset boundaries. Loop-5 is a fine-tuning loop with the L sub-section. The control word of the H sub-section h<1:8> is used as a current indicator, feeding to the replica circuit to adaptively control $I_{A\text{-}DC}$, for a better PSR at heavy load.

B. Working Principle

Fig. 3 shows the working principle of the proposed DLDO. As the light load case in Fig. 3(a), where $I_{LOAD} < I_{D\text{-}LSB}$, the AP part is in charge of the LDO to fulfill I_D=0 and I_A=I_{OUT}. Although V_{OUT} may deviate a little from V_{REF} due to the not sufficiently high loop gain of the AP section, LCO is eliminated in this ultra-light load case, as there is no quantization error and SR switching. Also, $I_{A\text{-}DC}$ is adaptively reduced to improve the DC regulation. Consequently, this LDO can lower the minimum load current to zero, which is not enjoyed by the DI-only DLDOs.

When an I_{LOAD} step occurs at t_1 as the heavy load case in Fig. 3(b), the fast AP section will provide most of the momentary I_{OUT}, preventing a large ΔV_{OUT}. Hence, a low f_{CLK} is allowed for the DI section, reducing power consumption. From t_1 to t_3 and from t_3 to t_4, the DI section operates with coarse and fine tuning, respectively. These resembles a slow but high gain integrator for a high DC accuracy, which can hardly be obtained by the AP-only designs at a low V_{IN} like 0.6V. Meanwhile, I_A decreases as I_D increases until I_A=$I_{A\text{-}DC}$ at t_4, and I_D=I_{OUT}−I_A. Since the fast-changing I_A always compensates for the slow varying I_D, LCO can be reduced in steady-state. When I_D exceeds a preset value (can be sensed by the control word h) at t_2, $I_{A\text{-}DC}$ is adaptively raised. I_A can response inversely to the supply ripple and thus will improve PSR, as illustrated in Fig. 3(c), and to be analyzed as follows.

C. PSR Analysis and Enhancement

The PSR of the proposed LDO can be approximately written as:

$$PSR \approx \frac{Z_{LOAD-CL}}{Z_{LOAD-CL}+r_{ds}} = \frac{1}{1+r_{ds}g_{mA}A_{OL}}, \quad (1)$$

where $Z_{LOAD\text{-}CL}$ is the closed-loop output impedance of the LDO, r_{ds} is the drain-source resistance of the turned-on power

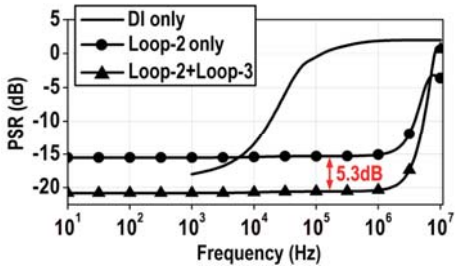

Fig. 4. The simulated PSR under V_{IN}=0.75V, V_{REF}=0.7V, V_{ripple}=40mV$_{pp}$, I_{LOAD}=10mA, f_{ripple}=1MHz, f_{CLK}=5MHz, when DI only, Loop-2 only and both Loop-2 and 3 are applied.

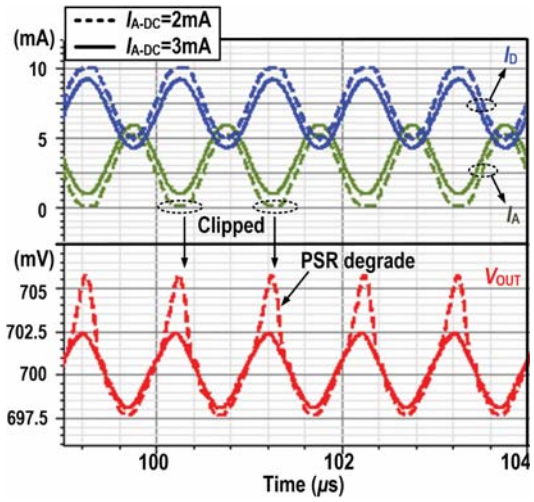

Fig. 5. The simulated transient waveforms of I_D, I_A and V_{OUT} when $I_{A\text{-}DC}$ is set to 2 (dashed line) and 3mA (bold line), respectively, with V_{IN}=0.75V, V_{REF}=0.7V, V_{ripple}=40mV$_{pp}$, I_{LOAD}=10mA, f_{ripple}=1MHz, f_{CLK}=5MHz.

transistors (including M_{PA} and digital power switches), A_{OL} is the open loop gain, and g_{mA} is the transconductance of M_{PA}. It should be noted that the transconductance does not include those of the power transistors in the DI section, because the slow DI operation can be neglected when f_{ripple} approaches f_{CLK}. Hence, the r_{ds}·g_{mA} term here can be much smaller than that of an analog-only LDO especially at heavy load, as I_A is only a small proportion of I_{LOAD}. This obviously undermines the PSR of the LDO.

In this work, Loop-3 is added to address this issue. Firstly, it adaptively reduces the proportion of I_D and sets a proper g_{mA} (proportional to $I_{A\text{-}DC}^{1/2}$) at heavy load, trading with a proportionally larger replica bias current. Secondly, it further improves A_{OL} and PSR, comparing to the conventional Loop-2 only case, because Loop-3 and Loop-2 match well and have almost equal loop gain and contribution to PSR (improved by 5.3dB in simulation as shown in Fig. 4). Thirdly, from the large-signal perspective, the dynamically enlarged $I_{A\text{-}DC}$ allows I_A to swing and handle the large ripple current caused by the supply ripple. Otherwise, the PSR will be much degraded if $I_{A\text{-}DC}$ is too low and the I_A waveform touches 0, as the $I_{A\text{-}DC}$=2mA case shown in Fig. 5.

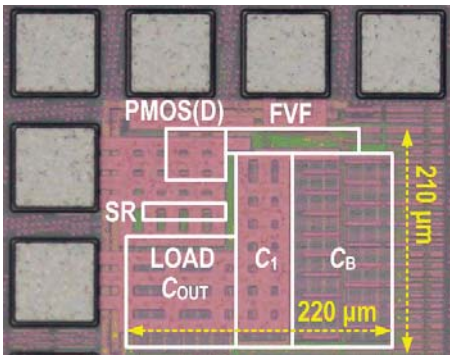

Fig. 6. Chip microphotograph of the proposed DLDO.

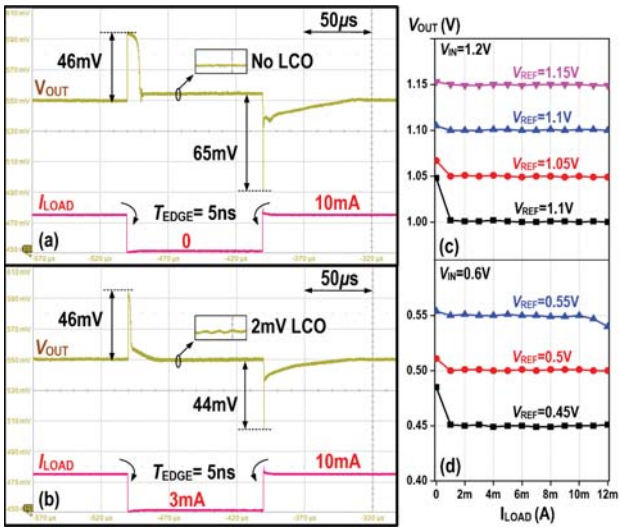

Fig. 7. The measured transient response with a (a) 0-10mA, and (b) 3-10mA I_{LOAD} step, when V_{IN}=0.6V, V_{REF}=0.55V, f_{CLK}=5MHz, with no or only 2mV LCO in the light load conditions; and the measured load regulation with (c) 0.6V and (d) 1.2V V_{IN}, respectively.

III. Measurement Results

The proposed DLDO is fabricated in a 65nm CMOS process. Fig. 6 shows the chip micrograph, with an active area of 0.04mm^2, including a 20pF on-chip output capacitor (C_{OUT}), a 13pF C_1, and a 26pF C_B. Fig. 7(a) shows the measured transient response with V_{IN}=0.6V, V_{REF}=0.55V, and f_{CLK}=5MHz, when I_{LOAD} changes from 0 to 10mA within 5ns edge times (T_{EDGE}). A 65mV undershoot and a 46mV overshoot are achieved, which are mainly determined by the AP loops. For I_{LOAD}=0, V_{OUT} deviates about 6mV from V_{REF}, but has no LCO. For the 3mA to 10mA I_{LOAD} change shown in Fig. 7(b), the V_{OUT} undershoot is reduced to 44mV, and V_{OUT} is well regulated to V_{REF} in the steady state, with about 2mV LCO. And the measured load regulation is shown for V_{IN}=0.6V and 1.2V in Fig. 7(c) and (d), respectively, where a precise regulation is maintained for I_{LOAD}>1mA, due to the adaptive $I_{A\text{-}DC}$ scheme. Fig. 8 shows the measured V_{OUT} transient waveforms for evaluating the PSR. In Fig. 8(a), when V_{IN}=0.75V, V_{REF}=0.7V, and I_{LOAD}=10mA, a 5mV$_{pp}$ V_{OUT} ripple is recorded with 1MHz and 40mV$_{pp}$ input ripples (V_{ripple}). In Fig. 8(b), when V_{IN}=0.6V, V_{REF}=0.5V, the PSR is −22dB at 1MHz. The measured PSR

TABLE I COMPARISON WITH THE STATE-OF-THE-ART WORKS

	[3]	[6]	[4]	[5]	[7]	[8]	**This work**
Year	2017	2017	2018	2018	2018	2018	**2018**
Process [nm]	65	65	65	130	28	65	**65**
Area [mm^2]	0.03	0.034	0.037	0.08	0.0055	0.0014	**0.04**
P-path	Digital	RC HPF	Digital	Digital	NMOS	Digital	**FVF**
I-path	Digital	SR	VCO	Analog EA	SR	SC	**SR**
V_{IN} [V]	0.45-1	0.5-1	0.6-1.2	0.6, 1.1-1.2	0.4-0.55	0.5-0.9	**0.5-1.2**
V_{OUT} [V]	0.4-0.95	0.45-0.95	0.4-1.1	0.5-0.55, 0.8-1.1	0.35-0.5	0.3-0.8	**0.45-1.15**
Max. f_{CLK} [MHz]	N.A.	10	>>3.9	560	4	0.1-1550	**5**
C_{OUT} [pF]	100	100*	40	500	24	165	**20**
$I_{LOAD,\ min}$ [μA]	14	2,000	10,000	30	500	10	**0**
ΔV_{OUT} [mV] @ ΔI_{LOAD} [mA]	34 @ 1.44	105 @ 10	108 @ 50	240 @ 10.3	117 @ 20	20.5 @ 3.25	**65 @ 10*****
1 MHz PSR [dB] @ V_{IN}/dropout [V] /V_{ripple} [V_{pp}]	N.A.	N.A.	−35 @ 1/0.2/N.A.	−12 @ 1.2/0.4/N.A.	N.A.	N.A.	**−18 @ 0.75/0.05/0.04 −22 @ 0.6/0.1/0.065**
I_Q [μA]	8.1-258	3.2	10-1070	26	0.81	48.4	**29*****
FoM [ps]**	20	0.23	1.38	166	0.0057	34.3	**0.38*****

* Total Capacitance. ** FoM=$C_{OUT}\cdot\Delta V_{OUT}\cdot I_Q/I_{OUT}^2$ [9]. *** At V_{IN}=0.6V and V_{REF}=0.55V.

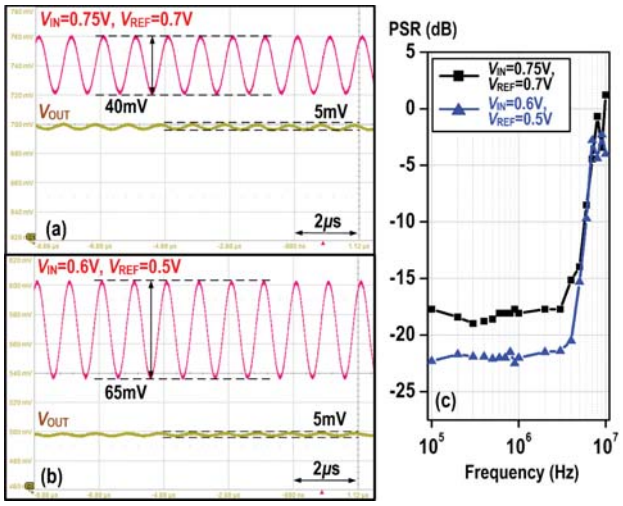

Fig. 8. The measured transient waveforms of V_{IN} and V_{OUT}, with I_{LOAD}=10mA, f_{ripple}=1MHz, f_{CLK}=5MHz when (a) V_{IN}=0.75V and V_{REF}=0.7V, (b) V_{IN}=0.6V and V_{REF}=0.5V; and (c) the summary of the measured PSR from 100K to 10MHz under these two cases.

curves versus frequency are also shown in Fig. 8(c), which are better than −17dB and −21dB up to 3MHz, respectively.

The proposed DLDO is compared with the state-of-the-art works as in Table I. Thanks to the AP-DI architecture, the proposed DLDO contains the fast response and good PSR features of an analog LDO, together with the high DC gain property of a conventional DLDO. Specifically, this work achieves a good PSR performance with a large $V_{ripple}/V_{dropout}$ ratio at a low V_{IN}. In addition, this work reaches $I_{LOAD,min}$=0 with no LCO observed, resulting the maximum $I_{LOAD,max}/I_{LOAD,min}$ ratio. Meanwhile, it achieves a 0.38ps figure-of-merit (FoM) that is comparable or better than the state-of-the-art works.

IV. CONCLUSIONS

This work proposes a multiple-loop DLDO with AP-DI controls. The AP part, implemented with an FVF under low V_{IN}, responses fast to the load step and supply noise. The PSR is further improved with a replica loop, which adaptively adjust the DC operating point of the AP part. The insufficient DC gain of the AP part under low V_{IN} is compensated by the DI section. Meanwhile, this topology reduces the LCO and extends the minimum I_{LOAD} limit to zero, which is a feature that has not been enjoyed by the DLDO works in the literature.

ACKNOWLEDGMENT

This work was supported by the Natural Science Foundation of China (61604044), the International Science & Technology Cooperation Program of Guangzhou (201807010065), and the Macau Science and Technology Development Fund (FDCT)—SKL Fund.

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