A Nonlinearity Digital Background Calibration Algorithm for 2.5bit/stage Pipelined ADCs With Opamp Sharing Architecture

Yuan Fei, Sai-Weng Sin, Seng-Pan U, Rui Paulo Martins[1]
Analog and Mixed Signal VLSI Laboratory (http://www.fst.umac.mo/en/lab/ans_vlsi/index.html)
Faculty of Science and Technology, University of Macau, Macao, China
Tel:+853 83978796, Fax: +853 83978797, email: ma66581@umac.mo
1 – On leave from Instituto Superior Técnico/TU of Lisbon, Portugal

***Abstract*— This paper presents a new digital background calibration algorithm for 2.5bits/stage pipelined analog-to-digital converters (ADCs) with opamp sharing architecture. Background calibration can extract calibration data without interrupting ADCs normal conversion operation. Digital calibration can relax the design difficulty of analog circuits of ADCs, and gains the improvement of technology scaled down. This algorithm provides a method to effectively estimate the nonlinearity of opamp, and calibrates it in digital domain. For a 10bit 2.5bit/stage pipelined ADCs with opamp sharing architecture, only one opamp need to be calibrated to achieve 10bit resolution. Simulation results show that the ENOB can be improved from 5.54b to 8.80b by the proposed algorithm.**

I. INTRODUCTION

Digital background calibration techniques haves been applied to pipelined analog-to-digital converters (ADCs) to improve resolution and/or reduce power dissipation. A pipelined ADC comprises some cascaded stages. For example, a 10bits pipelined ADC with 2.5bits per-stage. It comprises 4 2.5bits stages and a 2bits flash ADC. The 4 stages have 0.5 bit overlap to obtain an 8bits digital output with digital error correction. And for each 2.5bits stage, it comprises a sub-ADC which quantizes the stage's analog input, and a sub DAC which generates a corresponding analog signal with digital output of sub-ADC. Analog input subtract corresponding analog signal of sub-DAC to obtain the residue signal. This residue signal multiply a gain factor ("4" for 2.5 bit per stage), and output signal pass to next stage to do the same process until the final 2 bits flash ADC. Digital calibration corrects the digital output of pipelined ADC, and yielding a linear analog-to-digital (A/D) conversion characteristic. Opamp sharing architecture utilizes the opamp that is unnecessary for sampling phase of pipelined ADC to achieve one opamp sharing with two stages, which can obtain more power efficiency and less area cost.

There are some different background calibration schemes. In some schemes, an extra signal is injected into the signal path, and an additional signal range is required [3]. It needs a long time to converge. In other schemes, an additional ADC channel is required. This channel is used to be a reference to calibrate the main ADC channel [4]. But all of them only extract one gain error factor for each stage. For the high finite gain of opamp, gain error is dominated. But for low finite gain of opamp, nonlinearity becomes more dominated. The conventional linear calibration cannot calibrate gain error efficiently.

In [1], it's an algorithm for 1.5bit pipelined ADCs. The first five stages should be calibrated to achieve the resolution. Proposed algorithm apply to a 2.5bit pipelined ADCs with opamp sharing architecture, this architecture can further improve the calibration speed. To calibrate the nonlinear issue of opamp and further relax the design tradeoff of speed and accuracy of opamp, it needs at least two gain error factors for each stage. With these two gain error factors, the nonlinearity of gain error factor array of opamp can be estimated with a second order polynomial. Using this nonlinear model, the nonlinear gain error of each stage can be calibrated with corresponding output levels.

II. NONLINEARITY OF PIPELINED ADCS

For general pipeline stage, the *j*th stage analog input V_j, is quantized by a sub-ADC. Its digital output D_j, drives a sub-DAC to obtain an analog signal $V_j^{da}(D_j)$. Analog input V_j subtract $V_j^{da}(D_j)$ to obtain a residue signal, and this residue signal multiply gain factor G_j to generate the output signal of *j*th stage V_{j+1}. This is an ideal operation of a pipeline stage. It can be expressed as (1). Generally, switched capacitor circuit is applied to achieve the function of analog input subtract DAC output and multiply gain factor. So the ideal gain factor G_j can be expressed as (2)

$$V_{j+1} = G_j \times \left[V_j - V_j^{da}(D_j)\right] \quad (1)$$

$$G_j = \frac{C_s + C_f}{C_f} \quad (2)$$

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C_s , C_f are sampling capacitors of sample and hold circuit. $D_j \in \{-3,-2,-1,0,+1,+2,+3\}$ is determined with comparison of V_j with the -5/8V_r , -3/8V_r , -1/8V_r and +1/8V_r, +3/8V_r, +5/8V_r, But in reality, the nonlinear finite DC gain A_{0j} and parasitic capacitance of negative input node of opamp C_p also should be considered in gain factor calculation. So the gain factor also can be expressed as (3). And output of DAC $V_j^{da}(D_j)$ can be written as (4).

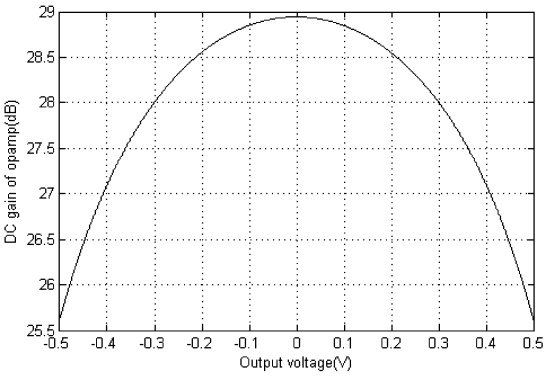

Figure 1. Example of nonlinear DC gain of opamp v.s. output voltage

$$G_j' = \frac{C_s + C_f}{C_f} \times \frac{1}{1 + \frac{1}{A_{0j}} \frac{C_s + C_f + C_p}{C_f}} \quad (3)$$

$$V_j^{da}(D_j) = V_r \cdot \frac{C_s}{C_s + C_f} \times D_j \quad (4)$$

The offset effect due to the input-referred offset voltage of the opamp, the charge injection from the analog switches, and the offset of sub-DAC can be summarized as an offset voltage. This offset voltage can be corrected by digital error correction algorithm. So it is not considered in this transfer function. The output of *j*th stage can be expressed as (5). For 2.5 bit stage, assume that $C_s = 3C_f$. (5) can be rewritten as (6). In (6), the analog input of *j*th stage just multiply a constant factor G_j. If the gain error $G_e$can be measured, and the transfer function of *j*th stage can be calibrated to ideal transfer function (1). This is the concept of calibration.

$$V_{j+1} = G_j' \times \left[V_j - V_j^{da}(D_j)\right] \quad (5)$$

$$V_{j+1} = G_e \times \left[G_j \cdot V_j - V_r \cdot D_j\right] \quad (6)$$

with

$$G_e = \frac{1}{1 + \frac{1}{A_{0j}} \frac{C_s + C_f + C_p}{C_f}} \quad (7)$$

In (7), G_e include the information of nonlinear gain of opamp and input parasitic capacitor of opamp. Assume A_{0j} is a constant. So the gain error $G_e$also can be written as a constant. But in real opamp design A_{0j} is even function of *j*th stage output V_{j+1}, which can be expressed as,

$$A_{0j} = A_{dc} + \sum_{i=1}^{\infty} a_i \cdot V_{j+1}^{2i} \quad (8)$$

A_{dc} represents DC gain of opamp. a_i are gain coefficients of polynomial of A_{0j}(Figure 1). If this output dependent gain is considered as a constant for linear calibration algorithm. After calibration, the output signal which is close to $\pm$Vr has more Inaccurate than the signal around common-mode level, so nonlinear calibration is applied to achieve higher accuracy of pipelined ADCs.

III. Proposed Gain error extraction Method

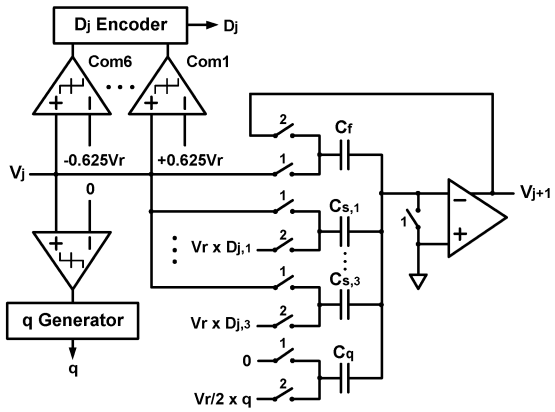

Figure 2. SC pipeline stage with single stage operation

In Figure 2, there is structure applied in 2.5 bit pipeline stage. Six comparators are quantized input signal as typical 2.5bit pipeline stage, and one more comparator and capacitor Cq are added. This comparator controls pseudorandom number generator for injecting pseudorandom number into signal path. The structure can solve the over-range issue when pseudorandom number is injected to signal path. As shown in Figure 3, the comparator at common-mode divide the full rang into two parts, when input signal less than common-mode level, pseudorandom number q can be +1 or 0. When input signals greater than common-mode level, pseudorandom number q can be -1 or 0. If all output signals are collected and be calculated, then one gain error factor can be extracted after calibration. In the proposed work, one more extracted gain factor is needed. The output signals in region A (form -5/8Vr to +5/8Vr) are collected to calculate another gain factor.

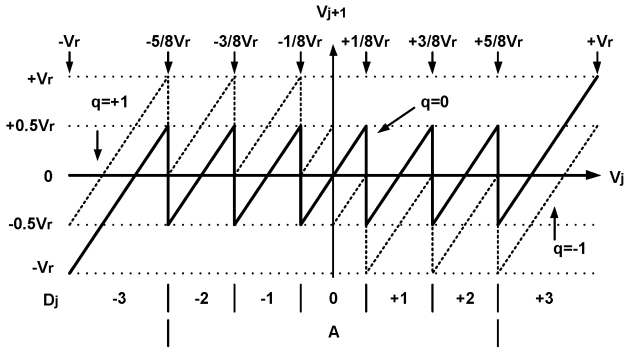

Figure 3. Transfer characteristcis of Figure 2's pipeline stage

And then, there are two gain error factors can be extracted. One is gain error factor of mid-region A of opamp's outputs, another is gain error factor of full-range of opamp's output. This range can be set to different values for each stage. With these two gain error factors, the nonlinearity of opamp can be estimated and calibrated.

IV. NONLINEARITY CALIBRATION ALGRITHM

As eq. (7) shown, all capacitance values are constant for pipeline stage. The only variable in eq. (7) is A_{0j}. It's not difficult to proof if A_{0j} is a even function, that gain error factor G_e has the same characteristic. So the same model can be used to estimate gain error factor G_e.

$$G_{ej} = G_{e0} + \sum_{i=1}^{\infty} b_i \cdot V_{j+1}^{2i} \tag{9}$$

In [2], the digital background calibration extracts gain error factors with correlation-based. This algorithm needs a large number of input samples. For *N*-bit ADC, the order of samples is on the order of 2^{2N}. So the final convergence gain error factor can be considered as the average of these samples. The two gain factors is extracted in Section III also can be considered as the gain average of different output range. Ordinary, the gain error factors of region A is larger than that of full range. (Figure 4)

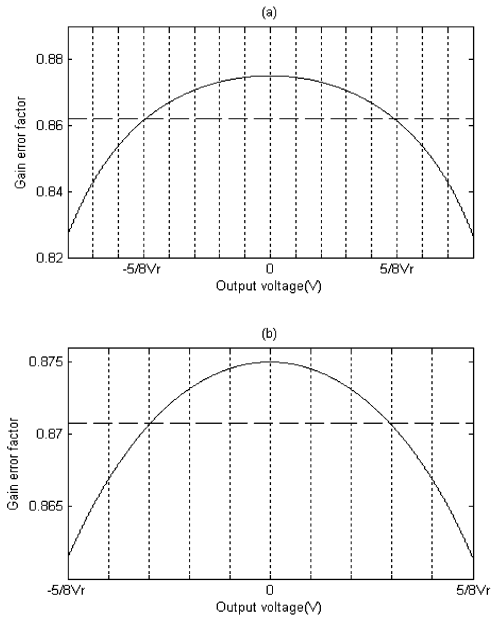

Figure 4. (a) Extraced gain error factor (dash line) and gain error factor(solid line) at full range (b) Extraced gain error factor(dash line) and gain error factor(solid line) at region A .

Two extracted gain error factors can be considered the average of these nonlinear gain error factors at different output range. So, in Figure 4, the area below the dash line (extracted gain error factor) should be equal to the area below the solid line (nonlinear gain error factor curve). With (9), if second order polynomial estimation is taken to approximate the gain error factor curve, the following equations can be written,

$$\begin{cases} \int_{-Vr5/8}^{Vr5/8} G_{e0} + b_1 \cdot V_{j+1}^2 dV_{j+1} = G_{e1} \cdot 2 \cdot (Vr5/8) \\ \int_{-Vr}^{Vr} G_{e0} + b_1 \cdot V_{j+1}^2 dV_{j+1} = G_{e2} \cdot 2Vr \end{cases} \tag{10}$$

In (10), G_{e1}, G_{e2} are extracted gain error factors for region A and full range, respectively. There are two unknown values G_{e0} and b_1 and two equations, so the values of this two coefficients can be obtained by solving equations. And put these two coefficients back to second polynomial estimation of G_e, the rebuild approximation curve can be drawn as Figure 5. With this second order polynomial gain error factor model, each stage is calibrated with an array of 2^{bit} gain error factor values for corresponding output levels, which instead of a single gain error factor value in linear gain calibration. With digital binary output of pipelined ADCs, the corresponding gain error factors of each stage can be identified. With these nonlinear gain error factors and output signals, the rest part of digital calibration is identical with conventional linear digital background calibration works.

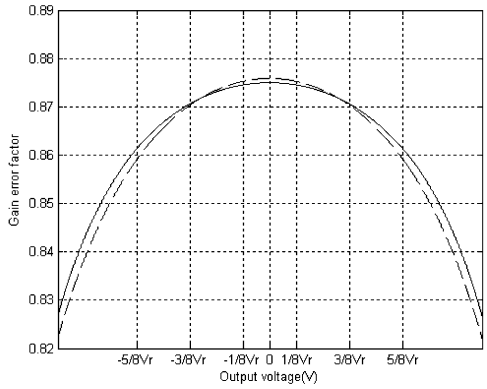

Figure 5. Second order polynomial rebuild G_e,(dash line), and higher order model of G_e for pipeline stage simulation (solid line)

V. SIMULATION RESULTS

The Matlab model of 10bit 200MHz pipelined ADC is applied to test the performance of proposed digital background nonlinearity calibration with first 4 stages of pipelined ADCs. Because there are two gain error factors should be extracted in propose algorithm, the convergence time is longer than conventional linear calibration. So this 2.5bit/stage pipelined ADC with opamp sharing architecture is applied to improve the calibration speed. The first two stages need to be calibrated and only one opamp need to be calibrated with this opamp sharing architecture to achieve 10 bit precision. In opamp model, the higher order polynomial is applied to build nonlinearity of opamp' open-loop gain. The DC gain in opamp model is only 30 dB. Input frequency is 99.8MHz. In table I, it shows that the original opamp with 30dB open loop gain and nonlinear effect, SNDR is only 35.14dB. With linear calibration, finite open loop gain issue can be improved so much and achieve a higher SNDR 47.32dB. But harmonic distortion is still a dominate issue of output. With proposed

nonlinear gain calibration, the harmonic distortion issue also can be suppressed and achieve 54.71dB SNDR.

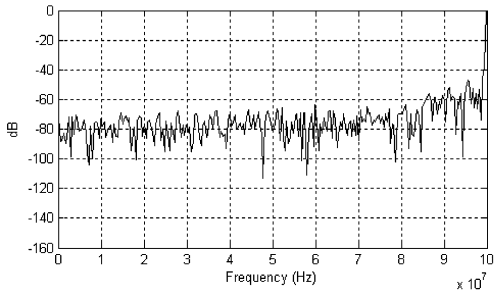

Figure 6. The FFT of output without calibration

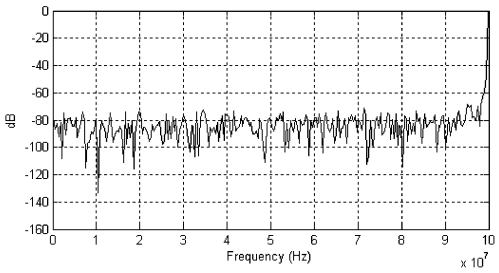

Figure 7. The FFt of output with conventional digital background linear calibration

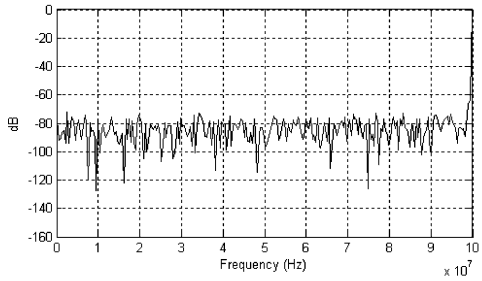

Figure 8. The FFT of output with proposed digital background nonlinear calibration

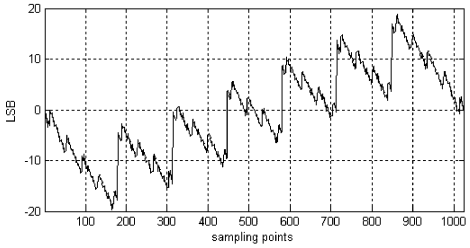

Figure 9. INL of output without calibration

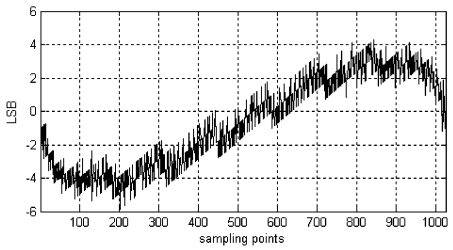

Figure 10. INL of output with conventional digital background linear calibration

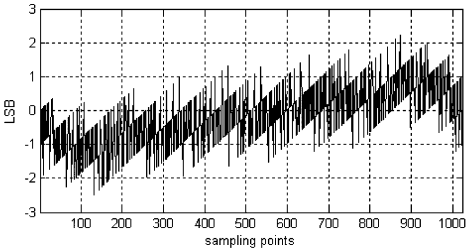

Figure 11. INL of output with proposed digital background nonlinear calibration

TABLE I. SIMULATION RESULTS OF DIFFERENT ALGORITHM

	Comparison of different Algorithm		
	Original output without calibration	***Digital background linear calibration***	***Digital background nonlinear calibration***
SNDR(dB)	35.14	47.32	54.71.
SFDR(dB)	37.35	48.64	63.53
ENOB(bit)	5.54	7.57	8.80
THD(dB)	-36.81	-48.14	-61.53
INL(LSB)	-19.7~+18.8	-5.9~+4.3	-2.5~+2.2

VI. CONCLUSIONS

This paper describes an algorithm of nonlinear digital background calibration for 10bit 2.5bits/stage pipelined ADC with opamp sharing architecture. Comparing with linear digital background calibration, this algorithm can further relax the design difficulty of opamp in pipeline stage or achieve a lower common-mode DC gain and/or higher speed.

VII. ACKNOWLEDGMENT

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VIII. REFERENCES

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